Letters

A Component-Minimized Single-Phase Active Power Decoupling Circuit With Reduced Current Stress to Semiconductor Switches

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***Abstract*—This letter proposes a novel circuit topology which can realize the power decoupling function without adding additional active switches into the circuit. The dc-link capacitor of a full bridge rectifier is split into two identical parts and the midpoint is connected to one leg through a filter inductor. With such a configuration, this leg can control the current going into the two output capacitors connected in series for power decoupling, and the other leg can control the line current according to active and reactive power requirement. The proposed topology does not require additional passive component, e.g., inductors or film capacitors for ripple energy storage because this task can be accomplished by the dc-link capacitors, and therefore its implementation cost can be minimized. Another unique feature of the proposed topology is that the current stress of power semiconductors can be reduced as compared to other existing active power decoupling circuits. This feature becomes more obvious when the converter operates with capacitive load, e.g., for grid voltage support. The operational principle of the proposed circuit is discussed, and experimental results are presented to show the effectiveness of the proposed circuit concept.**

***Index Terms*—AC/DC converter, active power decoupling, capacitance reduction, current stress.**

I. Introduction

PRESENTLY, the dc bus design of single-phase power electronics systems is dominated by electrolytic capacitors (E-caps) because they have relatively high capacitance-to-volume ratio and low cost, and the very large capacitance offered by them can effectively attenuate the double line frequency ripple power that is inherent in single-phase systems [1]. However, these E-caps are also known to have very limited ripple current capability and operation lifetime, which becomes particularly serious under high temperature operation [2]. Directly replacing E-caps with long lifetime film capacitors may not be a viable solution because with the same size and cost, the capacitance of film capacitors can be much lower and the resulting dc-link design will be too bulky and expensive. Therefore, exploration of new techniques for capacitance reduction in single-phase systems has recently become a hot research topic in power electronics, and researchers are particularly interested in photovoltaic and light-emitting diode applications where the system may require more than 20 years of operation lifetime [3].

Instead of simply using large E-caps for ripple power attenuation, various active power decoupling circuits have been proposed to reduce the dc-link capacitance requirement in single-phase systems [4]–[14], and the basic concept of active power decoupling is to use inductors or film capacitors to store the system ripple power in ac form through proper modulation of active circuits. In this case, the instantaneous power from ac side and dc side can be balanced and the dc-link capacitance can theoretically be zero. The reliability of such power electronics systems may be greatly improved because inductors and film capacitors are more robust and generally have much longer lifetime than E-caps.

Despite the active power decoupling circuits are capable of removing the ripple power in the dc-link and reducing the capacitance requirement, a common problem for most of the existing converter topologies is that the power decoupling function is realized with additional active switches and passive energy storage elements, and this may inevitably lead to higher implementation cost. Moreover, the current stress of power semiconductors is also increased because the decoupling circuit needs to handle system ripple power. Therefore, the system conversion efficiency is normally decreased [6], [10], and the efficiency drop becomes the main obstacle for practical implementation of the active power decoupling technique.

In this letter, a novel active power decoupling circuit is proposed to reduce the current stress of semiconductor switches and thus improve the conversion efficiency. It features a very simple circuit configuration and the only additional component as compared to a conventional full bridge pulse-width-modulated (PWM) rectifier is a small filtering inductor. The current stress of power semiconductors is at the similar level as the conventional case and it may become even lower during high load and capacitive load operation. A closed-loop controller is also proposed and it can accurately decouple the ripple power irrespective of circuit parameter deviations, and the proposed circuit concept is finally verified by experimental results.

II. Circuit Configuration and Operating Principles

The topology of the proposed active power decoupling circuit is shown in Fig. 1, where its dc-link is comprised of two identical film capacitors connected in series. As mentioned, these two capacitors are not only used for holding constant dc bus voltage, but also for power decoupling purpose. The midpoint of the

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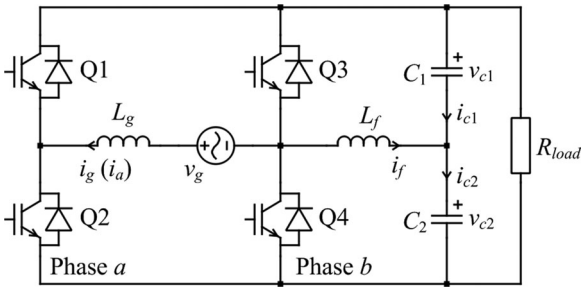

Fig. 1. Proposed single-phase active power decoupling circuit for dc-link capacitance reduction.

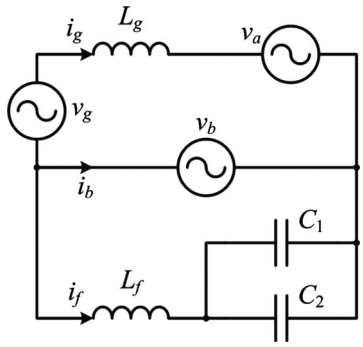

Fig. 2. Ac equivalent circuit of the proposed single-phase power converter.

dc-link is connected to one phase leg of the full bridge through a small filtering inductor L_f, and through proper modulation of this phase leg, the ripple energy can be absorbed by the dc-link film capacitors. The other phase leg in the full bridge should be modulated in such a way that the grid current is sinusoidal, and its line current phase angle is determined by the reactive power requirement. The ac equivalent circuit of the proposed converter is shown in Fig. 2.

To analyze the power flow inside of this circuit, the grid voltage $v_g(t)$ and current $i_g(t)$ are defined as

$$v_g(t) = \sqrt{2}V_g \cos(\omega t) \tag{1}$$

$$i_g(t) = \sqrt{2}I_g \cos(\omega t - \varphi) \tag{2}$$

where capital letters are used to represent rms values. ω is the fundamental angular frequency and φ is the line current phase angle. In order to simplify the analysis, the filter inductance is not considered and the circuit is assumed to be lossless. In this case, the ac side instantaneous input power $p_{ac}(t)$ can be found as

$$p_{ac}(t) = v_g(t)i_g(t) = V_g I_g \cos\varphi + V_g I_g \cos(2\omega t - \varphi). \tag{3}$$

Clearly, the time-varying term of (3) must be cancelled by the compensation network, and in order to achieve this, the voltages of the two film capacitors should contain a fundamental ac component with 180° phase shift, and they are also superposed with a dc component, which equals to half of the dc-link voltage, i.e., $V_{\rm dc}/2$. Because of this, the voltage stress of the two capacitors will be increased by $\sqrt{3}/\sqrt{2}$ times. The two capacitors' voltages can then be defined as

$$v_{c1}(t) = \frac{V_{\rm dc}}{2} - v_c(t) = \frac{V_{\rm dc}}{2} - \sqrt{2}V_c \cos(\omega t + \theta) \tag{4}$$

$$v_{c2}(t) = V_{\rm dc} - v_{c1}(t) = \frac{V_{\rm dc}}{2} + \sqrt{2}V_c \cos(\omega t + \theta) \tag{5}$$

where θ is the phase difference between the grid voltage and the ac component in the decoupling capacitor voltage $v_c(t)$, which can be changed between 0 to $V_{\rm dc}/2$. By differentiating (4) and (5), it is possible to find the upper capacitor current $i_{c1}(t)$, the low capacitor current $i_{c2}(t)$ and the filter inductor current $i_f(t)$ as follows:

$$i_{c1}(t) = C_f \frac{dv_{c1}(t)}{dt} = \sqrt{2}\omega C_f V_c \sin(\omega t + \theta) \tag{6}$$

$$i_{c2}(t) = C_f \frac{dv_{c2}(t)}{dt} = -\sqrt{2}\omega C_f V_c \sin(\omega t + \theta) \tag{7}$$

$$i_f(t) = i_{c2}(t) - i_{c1}(t) = -2\sqrt{2}\omega C_f V_c \sin(\omega t + \theta) \tag{8}$$

where C_f is the capacitance of C_1 and C_2. Similarly, it is easy to derive the instantaneous power $p_f(t)$ provided by this half bridge circuit

$$\begin{aligned} p_f(t) &= v_{c1}(t)i_{c1}(t) + v_{c2}(t)i_{c2}(t) \\ &= -2\omega C_f V_c^2 \sin(2\omega t + 2\theta). \end{aligned} \tag{9}$$

Since both V_c and θ are controllable through the modulation of Q3 and Q4 shown in Fig. 1, it is possible to equate (9) to the time-varying terms shown in (3) as follows:

$$\theta = -\frac{\pi}{4} - \frac{\varphi}{2} \quad \text{or} \quad \theta = \frac{3\pi}{4} - \frac{\varphi}{2} \tag{10}$$

$$V_c = \sqrt{\frac{V_g I_g}{2\omega C_f}}. \tag{11}$$

In this case, the ripple power can be absorbed by the two decoupling capacitors and will not appear in the dc-link. The required dc-link capacitance for maintaining constant bus voltage can be significantly reduced.

III. Current Stress Analysis

The current stress of power semiconductors is particularly of interest because it may directly determine the switching and conduction losses. According to (2) and (8), the rms value of phase *b* current $i_b(t)$ can be found as

$$\begin{aligned} I_b &= \frac{|i_b(t)|}{\sqrt{2}} = \frac{|i_g(t) + i_f(t)|}{\sqrt{2}} \\ &= |I_g \cos(\omega t - \varphi) - 2\omega C_f V_c \sin(\omega t + \theta)| \\ &= \sqrt{(I_g \cos\varphi - 2\omega C_f V_c \sin\theta)^2 + (I_g \sin\varphi - 2\omega C_f V_c \cos\theta)^2} \\ &= \sqrt{I_g^2 - 4\omega C_f V_c I_g \sin(\varphi + \theta) + (2\omega C_f V_c)^2}. \end{aligned} \tag{12}$$

In order to analyze the current stress of power semiconductors, two special cases of operation are considered. First, the unity power factor operation is considered where $\varphi = 0$. By neglecting the filter inductance shown in Fig. 2, the phasor diagram of the proposed converter with unity power factor operation can

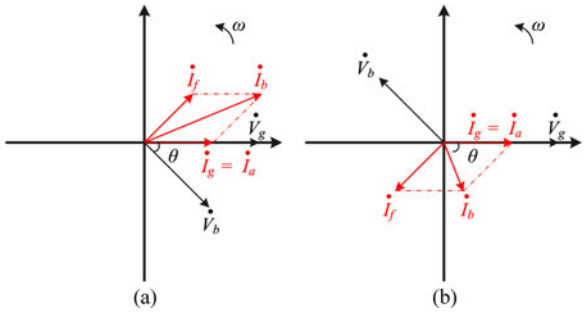

Fig. 3. Phasor diagram of the proposed converter with unity power factor operation when (a) $\theta = -\frac{\pi}{4}$ and (b) $\theta = \frac{3\pi}{4}$.

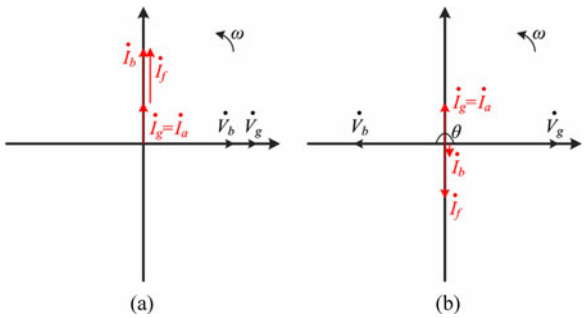

Fig. 4. Phasor diagram of the proposed converter with capacitive load operation when (a) $\theta = 0$ and (b) $\theta = \pi$.

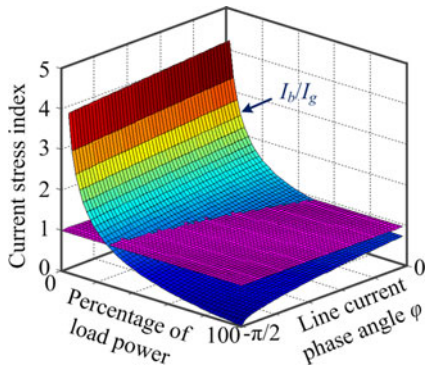

Fig. 5. Current stress index of phase b as a function of the load power and line current phase angle.

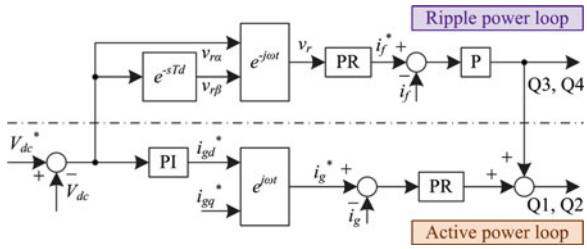

Fig. 6. Dual voltage control for the proposed power decoupling converter.

be presented in Fig. 3. From this figure and also (12), it is clear that the operation with $\theta = -\frac{\pi}{4}$ should be avoided because it may lead to even higher switching current in phase b. Therefore, with $\theta = \frac{3\pi}{4}$, (12) can then be simplified as

$$I_b = \sqrt{I_g^2 - 2\sqrt{2}\omega C_f V_c I_g + (2\omega C_f V_c)^2}. \tag{13}$$

Substituting (11) into (13), it is possible to derive that

$$I_b = \sqrt{I_g^2 - (2\omega C_f V_c)^2 \left(\frac{\sqrt{2}V_c}{V_g} - 1\right)}. \tag{14}$$

The aforementioned equation indicates that if $\sqrt{2}V_c > V_g$, the switching current in phase b can actually be lower than that of the one in a conventional full bridge converter, where $I_a = I_b = I_g$ always holds true. This circumstance may happen during high load operation because V_c increases with the load power as can be seen from (11).

It is more interesting to investigate the second special case where only capacitive load is assumed and $\varphi = -\frac{\pi}{2}$. In this case, the converter is operated to provide reactive power support to the utility grid. The corresponding phasor diagram is shown in Fig. 4 and similarly, the operation with $\theta = 0$ should always be avoided because the grid current will be in alignment with the filter inductor current, making the switching current in phase b to be even higher. In contrast, the two phase currents are directly cancelled with each other when $\theta = \pi$, and the resulting current stress of Q3 and Q4 can therefore be significantly reduced.

The proposed converter topology is however not recommended for inductive load operation, because it will either suffer from high current stress or high dc bus voltage requirement, e.g., more than double of the peak ac input voltage. Moreover, under no load operation, phase b needs to produce zero voltage because the ripple power is zero. In this case, phase a has to cover the total grid voltage, indicating that the required dc bus voltage should be at least double of the peak ac voltage. Since the switching losses are directly related to the dc bus voltage, a load-dependent adaptive dc voltage control method could be implemented to improve the system efficiency and this will not be further discussed in this letter.

By defining the current stress index to be I_b/I_g, a more generalized analysis of phase b current can be shown as the 3-D plot in Fig. 5, where it is clear that, in high load and capacitive load regions, the current stress index is lower than 1, implying reduced current stress to Q3 and Q4. For low load operation, phase b current can be much higher than the conventional case, but this will not increase the power loss by too much, because the amplitude of phase current is very low in this situation.

IV. System Controller Design

As mentioned, the objective of power decoupling in the proposed converter can be realized by controlling the voltages of decoupling capacitors to their reference values as dictated by (10) and (11). However, doing this may require the calculation of the square root function and inverse trigonometric function, if the instantaneous power of inductors is also considered [9]. This can be computation intensive for digital signal processor

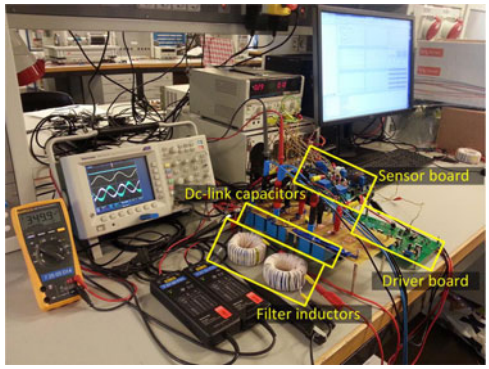

Fig. 7. Photo of the laboratory test bed.

TABLE I
CIRCUIT PARAMETERS USED FOR THE EXPERIMENTAL TESTS

Description	Symbol	Value
Nominal power	P_n	1 kW
Switching frequency	$f_{\rm sw}$	19.2 kHz
Line frequency	f_n	60 Hz
Grid voltage	V_g	120 V
Dc-link voltage	$V_{\rm dc}$	350 V
Dc-link capacitance	C_1/C_2	90 μF
Filter inductance	L_g/L_f	1 mH
Nominal load	$R_{\rm load}$	122.5 Ω

TABLE II
KEY COMPONENTS USED FOR THE EXPERIMENTAL PROTOTYPE

Component	Description
$Q_1 \ldots Q_4$	IKW30N60T, 30 A/600 V, INFINEON
L_g/L_f	85 turns, 50 × AWG#32, Core MS-301060-2, MICROMETALS
C_1/C_2	B32776E8306K, 30 μF/800 V, EPCOS

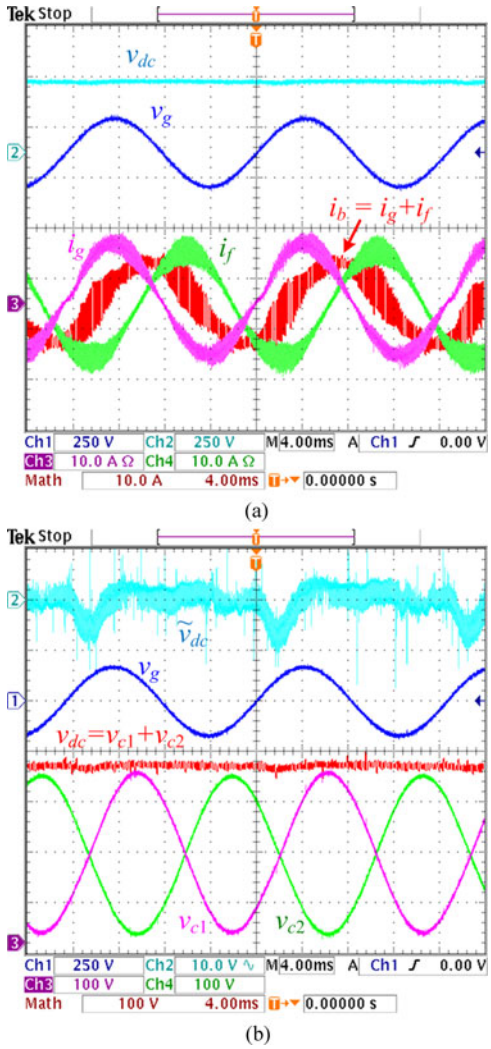

Fig. 8. Experimental steady-state waveforms with 800-W resistive load operation. (a) $v_{\rm dc}$ and v_g: 250 V/div; i_g, i_f, and i_b: 10 A/div. (b) $v_{\rm dc}$: 10 V/div ac coupled; v_g: 250 V/div, $v_{\rm dc}$, v_{c1}, and v_{c2}: 100 V/div.

implementation. Moreover, since the reference is obtained in an open-loop manner based on the power balancing (3) and (9), it will be very difficult to achieve perfect power decoupling if there are uncertainties and disturbances in the system, e.g., varying inductance due to the nonlinearity of magnetic components and varying capacitance due to component tolerance and aging effect.

In order to solve this issue, the dual voltage control scheme proposed in [15] is adopted in this letter and its complete control block diagram is shown in Fig. 6. As shown, it features a dual-loop control structure with one voltage control loop implemented in the stationary reference frame for ripple power decoupling, and another one implemented in the synchronous reference frame for active decoupling balancing. The voltage vector of phase *b* is solely determined by the ripple power control loop and its dynamic model can be found in [15]. Since the ripple voltage $v_{r\alpha}$ in the dc-link is of second order, it is delayed by quarter-cycle T_d so that its orthogonal counterpart $v_{r\beta}$ can be obtained and the harmonic to fundamental reference transformation can be performed. The fundamental reference frame ripple voltage v_r can then be mitigated by a proportional-resonant (PR) controller tuned at the same frequency. The output of this PR controller sets the reference i_f^* for the inner current control loop, where only a proportional (P) gain is used because the inductor current i_f is not necessarily to be sinusoidal. In this case, the current control output becomes a fundamental component, which can be directly used for modulation of phase *b*.

The active power control follows the standard controller design of a PWM rectifier. The dc-link voltage is regulated by a simple proportional-integral controller, whose output may determine the *d*-axis current reference i_{gd}^*. The *q*-axis current reference i_{gq}^* is adjusted according to the reactive power requirement. These two variables are then transformed into the stationary reference frame in order to obtain the current reference i_g^*. The inner current control loop employs another PR controller for sinusoidal current regulation. It should be noted that there is no low-pass filter or notch filter placed in the voltage control loop to remove the second order harmonic, because this task is already done by the ripple power control and the dc-link voltage

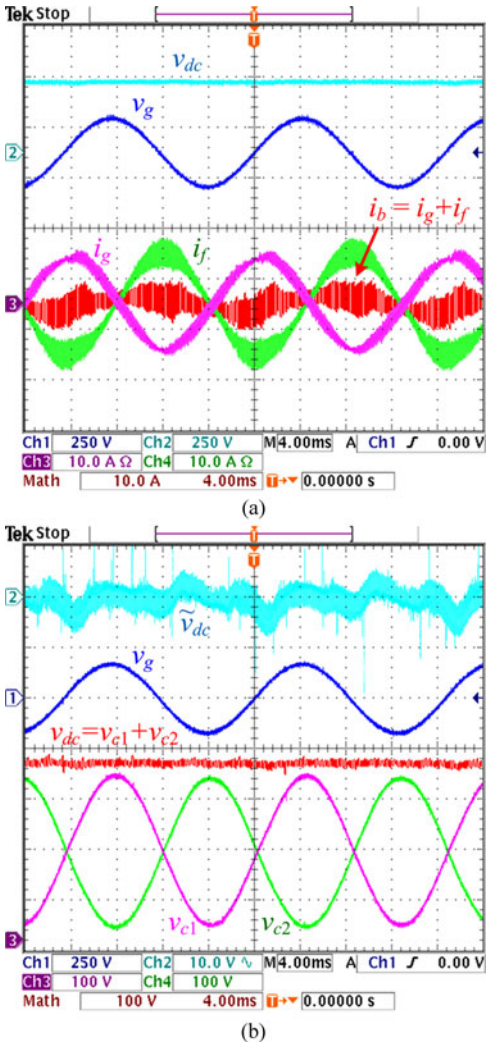

Fig. 9. Experimental steady-state waveforms with 700-VA capacitive ($\cos\varphi = 0.141$, leading) load operation. (a) $v_{\rm dc}$ and v_g: 250 V/div; i_g, i_f, and i_b: 10 A/div. (b) $v_{\rm dc}$: 10 V/div ac coupled; v_g: 250 V/div; $v_{\rm dc}$, v_{c1}, and v_{c2}: 100 V/div.

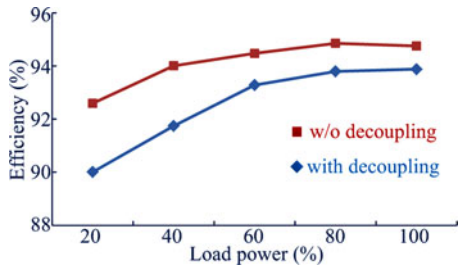

Fig. 10. Efficiency curve of the proposed converter compared with that of a conventional PWM rectifier.

controller can generate a clean sinusoidal current reference. In this case, the control bandwidth design becomes more flexible and it is not limited by the second-order harmonic. The controller gains for both ripple power and active power loops are chosen in such a way that the bandwidth of the inner current control loop is slightly less than one tenth of the sampling frequency, and the bandwidth of the voltage control loop is around one fifth of that of the current one. Eventually, the outputs of the two control loops are summed together in order to produce the voltage vector of phase *a* and also decouple the mutual effect between the two phases.

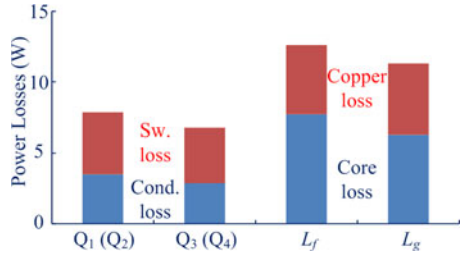

Fig. 11. Estimated loss distribution of the proposed converter with 800-W load operation.

V. Experimental Results

A prototype was implemented in the laboratory as shown in Fig. 7, and the used parameters are listed in Table I. The part numbers of the active and passive components are listed in Table II. The control algorithm was implemented with a Dspace1006 platform and the PWM was generated by a DS5101 digital waveform output board, whose clock frequency is 40 MHz. The ac power grid was emulated by a Chroma programmable ac source 61502, and the experimental waveforms were captured from a Tektronix TDS 3014C digital oscilloscope.

Fig. 8 shows the steady-state experimental waveforms when the converter is operated with 800-W load power. As expected, the filter inductor current i_f is lagging the grid voltage v_g by approximately $3/4\pi$ as shown in Fig. 8(a). This result is in consistence with the phasor diagram shown in Fig. 3(b). It is also noted that the switching current in phase *b* becomes smaller than the grid current. This implies that it is possible to achieve higher conversion efficiency through optimal design and selection of passive and active components. The zoom-in view of the dc-link voltage is shown in Fig. 8(b), where it is clear that the voltage variation is less than 10 V if the switching noise is not considered. The very smooth dc-link voltage is mainly contributed by the power decoupling function of C_1 and C_2 as well as the dual voltage closed-loop control.

Its experimental waveforms under 700-VA capacitive load operation are presented in Fig. 9, where the two inductor currents are basically opposite in phase and the resulting switching current in phase *b* becomes very small. The dc-link voltage variation is still negligible because of the tight regulation of the dual voltage control. Under both cases, the grid current is almost sinusoidal with low total harmonic distortion as the dc-link voltage controller can output a clean reference for the inner current control loop. The two capacitor voltages are always opposite in phase but contain the same dc offset. This matches well with the relationship defined by (4) and (5).

The efficiency curve of the proposed power decoupling converter is shown in Fig. 10 and compared with that of a conventional PWM rectifier. As can be seen, the efficiency drop

becomes smaller as the load power increases, and this is due to the fact that the current stress of Q3 and Q4 is relatively reduced as shown in Fig. 5. The system efficiency drop under high load operation is less 1% and this result is better than those reported in [6] and [8]. The estimated power loss distribution is shown in Fig. 11, and the system efficiency can be further improved by optimizing the switch selection, gate driver and filter inductor design.

VI. Conclusion

In this letter, a novel active power decoupling circuit is proposed for single-phase systems in order to reduce the dc-link capacitance. The proposed circuit is derived from a conventional full bridge rectifier, and it does not require any additional active switch or energy storage component for realization of power decoupling. Moreover, the current stress of one phase leg under high load and capacitive load operation can be lower than that of a conventional full bridge rectifier and therefore, it is possible to improve the conversion efficiency, which is the main challenge for other existing active power decoupling solutions. With a dual voltage closed-loop control, the proposed converter may exhibit excellent power decoupling performance regardless of system uncertainties and disturbances, and its effectiveness is also validated through laboratory experimental results.

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