Study and Handling Methods of Power IGBT Module Failures in Power Electronic Converter Systems

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***Abstract*—Power electronics plays an important role in a wide range of applications in order to achieve high efficiency and performance. Increasing efforts are being made to improve the reliability of power electronics systems to ensure compliance with more stringent constraints on cost, safety, and availability in different applications. This paper presents an overview of the major failure mechanisms of IGBT modules and their handling methods in power converter systems improving reliability. The major failure mechanisms of IGBT modules are presented first, and methods for predicting lifetime and estimating the junction temperature of IGBT modules are then discussed. Subsequently, different methods for detecting open- and short-circuit faults are presented. Finally, fault-tolerant strategies for improving the reliability of power electronic systems under field operation are explained and compared in terms of performance and cost.**

***Index Terms*—Fault detection, fault tolerant, insulated-gate bipolar transistor (IGBT) modules, physics-of-failure (PoF), power electronics, reliability.**

I. Introduction

POWER electronics, the technology for efficiently converting electric power from one stage to another, is used a wide range of applications to achieve high efficiency and performance. The field of power electronics has grown during the last few decades owing to two primary reasons: Development of fast semiconductor switches capable of switching rapidly and handling high power and production of advanced microcontrollers that can implement advanced and complex control algorithms. These factors have led to the development of cost-effective and grid-friendly converters [1], [2]. Moreover, innovative solutions in circuit topology, control strategy, and sensor and system integration have also contributed to the advancements in the development power electronics field [3]. The performance of power electronic systems, especially in terms of efficiency and power density, has been significantly improved by intensive research and advancements in the aforementioned areas.

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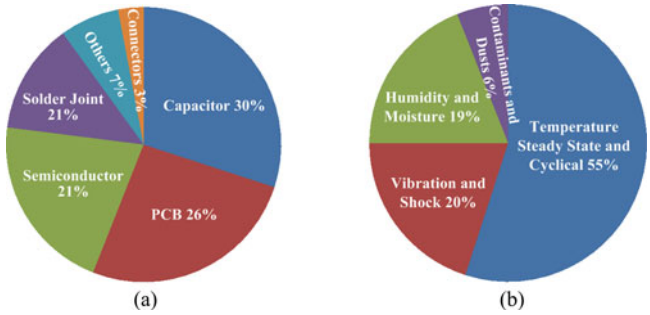

Fig. 1. Distributions of (a) faults in power converter (b) stress sources [7].

Automotive and aerospatiale industries have increasingly stringent reliability constraints into power electronic systems because of safety requirements. Additionally, the industrial and energy sectors are following the same trend by aiming to improve the reliability of power electronics systems with cost-effective and sustainable solutions [4]. The three widely studied research areas in the power electronics reliability are as follows. First is the analysis of the causes and process of failure of power electronics products. Second is design for reliability and sufficient robustness in power electronics products. Finally, intelligent control and monitoring condition to ensure reliable field operation under specific conditions [3].

A power device is one of the vulnerable components of power electronic converters [5]. As shown in Fig. 1(a), semiconductor and soldering failures in device modules account for 34% of failures in converter system. According to a survey based on over 200 products of 80 companies, semiconductor power devices have been selected by 31% of responders as the most fragile components [6]. Fig. 1(b) shows the sources of stressor that have significant impact on reliability [7], [8]. Temperature stressor has the most impact on the reliability of power electronic components and systems. Other factors such as humidity and vibration are very closely related to the failure of power devices.

As mentioned above, the reliability of power devices is very closely related to the reliability of overall power electronics system. Therefore, power device faults and their handing methods in power converters must be investigated for improving the reliability of power electronic systems.

This paper first presents an overview of the major failure mechanisms of power IGBT modules. Methods for lifetime prediction and junction temperature estimation of IGBT modules are then discussed. Thereafter, fault detection methods are presented by classifying faults as open- and short-circuit faults. Finally, different fault-tolerant strategies for improving the

TABLE I
COMPARISON OF CHARACTERISTICS OF WIRE-BONDED AND PRESS-PACK IGBT MODULES

Characteristic	Wire-Bond Module	Press-Pack Module
Power density	Moderate	High
Reliability	Moderate	High
Cost	Moderate	High
Failure mode	Open circuit	Short circuit
Easy maintenance	Better	Worse
Insulation of heat sink	Yes	No
Thermal resistance	Moderate	Small
Switching loss	Low	Low
Conduction loss	High	High

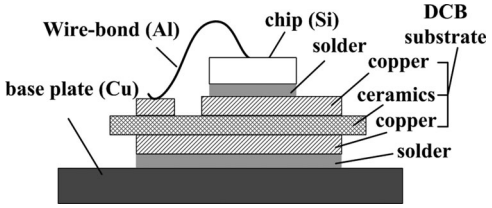

Fig. 2. Structure of a conventional IGBT power module package [27].

reliability of power electronic systems under field operation are discussed and compared in terms of performance and cost.

II. FAILURES IN IGBT MODULES

IGBT modules are typically classified into two types: Wire-bonded IGBT modules and press-pack IGBT modules. They have different characteristics which is a tradeoff between cost and performance, as shown in Table I [9].

IGBT modules have a larger thermal resistance, a lower power density, and higher failure rate because of soldering and bond-wire connection of the internal chips. Press-pack packaging technology improves the connection between chips by direct press-pack contact. Therefore, press-pack IGBT modules have better reliability, higher power density, and better cooling capability. However, their cost is also higher than that of conventional IGBT modules. Therefore, wire-bonded power device modules are still widely used in power electronics area and it is the main used device. Therefore, the failure mechanisms of the conventional wire-bond IGBT modules are presented.

A wire-bonded IGBT is made up of several layers consisting of different materials. The silicon chip is soldered on the direct copper-bonded (DCB) ceramic substrate. The DCB substrate insulates the Si chip from the baseplate and conducts the heat dissipated by the chip to the cooling system. Finally, the top side of the Si chip is contacted by aluminum (Al) bond wires [10]. Fig. 2 shows the structure of a wire-bond IGBT modules package.

The weak points in the wire-bond IGBT modules are the wire bond and silicon interconnection, the silicon and DCB substrate solder joint, and the DCB substrate and baseplate solder joint. The primary failure mechanism in the IGBT module is the wire-bond liftoff. Al and Si material have different coefficients of thermal expansion (CTE), and thermal cycling causes repeated cooling and heating, thus allowing the disparately joined materials to expand and shrink at different rates when stress is applied at the point of contact. This CTE mismatch with temperature swing leads to the wire-bond liftoff failure.

TABLE II
COEFFICIENTS OF THERMAL EXPANSION AND THERMAL CONDUCTIVITIES OF MATERIALS

Material	CTE (10^{-6} K^{-1})	Thermal Conductivity (W m^{-1} K^{-1})
Al_2O_3	6.8	24
AlN	4.7	170
Si_3N_4	2.7	60
BeO	9	250
Al	23.5	237
Cu	17.5	394
Mo	5.1	138
Si	2.6	148
AlSiC	7.5	200

Another dominant failure mechanism is solder joint fatigue. Two solder joints are present in a standard IGBT module between Si and DCB and between DCB and the baseplate. The CTE mismatch between DCB substrate and baseplate is higher than between DCB substrate and Si. Therefore, the possibility of failure is higher in the solder joint between DCB and the baseplate [11]–[13]. This solder joint degradation increases the thermal resistance of the power device module. Therefore, the temperature in the module increases, thus accelerating the lifting of wire-bond [14]. Table II shows the CTE and thermal conductivities of materials typically used in module packaging technology [15].

To improve the lifetime of a power device module, a new packaging technology has been proposed in [16] and [17]. The Al bonding wire was replaced with Cu bonding wire to reduce CTE mismatch, and a silver diffusion sintering technology was employed between the silicon die and the DCB substrate to replace the solder interconnection. With this technology, the CTE mismatches in the modules are reduced, and the lifetime of the power device module is increased.

The wear-out failure discussed above typically occurs due to long-term degradation; however, different types of catastrophic failures can also occur because of a single overstress event. Unlike wear-out failures, catastrophic failures are difficult to predict and handle. Therefore, power converters based on power device modules can be seriously damaged. The catastrophic failures in IGBTs can be classified as open- and short-circuit faults as shown in Fig. 3 [3], [18].

It should be noted that both wear-out and catastrophic failures can lead to the same failures such as bond wire liftoff. However, wear-out failure occurs because of long-term degradation, and catastrophic failures are due to a single overstress event in a short duration [3].

III. LIFETIME PREDICTION OF IGBT MODULE

The lifetime of the IGBT module must be predicted to design power converters with specific reliability. Lifetime prediction models can be used to estimate the life expectancy of a device module under certain operating conditions. Lifetime

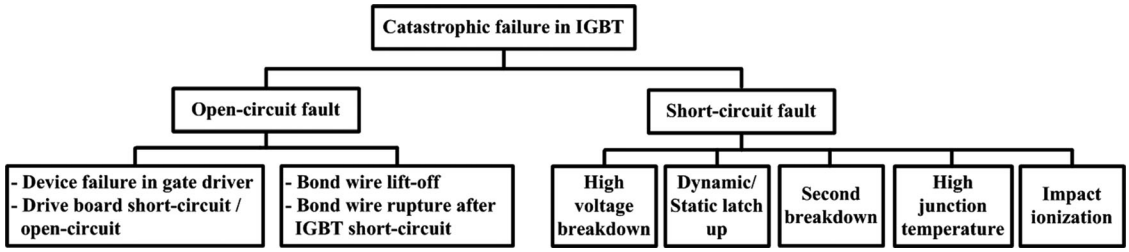

Fig. 3. Catastrophic failures in IGBT modules [18].

prediction models are mostly developed considering wear-out failures caused by long-term degradation due to stresses such as temperature, voltage, current, vibration, humidity, and cosmic radiation level and not catastrophic failures. In this section, lifetime prediction models and junction temperature estimation methods for predicting lifetime are introduced. The lifetime prediction models can be classified into empirical and more physical-based models [10].

A. Lifetime Prediction Models

1) Empirical Lifetime Models: The lifetime of a power module can be predicted analytically using Miner's rule for damage accumulation. These approaches estimate the lifetime of a device module in terms of the number of cycles to failure N_f considering variable factors such as temperature variation, medium temperature, frequency, and wire-bond current. The primary drawback of the analytical models is that the number and amplitude of temperature cycles cannot be accurately determined from a given temperature profile. Therefore, numerous methods have been proposed to extract the number and amplitude of temperature cycles from a temperature profile, and the rainflow counting algorithm is the most commonly used method [10]–[12], [19], [20].

a) Coffin–Manson model: The simple Coffin–Manson model is expressed as

$$N_f = \alpha \times (\Delta T_j)^{-n} \tag{1}$$

where ΔT_j is the temperature variation of the junction, and parameters α and *n* can be obtained through numerical simulations or experimental measurements. This model only considers the effect of temperature variation and not that of average temperature, thermal cycle time, and geometry.

b) Coffin–Manson–Arrhenius model: This model is an improvement over the simple Coffin–Manson model and takes into account the average temperature (T_m) and ΔT_j. This model is expressed as

$$N_f = \alpha \times (\Delta T_j)^{-n} \times e^{E_a/(k \times T_m)} \tag{2}$$

where *k* is the Boltzmann constant and E_a is the activation energy parameter, which can be determined experimentally. This model is widely used because it is simple.

c) Bayerer model: The Bayerer model, given by (3), is the most comprehensive analytical model. It has a large number of parameters, and it considers variations in different parameters of power cycling and power module characteristics [21]

$$N_f = K \times (\Delta T_j)^{\beta_1} \times e^{\beta_2/(T_{j\max}+273K)} \times t_{\text{on}}^{\beta_3} \times I^{\beta_4} \times V^{\beta_5} \times D^{\beta_6} \tag{3}$$

where $T_{j\max}$ is the maximum junction temperature, and t_{on} is the heating time. Further, *I* is the applied dc current, and *D* and *V* are the diameter of bond wires and blocking voltage, respectively. The constants *K* and β are extracted from a large volume of data collected from long-term reliability experiments.

d) Lifetime model for advanced power modules with sintered chips: Recently, a new lifetime model of bond-wire fatigue for advanced power modules with sintered chips has been proposed in [22]. This new model considers not only all the above factors but also the effect of diodes in power device modules. This model is defined as

$$N_f = A \cdot \Delta T_j^{a} \cdot ar^{\beta_1 \cdot \Delta T_j + \beta_0} \cdot \left(\frac{C + t_{\text{on}}^{\gamma}}{C+1}\right) \cdot \exp\left(\frac{E_a}{k_B \cdot T_m}\right) \cdot f_{\text{Diode}} \tag{4}$$

where ΔT_j is the temperature swing, and T_m is the average temperature. Further t_{on} is the pulse duration, and *ar* and f_{Diode} are the wire-bond aspect ratio and derating factor for the test on freewheeling diodes, respectively.

2) Physical Lifetime Model: Physical lifetime models do not require the knowledge of the number and amplitude of thermal cycles; however, the failure mechanisms must be known [19]. They are based on the knowledge of stress–strain deformation within devices; this information can be obtained either through simulations or experiments.

a) Lifetime models for solder joint: The physical lifetime models for the estimation of lifetime of solder joints can be divided into stress-, strain-, energy-, and damaged-based models. Among these, energy-based models are the most convenient and produce more accurate results when compared with the other models because they have the ability to capture test conditions more accurately [20]. Energy-based models form the largest group of models. These models are used to predict fatigue failures on the basis of a hysteresis energy term or type of volume-weighted average stress-strain history. Fatigue energy is calculated from some correlation to the energy under the stress–strain hysteresis loop [23]. Some energy-based models were proposed previously. Akay *et al.* [24] proposed a fatigue

model based on total strain energy, as given by

$$N_f = \left(\frac{\Delta W_{\text{total}}}{W_0}\right)^{1/k} \tag{5}$$

where N_f is the mean cycle to failure, and ΔW_{total} is the total strain energy. In addition, $W_0 = 0.1573$ and $k = -0.6342$ are the fatigue coefficients. These constants were experimentally derived from testing lead-based solder joints.

Lee *et al.* [23] has developed a fatigue life prediction methodology that considers the geometry of a solder joint. The fatigue life is calculated on the basis of an energy-based fatigue criterion as given by

$$N_f = C\,(W_{\text{ss}})^{-m} \tag{6}$$

where W_{ss} is the stress–strain hysteresis energy density, and *C* and *m* are the temperature-dependent material constants derived from low-cycle fatigue test.

Pan [25] proposed a strain energy-based fatigue model referred to as critical accumulated strain energy or CASE. This model is developed under the assumption that strain energy accumulates during thermal cycling and eventually reaches a critical value *C*. This fatigue model is given as follows:

$$C = N_f(aE_p + bE_c) \tag{7}$$

where N_f is the number of cycles to failure, and *C* is defined as the critical strain energy density and was considered to be 4.55 Mpa/mm^3 for the range of tests performed. Moreover, the constants *a* and *b* are determined from multiple linear regression of finite element analysis (FEA) results. The creep and plastic energies denoted by E_c and E_p were also calculated using FEA.

b) Lifetime models for wire bond: Besides the physics lifetime models of solder joint, the lifetime models for Al wire bond also has been proposed [73]–[75]. The most common lifetime model for wire bond is the plastic strain-based fatigue model. This model has been developed under the assumption that the wire bonds is under the plastic strain regime due to large thermomechanical mismatch between Si and Al. This is based on the Coffin–Manson relationship which defines a power law relation between the number of cycles to failure N_f and the plastic strain induced per cycle (ε_{pl}) for low-cycle fatigue. This model can be defined as

$$N_f = C_1(\Delta\varepsilon_{pl})^{-C_2} \tag{8}$$

where the plastic strain induced per cycle (ε_{pl}) can be calculated by FEA [73]. The constants C_1 and C_2 can be obtained from stress experiments or multiple linear regressions of FEA results. However, if the wire bond is below their yield stress which is elastic regime, the lifetime prediction is usually based on Basquin's equation [74] as shown

$$N_f = C_3(\Delta\sigma)^{-C_4} \tag{9}$$

where stress range $\Delta\sigma$ is used as damage metric instead of plastic strain amplitude. The constant C_3 and C_4 also can be obtained in the same way as above. In [75], the model based on the energy density has been proposed. In this approach, it is assumed that the Al ribbon can dissipate a fixed energy value (critical accumulated energy) during its life. The N_{f} associated to a current *I* of wire bond is calculated as

$$N_{f(I)} = \frac{w_{pl}^{cr}}{w_{pl(I)}} \tag{10}$$

where $w_{pl(I)}$ is the dissipated energy density in one ribbon corresponding to the current (*I*) in a stabilized cycle. w_{pl}^{cr} is the plastic strain energy density accumulated in a ribbon during its life time.

Based on the physical approach, more complicated models can be developed which consider additional failure mechanism such as, stress relaxation, anisotropic effects, and microstructural change. However, unfortunately, the number of free parameters related to these approaches would make the calibration of those models impossible [26].

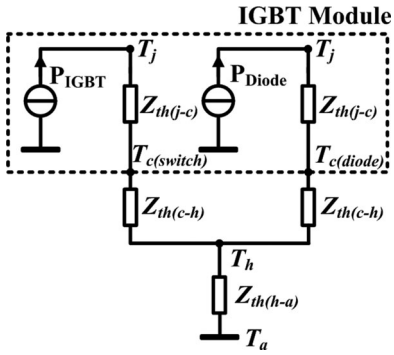

Fig. 4. Thermal equivalent block diagram of IGBT module.

B. Estimation of Internal Junction Temperature

A power semiconductor generates losses during switching and conduction of electric currents at a certain operating voltage. The energy loss in the semiconductor components is converted to heat and increases the temperature. The thermal characteristics of a power device module are typically specified with $Z_{\text{th}(j-c)}$, which is the thermal impedance between the junction and the case for the IGBT and the diode. Additionally, the interface impedance between the case and the heat sink $(Z_{\text{th}(c-h)})$ is given for each IGBT and diode.

Fig. 4 shows the thermal equivalent block diagram of the power device module with the baseplate in which the thermal impedance between the junction and the case $Z_{\text{th}(j-c)}$ and the junction and the heat sink $Z_{\text{th}(j-h)}$ can be represented by two thermal models. Using these two thermal models, the junction temperature can then be estimated.

The first model is the Cauer model shown in Fig. 5(a). It directly represents the actual physical layers and materials in the IGBT module. This model requires precise material parameters, especially parameters for thermal lateral spread effect in relevant layers. The second model is the Forster model shown in Fig. 5(b). It has no relation to the actual physical layers and materials. Hence, it is suitable for metrological determination of thermal resistance and impedance. The precise material parameters need not be known to use this model. Therefore, the Forster model

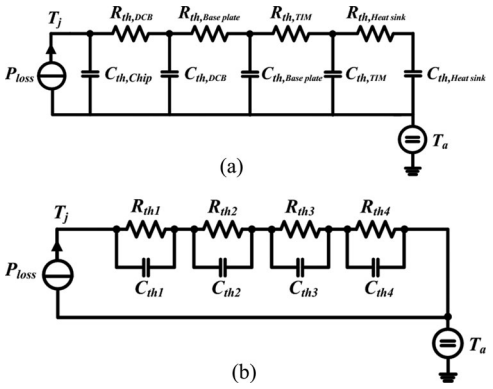

Fig. 5. Thermal models for IGBT module (a) Cauer model and (b) Forster model [27].

TABLE III
PARAMETERS FOR THERMAL MODEL OF IGBT MODULE

Thermal Impedance	Point (*i*)					
	1	2	3	4	5	6
$R_{(j-h)IGBT1}$ (K/W)	0.1	0.28	0.16	0.04	0.02	-
τ_{IGBT1} (s)	1.7	2.4 E − 1	6.7 E − 2	8.5 E − 3	5.6 E − 4	-
$R_{(j-h)Diode1}$ (K/W)	0.06	0.3	0.77	0.28	0.14	-
τ_{Diode1} (s)	3.9	3.8 e^{-1}	7.8 e^{-2}	1.2 e^{-2}	1.2 e^{-3}	
$R_{(j-h)IGBT2}$ (K/W)	0.04	0.17	0.62	0.31	0.12	0.06
τ_{IGBT2} (s)	9.0	1.1	1.7 e^{-1}	3.9 e^{-2}	6.7 e^{-3}	4.1 e^{-4}
$R_{(j-h)Diode2}$ (K/W)	0.06	0.3	0.8	0.28	0.11	0.07
τ_{Diode2} (s)	9.8	1.1	1.8 e^{-1}	3.3 e^{-2}	5.6 e^{-3}	3.8 e^{-4}

is generally used for thermal analysis [15], [27]. The transient thermal impedance $Z_{\mathrm{th}(j-c)}$ or $Z_{\mathrm{th}(j-h)}$ can be expressed as

$$Z_{\mathrm{th}(j-c)}(t) = \sum_{i=1}^{n} R_i(1 - e^{-t/\tau_i}) \tag{11}$$

where $\tau_i = R_i C_i$. The parameters in the above equation can be obtained from data sheets, FEM simulation, or experiments. Table III shows the thermal parameters of the IGBT module for the thermal model.

An FZ12NMA080SH IGBT module manufactured by Vincotech is used for junction temperature estimation case study in which IGBTs (S_1 and S_4) and diodes (D_1 and D_4) indicate the half-bridge IGBTs and diodes, respectively, and IGBTs (S_2 and S_3) and diodes (D_2 and D_3) represent the neutral-point IGBTs and diodes, respectively, as shown in Fig. 6. The heat sink temperature is set to be a constant 60 °C during inverter operation because the heat sink has the largest thermal capacitance [28].

Fig. 7(a) shows the estimated junction temperatures of the IGBTs and diodes in a T-type three-level inverter under the following conditions: $V_{\mathrm{DC}} = 650\,\mathrm{V}$; output power = 20 kW; modulation index = 0.829; and power factor = 1 (inverter operation). Fig. 7(b) shows the estimated junction temperatures

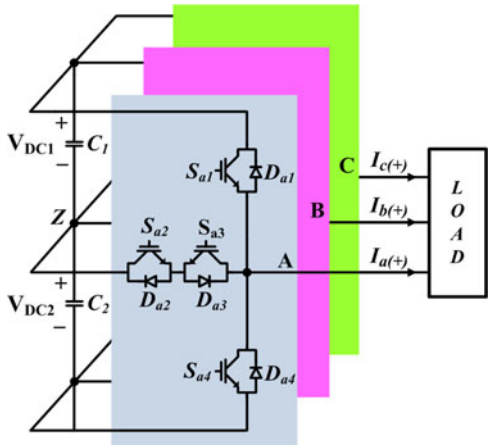

Fig. 6. Simplified circuit diagram of a T-type three-level inverter system.

of T-type modules when the power factor is −1 (converter operation).

IV. DETECTION METHODS OF POWER DEVICE FAULTS IN POWER CONVERTERS

In this section, the methods for detecting open- and short-circuit faults in power devices are introduced.

A. Open-Circuit Fault Detection Methods

Open-circuit faults mainly occur owing to the lifting of wire bond in a power module due to the thermal stresses as explained above. The gate drive faults are also one of the common causes of open-circuit faults. An open-switch fault does not cause serious damage when compared with short-circuit faults; however, it does reduce system performance. It leads to current distortion at the output and can cause secondary problems in other components through induced noise and vibrations in the load [38]. Therefore, methods for detecting open-circuit faults and fault-tolerance control strategies are required in power electronic systems.

1) Current Vector Shape Method [29]–[33]: Open-circuit faults can lead to a distortion of output phase currents due to an undesirable current path. The distortion of phase currents depends on the location of a faulty switch. Therefore, an open-circuit fault can be detected, and the location of the faulty switch can be identified from its current vector shape. A simplified circuit diagram of a two-level three-phase inverter system is shown in Fig. 8 to explain the principle of this method. The output currents can be transformed into stationary *d-q* frame currents as follows:

$$i_d^s = \frac{2}{3} i_a - \frac{1}{3} i_b - \frac{1}{3} i_c \tag{12}$$

$$i_q^s = \frac{1}{\sqrt{3}} (i_b - i_c). \tag{13}$$

The currents expressed by the above equations can be represented in the stationary *d-q* frame where the horizontal axis is denoted by i_d^s and the vertical axis is identified by i_q^s. The

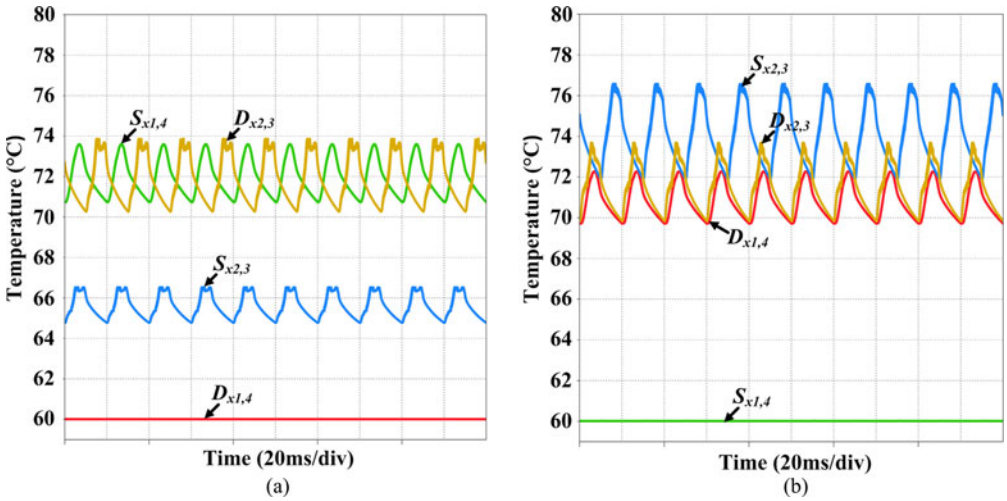

Fig. 7. Estimated junction temperatures at 20 kW load for (a) inverter $(PF = 1)$ and (b) converter $(PF = -1)$ [67].

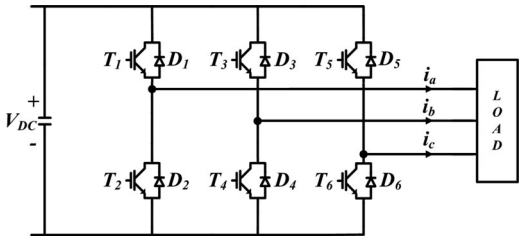

Fig. 8. Simplified circuit diagram of a two-level three-phase power converter system.

TABLE IV
ANGLES OF CURRENT VECTORS DEPENDING ON THE FAULTY SWITCH

Switch	Θ
T_1	150° ∼ 210°
T_2	330° ∼ 30°
T_3	270° ∼ 330°
T_4	90° ∼ 150°
T_5	30° ∼ 90°
T_6	210° ∼ 270°

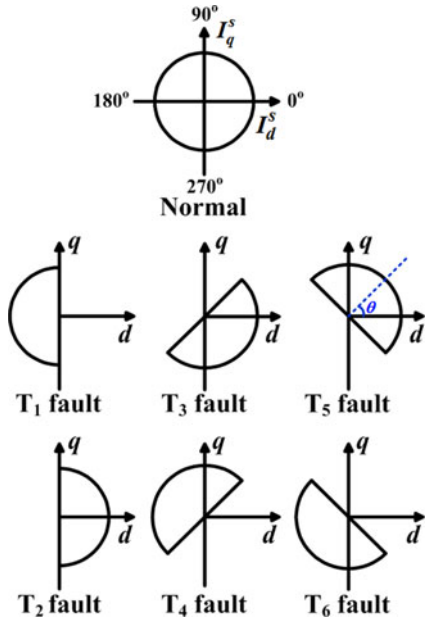

Fig. 9. Current patterns in a *d*-*q* frame according to the faulty switch.

current vectors in this frame have a specific shape and angle depending on the faulty switch as shown in Fig. 8. Therefore, the variations in the shape and angle of the current vector indicate the occurrence of an open-circuit fault condition and can indicate the location of the faulty switch, as shown in Table IV. The center of the current vector is considered for the angle of current vector. For example, a fault in T_5 as shown in Fig. 9, the angle of current pattern under T_5 fault is in the range of 30° to 90°.

2) Direct Average Current Method [34], [35]: This method directly uses the average three-phase currents calculated as

$$I_{x\_\mathrm{avg}\,(x=a,b,c)} = \frac{1}{N}\sum_{i=k-N+1}^{k} I_x(i). \tag{14}$$

Under normal operating conditions, the average of phase currents during a fundamental cycle is zero. However, if an open-switch fault occurs, the average of phase currents can be positive or negative value depending on the distortion of the phase current. Fig. 10(a) and (b) shows the distortion of output phase currents, when an open-circuit fault occurs in switches T_1 and T_2, respectively. The positive or negative phase current of a faulty phase does not flow; thus, the average of currents becomes a positive or negative value. The polarity of the average output current is determined by comparing with a threshold value I_{thr}, and the faulty switch location can then be identified. However, this method tends to be highly unreliable under varying operating conditions, especially during fast transient conditions, and causes of the false alarms. The identification of the faulty switch by comparing the average current with a threshold value is shown in Table V.

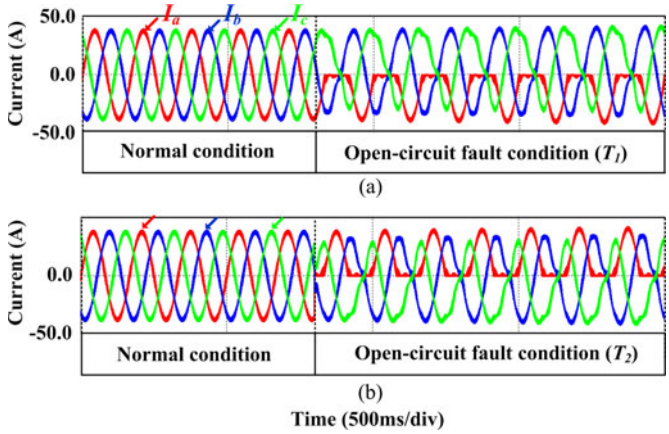

Fig. 10. Distortions of output currents under (a) T_1 and (b) T_2 faults.

TABLE V
FAULTY SWITCH IDENTIFICATION USING DIRECT AVERAGE CURRENT METHOD

Switch	$I_{a\,\mathrm{avg}}$	$I_{b\,\mathrm{avg}}$	$I_{c\,\mathrm{avg}}$
T_1	$<-I_{\mathrm{thr}}$		
T_3		$<-I_{\mathrm{thr}}$	
T_5			$<-I_{\mathrm{thr}}$
T_2	$>I_{\mathrm{thr}}$		
T_4		$>I_{\mathrm{thr}}$	
T_6			$>I_{\mathrm{thr}}$

3) Modified Normalized Average Current Method [34]–[36]: The direct average current method can be unreliable and may cause false alarms. Therefore, to avoid false alarms and improve accuracy, the normalized average current method is proposed. The normalized average current is calculated as

$$\gamma_{x\,(x=a,b,c)} = \frac{I_{x\_\mathrm{avg}}}{\sqrt{a_{1x}^2 + b_{1x}^2}} \tag{15}$$

$$a_{1x\,(x=a,b,c)} = \frac{2}{N}\sum_{K=1}^{N} I_x(k\tau)\cos\left(\frac{2\pi k}{N}\right) \tag{16}$$

$$b_{1x\,(x=a,b,c)} = \frac{2}{N}\sum_{K=1}^{N} I_x(k\tau)\sin\left(\frac{2\pi k}{N}\right) \tag{17}$$

where a_{1x} and b_{1x} are the first-order harmonic coefficients of the inverter ac currents

$$d_{1x\,(x=a,b,c)} = \begin{cases} 1, & \gamma_x > 0 \\ 0, & \gamma_x \le 0 \end{cases} \tag{18}$$

$$d_{2x\,(x=a,b,c)} = \begin{cases} 1, & |\gamma_x| > 0.45 \\ 0, & |\gamma_x| \le 0.45 \end{cases}. \tag{19}$$

For identifying the faulty switch, the largest absolute value of γ_a, γ_b, and γ_c is compared with the thresholds given in (18) and (19). The faulty switch can then be identified using Table VI. A threshold of 0.45 is considered to be a universal value from experience.

4) Slope of Trajectory of Space Vector Method [33], [37]: The slope ψ of the diameter of current space vector trajectory can be also considered to be an indicator for open-circuit fault detection. The slope is defined as

$$\psi = \frac{i_{dk}^s - i_{d(k-1)}^s}{i_{qk}^s - i_{q(k-1)}^s} \tag{20}$$

where i_{dk}^s and i_{qk}^s are the sampled currents transformed into a stationary reference frame. Under normal conditions, ψ always varies because the current vector trajectory is a circle. If an open-circuit fault occurs, the value of slope depends on faulty phase. However, only the faulty phase can be identified using the slope value. To identify the faulty switch in the faulty phase, the polarity of the phase current must also be determined. A positive faulty phase current indicates an open-circuit fault in the lower switch. Conversely, negative faulty phase current indicates an open-circuit fault in the upper switch. The faulty switch detection method based on the slope of the current vector trajectory and polarity of the phase current is shown in Table VII. Numerous improved methods based on the slope of phase current have recently been proposed for open-fault detection in [42] and [43].

5) Method Based on Switching Function Model [38]: The relationship between the collector–emitter voltage of the IGBTs and the binary variables can be given by (21) under the assumption that the power switches are ideal and ignoring the dead-time effect

$$\begin{cases} V_{\mathrm{T1}} = (1 - S_{a+})V_{\mathrm{DC}} \\ V_{\mathrm{T2}} = S_{a-}V_{\mathrm{DC}} \\ V_{\mathrm{T3}} = (1 - S_{b+})V_{\mathrm{DC}} \\ V_{\mathrm{T4}} = S_{b-}V_{DC} \\ V_{\mathrm{T5}} = (1 - S_{c+})V_{\mathrm{DC}} \\ V_{T6} = S_{c-}V_{\mathrm{DC}} \end{cases} \tag{21}$$

where V_{DC} is the dc-link voltage, and S_a to S_c are the switching functions representing the switching states and are set to be 1 or

TABLE VI
FAULTY SWITCH IDENTIFICATION USING MODIFIED NORMALIZED AVERAGE CURRENT METHOD

Switch	d_{1a}	d_{1b}	d_{1c}	d_{2a}	d_{2b}	d_{2c}
T_1	0			1		
T_3		0			1	
T_5			0			1
T_2	1			1		
T_4		1			1	
T_6			1			1

TABLE VII
FAULTY SWITCH IDENTIFICATION USING A SLOPE METHOD

Faulty Switch	Slope ψ	Polarity of Current in Faulty Phase
T_1	0	$-$
T_2	0	$+$
T_3	$\sqrt{3}$	$-$
T_4	$\sqrt{3}$	$+$
T_5	$-\sqrt{3}$	$-$
T_6	$-\sqrt{3}$	$+$

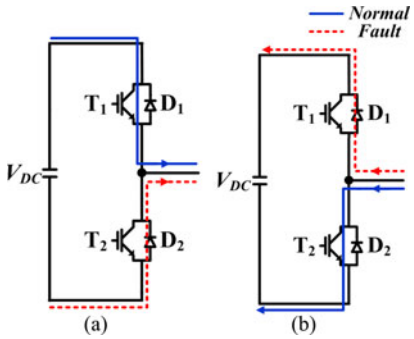

Fig. 11. Current paths under (a) T_1 fault condition when $S_{a+} = 1, S_{a-} = 0$ and (b) T_2 fault condition when $S_{a+} = 0, S_{a-} = 1$.

TABLE VIII
COMPARISON OF COLLECTOR–EMITTER VOLTAGES UNDER OPEN-SWITCH FAULT T_1

I_a	S_{a+}	S_{a-}	Normal		T_1 Fault Condition	
			V_{T1}	V_{T2}	V'_{T1}	V'_{T2}
+	**1**	**0**	**0**	V_{DC}	$V_{DC}{}'$	**0**
+	0	0	V_{DC}	0	V_{DC}	0
+	0	1	V_{DC}	0	V_{DC}	0
−	1	0	0	V_{DC}	0	V_{DC}
−	0	0	0	V_{DC}	0	V_{DC}
−	0	1	V_{DC}	0	V_{DC}	0

0 when the switch is closed, respectively. Further, V_{T1} to V_{T6} indicate the collector–emitter voltages of the six IGBTs. This method is explained further considering phase *A* fault.

a) Open-switch fault in upper switch: Fig. 11(a) shows the change of current path under T_1 fault condition. If the current is positive under open-circuit fault T_1, the current flows through D_2 instead of T_1 under upper switching signal mode ($S_{a+} = 1, S_{a-} = 0$). In this case, T_1 endures V_{DC} and the voltage of T_2 is null, which is in contrast to the voltages calculated using the switching function model in (21). Therefore, the open-circuit fault T_1 can be detected from the voltage difference between the actual collector–emitter voltage values (V_{T1} and V_{T2}) and the calculated voltage values (V'_{T1} and V'_{T2}). A comparison of the collector–emitter voltages under fault T_1 is given in Table VIII.

b) Open-circuit fault in lower switch: The principle for fault detection by comparing the collector–emitter voltages is same as discussed above. In the T_2 open-circuit fault case, the actual collector–emitter voltages of switches are different from the calculated values when $S_{a+} = 0, S_{a-} = 1$ and the output current is negative. In this case, the current flows through D_1 instead of T_2, as shown in Fig. 11(b). Therefore, V_{T1} and V_{T2} become zero and V_{DC}, respectively, instead of V_{DC} and zero. A comparison of the collector–emitter voltages of different switching states is shown in Table IX.

6) Lower-Switch Voltage Measurement Method [39]: The voltage across the lower switch is V_{DC} or 0 and changes complementarily according to its state under normal operating conditions. However, under the open-circuit fault condition, the voltage across the lower switch in the faulty phase is $(1/2)V_{DC}$

TABLE IX
COMPARISON OF COLLECTOR–EMITTER VOLTAGES UNDER OPEN-SWITCH FAULT T_2

I_a	S_{a+}	S_{a-}	Normal		T_2 Fault Condition	
			V_{T1}	V_{T2}	V'_{T1}	V'_{T2}
+	1	0	0	V_{DC}	0	V_{DC}
+	0	0	V_{DC}	0	V_{DC}	0
+	0	1	0	V_{DC}	0	V_{DC}
−	1	0	0	V_{DC}	0	V_{DC}
−	0	0	0	V_{DC}	0	V_{DC}
−	**0**	**1**	V_{DC}	**0**	**0**	V_{DC}

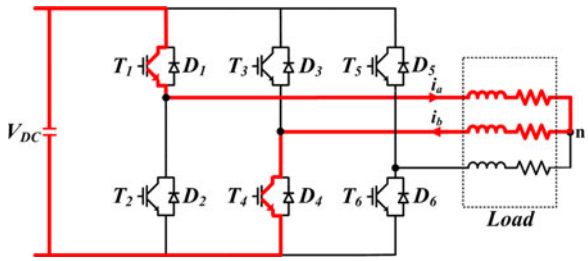

Fig. 12. Operation of inverter under T_6 fault when the switching state is [100].

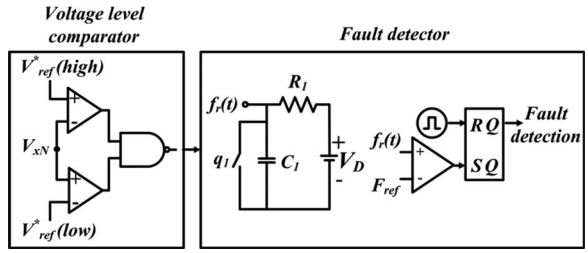

Fig. 13. Lower-switch voltage measuring method procedure for the fault detection [39].

under either the upper or lower switch fault. For example, in the case of T_6 open-circuit fault, the voltage across T_6 becomes $(1/2)V_{DC}$ when the switching state of the inverter is [1 0 0], because the current does not flow, as shown in Fig. 12. The switching state [1 0 0] indicates that T_1, T_4, and T_6 are ON and T_2, T_3, and T_5 are OFF. The measured voltages are compared with the reference voltage using an op-amp-based voltage level comparator. The comparator output is applied to the gate of switch q_1. The middle voltage ($(1/2)V_{DC}$) detected by the comparator is changed to function $f_r(t)$, which is a ramp function that increases according to the middle voltage level width and is calculated as

$$f_r(t) = q_1 V_D \left(1 - e^{\frac{-t}{R_1 C_1}}\right) \tag{22}$$

where q_1 is the switching function, and $f_r(t)$ is compared with the threshold value F_{ref} to detect the fault. Fig. 13 shows the fault detection algorithm based on the lower-switch voltage. If $f_r(t)$ is less than F_{ref}, the system is considered to be under normal condition. If $f_r(t)$ is greater than F_{ref}, a fault signal is produced. The fault is detected with a set signal of the flip flop.

TABLE X
COMPARISON OF INTRODUCED OPEN-CIRCUIT FAULT DETECTION METHODS

Methods	Effectiveness	Diagnosis Time	Considered Parameters	Implementation Effort	Tuning Effort	Additional Hardware
Current vector shape method [29]–[33]	Poor at small current	Within 2 fundamental periods	3-phase currents	Low	Medium	Not required
Slope of space vector's trajectory method [33], [37]	Poor at small current	Average 2 fundamental periods	3-phase currents	Low	High	Not required
Direct average current method [34], [35]	Poor at small current	Within 1.5 fundamental periods	3-phase currents	Low	Medium	Not required
Modified normalized average current method [34], [36]	Good	Within 1.5 fundamental periods	3-phase currents	Low	Low	Not required
Method based on switching function model [38]	Good	Fast but not defined	Switch voltage, and signal	Medium	Low	Required
Lower-switch voltage measuring method [39]	Good but the location cannot be identified	Approximately 2.7 ms	Lower-switch voltage	Medium	Low	Required

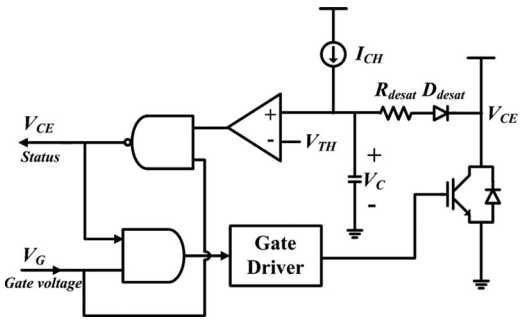

Fig. 14. Example circuit for desaturation detection method for short-circuit detection [46].

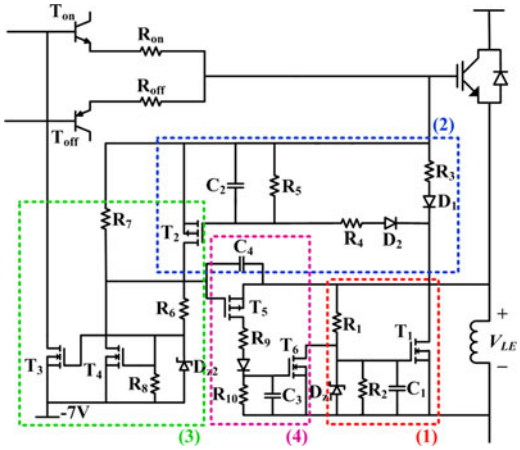

Fig. 15. Fault detection circuit based on *di/dt* feedback control method [47].

Fault detection methods are typically specialized for different applications. Therefore, the above methods are not applicable to certain applications, such as grid-connected NPC inverter systems [40], because the distortion of output phase currents is the same under both upper or both lower switches. Namely, the fault switch cannot be pinpointed using the methods based on current distortion. For identifying the faulty switch in these cases, a method using an additional simple switching control has been proposed in [40]. Open-circuit fault detection methods for T-type inverter and NPC converter have also been proposed in [41] and [71].

A comparison of the introduced open-circuit fault detection methods is shown in Table X.

B. Short-Circuit Fault Detection Methods

Short-circuit faults can occur because of numerous reasons such as incorrect gate voltage, overvoltage, avalanche stress, or temperature overshoot. Short-circuit faults cannot be easily handled because they lead to an abnormal over current that can cause serious damage to other components in a short time. Therefore, most of the short-circuit fault detection and protection methods are based on hardware circuits in order to be fast enough [64].

1) Desaturation Detection Method [44]–[46]: Fig. 14 shows an example circuit for desaturation detection method. If the switch is turned ON, the current source in the protection circuit provides a small charge current $(I_{\rm CH})$. The capacitance voltage (V_C) increases, and the sensing diode $(D_{\rm clamp})$ is then forward biased. Under normal operating conditions, (V_C) is very small because the on-state collector–emitter voltage $(V_{\rm CE\_ON})$ is also very small. However, if a short-circuit fault occurs, $V_{\rm CE\_ON}$ increases significantly owing to the large current, thus leading to the increase in V_C. The protection circuit determines whether a fault has occurred by comparing V_C with threshold value $(V_{\rm TH})$, which is typically 7 V. If V_C reaches the threshold value, the protection circuit generates a control signal to suppress the gate on pulses. This method requires only a simple circuit. However, it is not suitable for high-speed IGBT switching because it requires a blanking time of approximately 1 to 5 μs. Blanking time is the taken time to charge the capacitor by the internal charge current $(I_{\rm CH})$, and it can reject the noise from normal switching behaviors. Moreover, the dynamic feedback information is not provided.

2) di/dt Feedback Control Method [47], [48], [66]: In this method, the voltage across the stray inductance (L_E) between the Kelvin emitter and the power emitter as shown in Fig. 15 is measured to detect short-circuit faults. The voltage across the inductor is expressed as

$$V_{LE} = L_E \frac{di}{dt}. \tag{23}$$

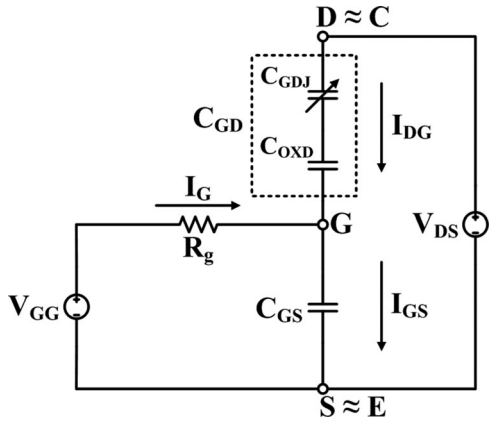

Fig. 16. IGBT equivalent circuit seen from gate (G) to emitter (E) [50].

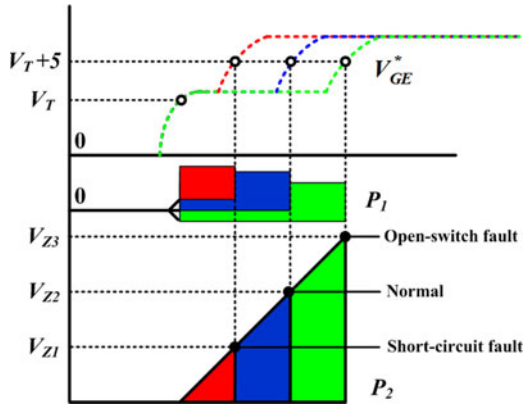

Fig. 17. Variation in V_{GE} during turn-on and fault detection by P_1 width and P_2 amplitude [50].

This measured voltage that reflects the current is compared with the preset threshold value to determine whether a short-circuit fault has occurred. If a fault is detected, *di/dt* shutdown control is activated to limit the fault current to a safe level, and the gate signal is disabled. Finally, a slow turn-off mechanism is applied to reduce the voltage overshoot due to the effect of power-loop stray inductance and high *di/dt* under short-circuit condition. This method does not require any blanking time. Therefore, it dynamically responds to a fault condition after a fault is detected. However, this method requires additional complex circuitry.

Fig. 15 shows a sample of a fault diagnosis circuit based on the *di/dt* feedback control method. This circuit provides four functions which are indicated as shown in Fig. 15:

1) *di/dt* dynamic control **(1)**;
2) *di/dt* control sensing and hold **(2)**;
3) Command disable, IGBT slow turn-off, *di/dt* shutdown enable **(3)**;
4) *di/dt* control shutdown **(4)**.

Recently, another circuit based on *di/dt* feedback has been proposed in [66].

3) Gate Voltage Monitoring Method [49], [50]: The region between the gate and drain of an IGBT can be modeled by C_{GD}. Further, C_{GD} consists of a variable capacitance C_{GDJ}, which models the depletion zone, and a fixed capacitance C_{OXD}, which models the oxide zone. Fig. 16 shows a simplified circuit seen from the gate to the emitter. The variable capacitance C_{GDJ} can be defined as

$$C_{\mathrm{GDJ}} = A_{\mathrm{GD}} \sqrt{\left(\frac{q \cdot N_B \cdot \varepsilon_{si}}{2(V_{\mathrm{DS}} - V_{\mathrm{GS}})} \right)} \tag{24}$$

where N_B is the *n*-layer doping concentration, and q is the electron charge. In the above expression, a variation in different parameters such as gate–drain area (A_{GD}) and dielectric constant (ε_{si}) significantly affects C_{GDJ}. A variation in these parameters can cause destructive effects in IGBTs. A variation in C_{GDJ} also causes a change in C_{GD} because C_{GD} can be expressed by the transient behavior of V_{DS} and V_{GS} when the

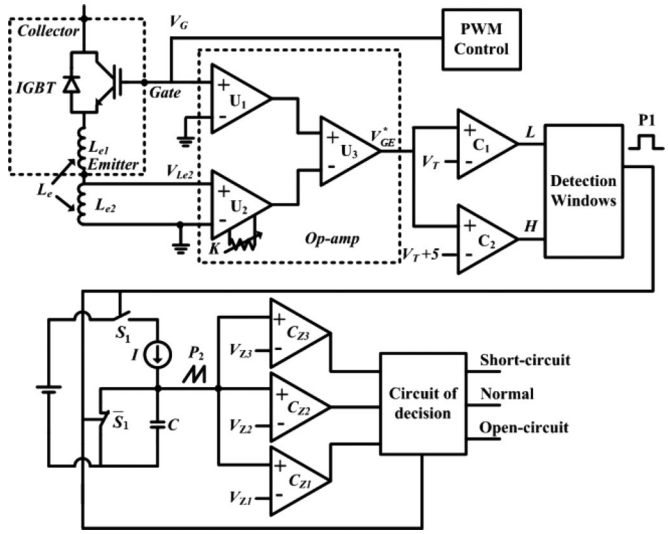

Fig. 18. Circuit for gate voltage sensing and fault detection [50].

IGBT is turned ON $(V_{\mathrm{DS}} > V_{\mathrm{GS}})$

$$C_{\mathrm{GD}} = \frac{C_{\mathrm{OXD}} \cdot C_{\mathrm{GDJ}}}{C_{\mathrm{OXD}} + C_{\mathrm{GDJ}}} \ (V_{\mathrm{DS}} > V_{\mathrm{GS}}). \tag{25}$$

The variation in C_{GD} directly affects the gate current and leads to a significant variation in the gate voltage, as shown in Fig. 17. The short- and open-circuit faults increase and decrease C_{GDJ}, respectively. Therefore, the variations in the gate voltage characteristics during the turn-on transient can be used to identify a faulty condition. Fig. 18 shows the circuit for fault detection. The detection-circuit design is based on the measurement of the gate signal. The principle of the design involves measuring the energy of the IGBT gate charge from V_T up to $V_T + 5\,V$, when it is turned ON. According to the condition, the measurement circuit generates different durations of the output signal P_1, thus generating different amplitudes of P_2. By comparing the value of P_2 with the thresholds V_{Z1}, V_{Z2}, and V_{Z3}, the faults of the IGBT can be determined. Fig. 17 shows the fault determination using P_1 width and P_2 amplitude. The principle

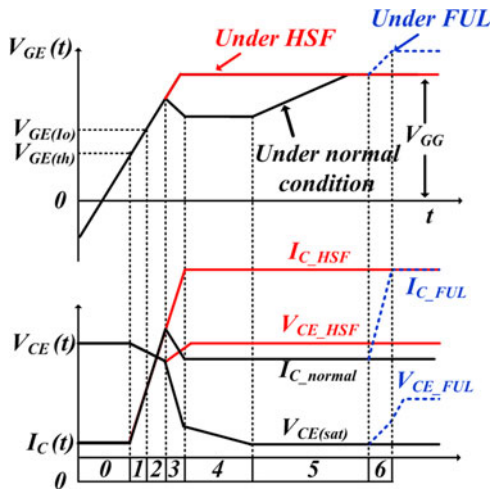

Fig. 19. Turn-on characteristics of IGBT under normal and HSL conditions (red: fault; black: normal) [72].

of this method is simple; however, it requires a complicated circuitry for sensing gate voltage and detecting faults.

4) Gate Voltage Comparison Method [51], [65], [72]: The short-circuit faults of an IGBT can be classified into two cases depending on the faulty conditions. The first is the fault under load (FUL) that occurs when a short-circuit current is applied when the IGBT is in the on-state. The second is hard switching fault (HSF) that occurs when a device is turned ON under short-circuit fault condition. Under the short-circuit fault condition, the characteristics of gate voltage $V_{\rm GE}$ differ from those under normal condition. Therefore, the short-circuit fault can be detected by comparing the gate input voltage $V_{\rm GG}$ and gate voltage $V_{\rm GE}$. Fig. 19 shows the turn-on switching characteristics of the IGBT under different conditions (normal, FUL, and HSF). Here, $V_{\rm GE}$ is kept constant because of the Miller effect in *region3* $\sim$ *region4* in Fig. 19 and this value is smaller than $V_{\rm GG}$ under normal condition. However, under the HSF condition, $V_{\rm GE}$ increases until $V_{\rm GG}$ in *region3* $\sim$ *region4* because Miller effect is low swing to the small variation in $V_{\rm CE}$. In the case of FUL, a large shoot-through current is produced when the opposite side of IGBT is turned ON under short-circuit fault condition. The current I_C increases rapidly, and the IGBT enters the active region. Further, $V_{\rm CE}$ increases, and $V_{\rm GE}$ can increase above $V_{\rm GG}$, as shown in Fig. 18. Consequently, the short-circuit fault can be detected by comparing $V_{\rm GG}$ and $V_{\rm GE}$. Fig. 20 shows an example of a fault diagnosis circuit for the gate voltage comparison method.

5) Current Mirror Method [47]: In this method, a collector current is sensed using a current mirror circuit by integrating a second IGBT with the main IGBT. The second IGBT carries a scaled-down current of the main IGBT, which is also referred to as a mirror current. This current, through a known resistor, can also be used for fault-current detection by measuring the voltage drop across the known resistor created by the mirror current. This method is simple to implement; however, it is expensive because a special design is required at the semiconductor level in the devices containing a current mirror circuit.

6) Protection With Snubber and Clamp Circuit [52]: Fig. 21 shows a voltage clamp circuit used for protecting IGBTs. If the IGBT is turned OFF, the collector–emitter voltage $(V_{\rm CE})$ increases rapidly and can increase above the bus voltage because of the circuit dc loop stray inductance (L_S). The snubber diode is then forward biased, and the snubber is activated. The energy trapped in the stray inductance is diverted to the snubber capacitor, which absorbs this incremental energy without a substantial increase in its voltage. Hence, the voltage overshoot due to the stray inductance can be reduced substantially. Further, this circuit also suppresses the overshoot voltage when the IGBT is turned ON. However, these circuits are not efficient for protection against turn-off transients caused by rapid suppression of gate drive because they require high-capacity, high-voltage snubber capacitors that are bulky and expensive [44].

7) Protection by Slow Turn-Off of IGBT [52]: If the IGBT is turned OFF rapidly to prevent the short-circuit current from flowing, high-voltage overshoot can be generated owing to extremely high *di/dt* with stray inductance. This overshoot voltage causes an IGBT failure and can be reduced by slowing the turn-off time. Therefore, two novel circuits are proposed to reduce the $V_{\rm GE}$ drop rate when a fault current is sensed.

a) Resistive method: Fig. 22 shows that the fault-protection circuit is consists of a desaturation sensing diode D_1 and a P-channel MOSFET to switch the gate resistor with higher value by adding the resistor R_{g2} when a short-circuit fault occurs. If a short-circuit fault occurs, D_1 is reverse biased, and the P-MOSFET input starts to discharge through R_1 and R_2. The MOSFET is then turned-off because its gate voltage drops below the threshold value. The $V_{\rm GE}$ fall rate reduces significantly because the discharge occurs through R_{g2}. Consequently, the fault current fall rate also decreases.

b) Capacitive method: Fig. 23 shows the fault-protection circuit using the capacitive method. It also comprises the desaturation diode D_1 for short-circuit fault detection and an N-channel MOSFET to increase the total input capacitance by connecting the higher value of the capacitor C_1 in parallel to the IGBT input capacitance. If a short-circuit fault occurs, D_1 is reverse biased, and the N-channel MOSFET gate input capacitance is charged by the gate driver voltage. If the MOSFET is turned ON, C_1 is connected in parallel to the IGBT input capacitor. Hence, the total input capacitance of the IGBT is raised, thus increasing the IGBT discharge time constant. Therefore, the fault current *di/dt* decreases, and the transient voltage substantially reduced.

Table XI shows a comparison of the proposed short-circuit fault detection and protection methods.

V. Fault-Tolerant Strategy

Fault-tolerance controls are essential in renewable energy systems for maintaining operation under faulty conditions to ensure high availability. Fault-tolerant topologies typically require additional components in the form of silicon switches and/or fuses to provide continuous operation and minimize the effects of faults.

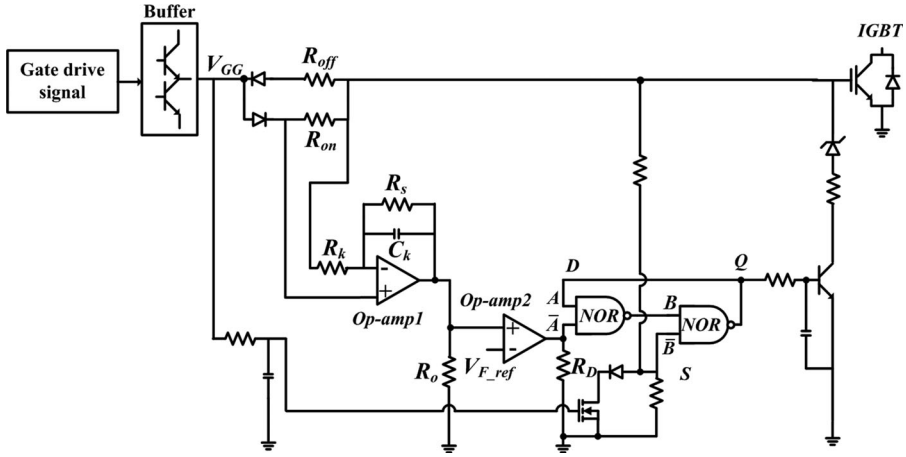

Fig. 20. Fault diagnosis circuit for gate voltage comparison method [72].

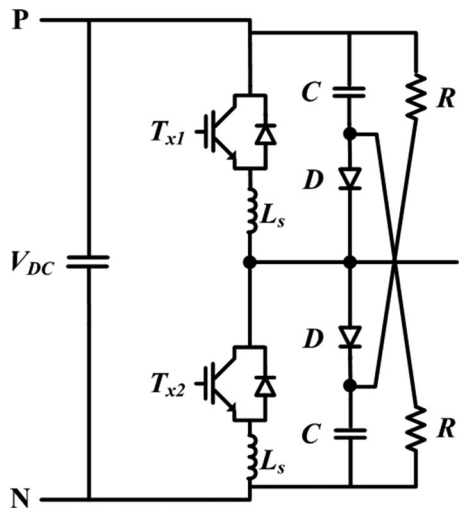

Fig. 21. RCD voltage clamp for IGBT protection [52].

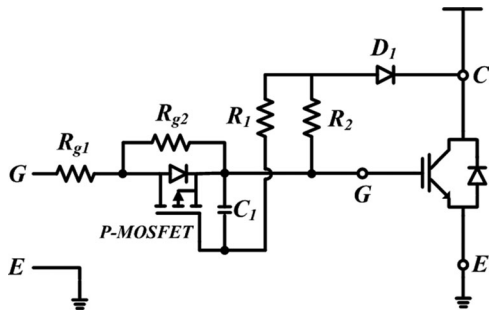

Fig. 22. Circuit for the resistive short-circuit protection method [52].

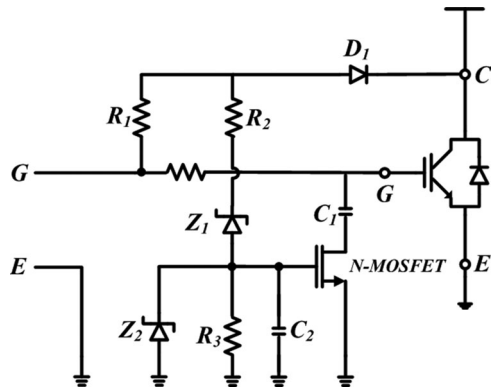

Fig. 23. Circuit for a capacitive short circuit protection method [52].

A. Switch-Redundant Topology [53]–[56]

This topology consists of a conventional inverter, three TRIACs, and six fast-acting fuses. The dc-link capacitor is split into two capacitors to provide a point [O], as shown in Fig. 24. For open faults, only the TRIACs are needed in the topology [Fig. 24(a)]. If an open-switch fault occurs, the faulty leg is connected to point [O] by the TRIAC. In the case of short-circuit faults, additional fast fuses are required. If a short-circuit fault occurs, the fuses in the faulty leg are triggered and the faulty leg is connected to point [O] by the TRIAC. If a fault occurs in this configuration, the topology is reduced to a four-switch three-phase inverter, as shown in Fig. 24(b) and can be operated as explained in [54].

If one of the phases of the load is connected to the dc-link midpoint [O], the SVM technique must be altered during the faulty condition to allow continuous drive operation. Under normal conditions, the dwell time is given by

$$v^*_{xn\_\mathrm{ref}} = v^*_{x\_\mathrm{ref}} + v_{sn} \tag{26}$$

$$T_{x(x=a,b,c)} = \left(\frac{1}{2} + \frac{v^*_{xn\_\mathrm{ref}}}{V_{\mathrm{DC}}}\right) T_{\mathrm{samp}} \tag{27}$$

where V_{DC} is the dc-link voltage, and T_{samp} is the sampling period. Further, v_{sn} is the third harmonic offset voltage, and $v^*_{xn\_\mathrm{ref}}$ is the reference voltage for SVM. Assuming that a fault occurs in T_1, the inverter leg A is isolated, and the TRIAC t_{r1} is triggered, thus resulting in $v_a = 0$. The other reference pole voltages are redefined as

$$v^*_{bn\_\mathrm{ref}} = v^*_{b\_\mathrm{ref}} - v^*_{a\_\mathrm{ref}} \tag{28}$$

TABLE XI
COMPARISON OF SHORT-CIRCUIT FAULT DETECTION METHODS

Method	Reliability	Considered Parameters	Implementation Effort	Turn-Off	Remarks
Desaturation detection method [44]–[46]	Medium	Collector voltage	Low	Abrupt	Device turn-off not assured
di/dt feedback control method [47], [48], [66]	Medium	Device current	High	Soft	Stray inductance difficult to control
Gate voltage monitoring method [49], [50]	Low	Gate voltage	Low	Abrupt	Requires complex circuitry
Gate voltage comparison method [51], [65], [72]	Low	Gate voltage	Low	Soft	Requires complex circuitry
Current mirror method [47]	Medium	Device current	Low	Abrupt	Expensive
Protection using snubber and clamped circuit [52]	Low	Device voltage	High	N/A	Expensive
Protection by slow turn-off of IGBT [52]	Low	Gate voltage	High	Soft	Requires complex circuitry

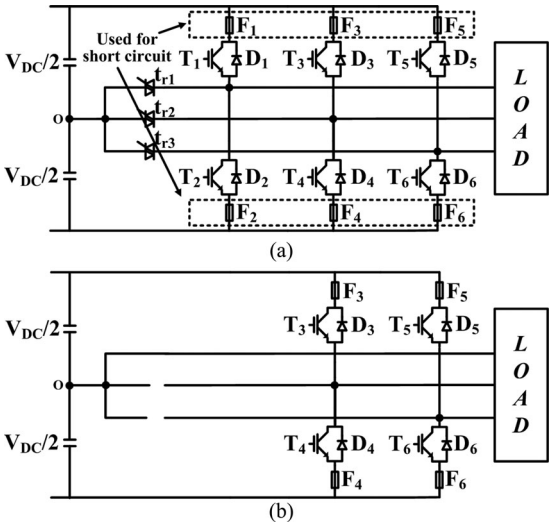

Fig. 24. Switch-redundant topology (a) under normal operation and (b) when fault occurs in leg A [54].

$$v^*_{cn\_\mathrm{ref}} = v^*_{c\_\mathrm{ref}} - v^*_{a\_\mathrm{ref}}. \tag{29}$$

For the case in which the inverter leg B is isolated

$$v^*_{an\_\mathrm{ref}} = v^*_{a\_\mathrm{ref}} - v^*_{b\_\mathrm{ref}} \tag{30}$$

$$v^*_{cn\_\mathrm{ref}} = v^*_{c\_\mathrm{ref}} - v^*_{b\_\mathrm{ref}}. \tag{31}$$

Similarly, when the inverter leg C is isolated

$$v^*_{an\_\mathrm{ref}} = v^*_{a\_\mathrm{ref}} - v^*_{c\_\mathrm{ref}} \tag{32}$$

$$v^*_{bn\_\mathrm{ref}} = v^*_{b\_\mathrm{ref}} - v^*_{c\_\mathrm{ref}}. \tag{33}$$

Depending on the isolated faulty leg, only one set of modified reference voltages must be used to accomplish balanced operation after a fault occurs. Using the modified reference pole voltage, the dwell time is then recalculated using (27).

B. Neutral Leg Topology [56]–[58]

This topology is also referred to as double switch-redundant topology and is shown in Fig. 25. It consists of a four-leg inverter with additional components, including two fuses and two SCRs per leg, for achieving fault tolerance. A pair of capacitors is also required to clear the fuses and isolate the faulty leg. If a fault occurs in leg A, SCRs Sc_1 and Sc_2 are turned ON after detection. The fuse is cleared using C_1, and the faulty leg is isolated from the system. The double switch-redundant topology fault-tolerance strategy is identical to that of the switch-redundant topology in terms of commanded currents. They differ in the way that neutral point of the motor is connected to a fourth leg. This concept has two significant purposes. First, the system is free of the dc-midpoint balancing problem. Second, it enables the control method of shifting the voltage at the neutral point of the machine, which can be applied to a three-phase system when one phase is open.

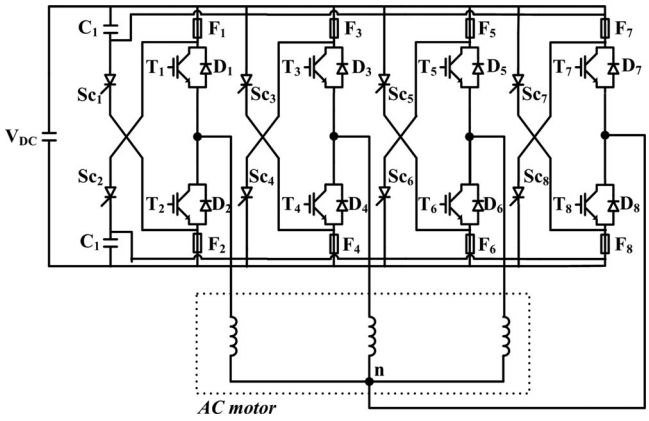

Fig. 25. Neutral leg topology with a standard three-phase motor [56].

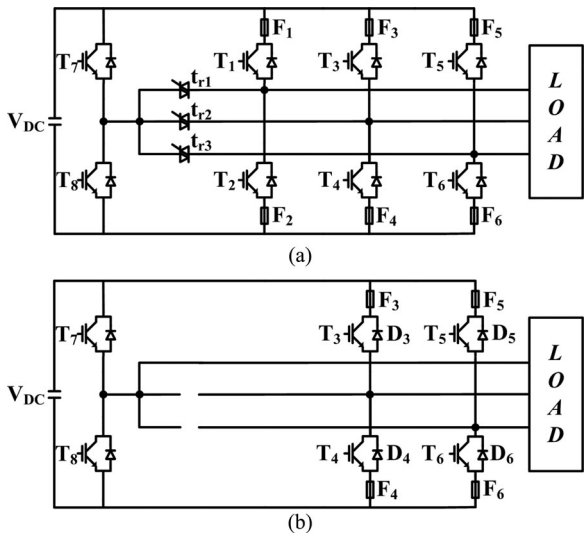

Fig. 26. Additional phase leg topology under (a) normal operation and (b) fault occurs in leg A [54].

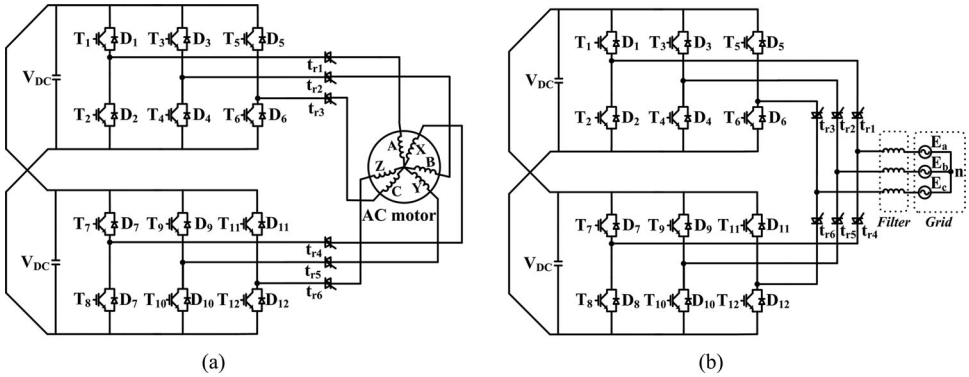

Fig. 27. Cascaded inverter topology for (a) AC motor and (b) grid-connected system.

TABLE XII
COMPARISON OF INTRODUCED FAULT-TOLERANT TOPOLOGIES IN THREE-PHASE CONVERTER

Topology	Fuse	Capacitor	IGBT	SCR	TRIAC	PFPF	CF	Fault Tolerance				Application	
								1 Switch Short	Phase-Leg Short	1 Switch Open	Phase-Leg Open	Grid-Connected	Motor (Generator)
Standard (see Fig. 8)	0	1	6	0	0	0	1	X	X	X	X	X	X
Switch-redundant for open fault (see Fig. 24) [53]–[56]	0	2	6	0	3	0.5	1.47	X	X	O	O	X	O
Switch-redundant (see Fig. 24) [53]–[56]	6	2	6	0	3	0.5	1.82	O	O	O	O	X	O
Neutral-leg (see Fig. 25) [56]–[58]	8	1	8	8	0	0.58	2.64	O	O	O	O	X	O
Additional phase leg (see Fig. 26) [57]–[61]	6	1	8	0	3	1.0	1.94	O	O	O	O	O	O
Cascaded inverter (see Fig. 27) [62]–[64]	0	2	12	0	3	0.58 (1.0)	1.76 (2.35)	O	X	O	O	O	O

C. Additional Phase Leg Topology [57]–[61]

The four-leg inverter topology is shown in Fig. 26(a). It requires two additional IGBTs, three TRIACs, and six fast-acting fuses. Under normal operation, the fourth leg is not used. If an open-switch fault occurs, the faulty leg is isolated by a TRIAC. If an open-circuit fault occurs in leg A, the TRIAC t_{r1} is triggered to replace A with the fourth leg. If a short-circuit fault occurs in one of the switches of leg A, the complementary switch turns ON to blow fuses F_1 and F_2. The requirement for selecting the power device is that the integral current square $\int i^2 t$ of the fuses must be less than the tolerable value of the power switch. Because the faulty leg is replaced by the fourth leg, it must be controlled as if it were the isolated faulty leg. Therefore, SVM modification is not required. Fig. 26(b) shows the four-leg inverter circuit after a fault has occurred in leg A.

D. Cascaded Inverter Topology [62]–[64]

Fig. 27(a) shows a cascaded inverter topology. This topology consists of a dual-winding three-phase AC motor with each winding set connected to a normal three-leg inverter delivering 50% of the rated power under normal operation. If a fault occurs in one of the inverters, the other inverter delivers 50% of the rated power under the fault condition. The faulty inverter is isolated by the TRIACs in series with the motor. Fig. 27(b) shows the cascaded inverter topology when it is applied to a grid-connected system. Under normal operation, this topology can be made to operate as a two-, three-, or four-level inverter depending on the dc-link voltage [62]. If a fault occurs, the inverter containing the faulty switch is isolated from the system by the TRIACs. This topology consists of 12 IGBTs, two dc-link capacitors, and six TRIACs. Because the inverter delivers 50% of the rated power during normal operation, the costs of the IGBT and capacitor can be reduced. If an application requires rated power under fault, then each inverter must be designed for the rated power. The total cost of the cascaded inverter topology increases in comparison with standard inverter topology because of the doubled number of components required.

In addition to above methods, numerous fault-tolerant control strategies have been proposed for specific applications in [67]–[70], [76]. Some multilevel inverters and matrix inverters have inherent fault tolerant capability. Therefore, the continuous operation can be possible without additional components.

Table XII shows a comparison of the introduced fault-tolerance topologies. To quantify the output capacity of each system under a fault, a postfault performance factor (PFPF) has

been defined as

$$\text{PFPF} = \frac{\text{Postfault inverter output}}{\text{Rated output power of the standard}}. \quad (34)$$

To compare the costs associated with the additional components for the different fault-tolerant topologies, the cost factor (CF) is employed. It is defined as

$$\text{CF} = \frac{\text{Cost ofthe fault tolerant inverter}}{\text{Cost of the standard inverter}}. \quad (35)$$

To provide a basis for such as a comparison, the cost of the components is expressed in terms of IGBT cost, which is assumed to be 1 pu. Therefore, the relative costs of the different components used in the fault-tolerant topologies are as follows: DC-link capacitor: 2.5 pu; the fuse: 0.5 pu; SCR: 0.5 pu; and TRIAC: 1 pu. If the power is reduced by 50% of the rated power, the costs of the IGBT and the capacitor are reduced to 0.7 and 1.75 pu, respectively [55], [56].

VI. Conclusion

Reliability is an important performance factor in power electronics system. This paper presented the faults of power device modules in power converters and their handing methods. This paper first provided an overview of the major failure mechanisms of the power IGBT modules. The methods for lifetime prediction and estimation of the junction temperature of IGBT modules are then discussed. In addition, short- and open-circuit fault detection methods are discussed and evaluated. Finally, fault-tolerant strategies have been introduced to improve the reliability of power electronic systems under field operation, and the proposed methods are compared in terms of performance and cost.

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