Online High-Power P-i-N Diode Chip Temperature Extraction and Prediction Method With Maximum Recovery Current *di/dt*

Haoze Luo, Wuhua Li, *Member, IEEE*, and Xiangning He, *Fellow, IEEE*

***Abstract*—P-i-N diode chip temperature is a significant indicator when evaluating the reliability of high-power converters. The feasibility of state-of-the-art thermosensitive electrical parameter (TSEP) extraction strategies for a high-power module is investigated and the limitations of using forward voltage drop for high-power P-i-N diode TSEP are explored. In the widely employed half-bridge topology, by detailed analysis of the upper antiparallel diode reverse recovery process due to lower nonideal insulated-gate bipolar transistor switching behavior, the inherent monotonic relationship between the maximum recovery current rate di_d/dt and chip temperature is disclosed. The maximum di_d/dt during the recovery period is chosen as the better TSEP, which can accurately reflect P-i-N diode chip temperature variation. Fortunately, by monitoring the negative peak voltage on the parasitic inductor between the Kelvin and power emitters under different temperatures, the maximum recovery rate di_d/dt can be readily determined. Consequently, additional passive components are not required for P-i-N diode chip temperature extraction, which is practical and cost-effective for high-power applications. Finally, a dynamic switching characteristics test platform based on a half-bridge topology is designed and adopted to experimentally verify the theoretical analysis. The experimental results show that the dependence between P-i-N diode chip temperature and the maximum recovery di_d/dt is approximately linear. This leads to a 3-D lookup table that can be used to estimate online P-i-N diode chip temperature.**

***Index Terms*—Chip temperature extraction, high-power P-i-N diode modules, reverse recovery current *di/dt*, thermosensitive electrical parameter (TSEP).**

I. Introduction

HIGH-POWER converter capacity is increasing in industrial applications. For instance, the power rating has been extended to 100 MW in electric propulsion systems [1] and over 1000 MVA in high-voltage direct current transmission systems used to enhance the flexibility of modern power systems [2]. Although power semiconductor and manufacturing techniques are continually improving, the switching power and switching frequency product of hard switching has been restricted to approximately 10^9–10^{10} VA/s due to material limitations of silicon-based power devices [3]. An auxiliary snubber circuit with advanced modulation can provide optimized operation for the power devices and increase the frequency–power product to 5×10^9 VA/s [4]. Unfortunately, the auxiliary snubber is complex and difficult to design in high-power conversion systems. Wide bandgap semiconductors, such as silicon carbide devices, are promising candidates to break through the frequency–power product limitation of silicon-based power devices. However, the use of such power devices for the high-power applications is rare, since they are currently too expensive for the industrial applications. Consequently, silicon-insulated-gate bipolar transistors (IGBTs) are still the mainstream power devices for MW high-power systems.

The potential of IGBT power modules has not been fully exploited. Increasing chip operating temperatures from 150 to 175 °C, and higher, would reduce heat sink size and enhance the power density [5]. Nearly 60% of power device failures are temperature induced [6]. For instance, the wire-bond, emitter metallization, and die-attach interfaces are the common power module failure areas, and are related to the mean temperature $T_{\rm m}$ and the thermal swing amplitude ΔT_j during power cycling. The thermal swing amplitude ΔT_j has more impacts on power module life than the mean temperature T_m [7]. The chip temperature T_j of power semiconductors during high-power converter operation is a significant parameter, which can provide valuable information on the internal operational status.

IGBT failure mechanisms are discussed in the literature and research effort has been devoted to IGBT failure reduction [5], [7]–[10]. For commercial high-power IGBT modules, the transient thermal impedance of the antiparallel diodes is higher than that of the IGBTs. Also, the safety operation area (SOA) of antiparallel diodes is smaller than that of the IGBTs. For MW wind power generators, a power cycling overview of two-level wind power converters under full-grid code operation is presented in [11]. It is concluded that when the generator-side converter operates as a rectifier or with rated reactive power injection, higher conduction losses are produced in the antiparallel diodes than in the IGBTs. Therefore, the antiparallel diodes have a higher chip mean temperature T_m than the IGBTs. The unbalanced power losses distribution in a neutral point clamped three-level topology is discussed in [12]. From the simulated losses distribution and the corresponding average chip temperature comparison, the antiparallel diodes are clearly identified with the higher thermal stress. Generally, the switching frequency and output power of converter systems are restricted by the highest thermally stressed power device. Consequently, the reliability

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The authors are with the College of Electrical Engineering, Zhejiang University, Hangzhou 310027, China (e-mail: woohualee@zju.edu.cn).

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design of the antiparallel diodes is important. As a result, monitoring the chip temperature in a power module, especially the antiparallel diodes, can enable a power module to operate within its SOA.

In practice, operational chip temperature and thermal swing of power modules vary with thermal design and operation mode [13]. Consequently, achieving accurate online thermal stress measurement and monitoring is paramount to improving reliability in MW high-power conversion systems. Conventional IGBT chip temperature measurement methods can be divided into optical, physical contact and thermosensitive electrical parameter (TSEP) methods [14], [15]. The TSEP extraction method is the only way to attain fast (within 100 μs) measurement from packaged IGBT modules [16]. However, most online chip temperature measurement methods focus on the IGBT rather than the antiparallel diode.

P-i-N power diodes with breakdown voltages of several kilovolts are mainly used as antiparallel diodes in high-voltage IGBT modules and high-power applications [17]. In this paper, the typical TSEP extraction methods for temperature indication of the high-power IGBTs and P-i-N diodes are summarized and the feasibility of online testing of these methods is assessed first. From the insightful overview of the TSEP extraction methods, it will be concluded that most TSEP extraction methods cannot directly be employed to evaluate high-power P-i-N diodes. It is summarized that the reverse recovery current and forward voltage drop are two important TSEPs of high-power P-i-N diodes. Hence, this study aims to explore the interaction between P-i-N diode chip temperature and reverse recovery current. Although the suitability of measuring the other TSEPs that could be used has also been studied, the maximum recovery current rate *di/dt* is chosen as better when extracting the chip temperature of high-power P-i-N diodes.

This paper is organized as follows: In Section II, the feasibility of online temperature extraction-based TSEPs is overviewed, and a new online temperature measurement method for the high-power P-i-N diode is proposed. In Section III, the proposed approach is discussed, and the P-i-N diode reverse recovery process with nonideal IGBT switching commutation, in a half-bridge topology, is analyzed in Section IV. The relationship between reverse recovery current and diode chip temperature is discussed in Section V. In Section VI, the substantiating experimental results are presented, and this paper is concluded in Section VII.

II. Feasibility of Online Power Module Temperature Extraction

A. TSEP Approaches for Online Power Module Temperature Measurement

Most physical parameters of silicon semiconductor devices are temperature dependent. The intrinsic carrier concentration and carrier lifetime increase with silicon temperature, but the mobility of electrons and holes decreases with temperature [18]. Because the relationships between semiconductor physical parameters and temperature exist, the chip temperature can be extracted from the electrical characteristics without access into the package. This means thermal sensors or infrared instruments are not required for simple noninvasive online chip temperature extraction. Consequently, many TSEP approaches have been proposed, which can be classified into static and dynamic-based parameters, as illustrated in Fig. 1.

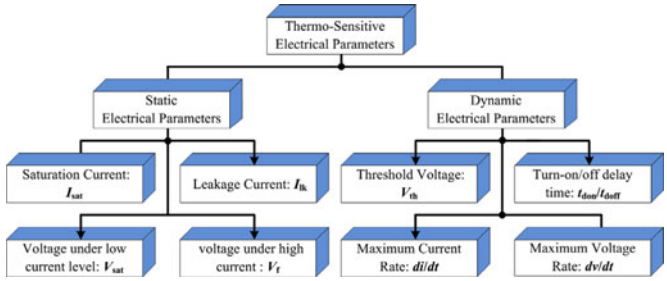

Fig. 1. Classification of TSEPs.

The static parameters are constant at a defined chip temperature. These parameters can be extracted when the power device operates in the on-state or the off-state. In the case of high-power P-i-N diodes, static parameters like I_{lk} and $V_{\rm sat}$ can be chosen as TSEPs. However, leakage current I_{lk} is relatively low. Any milliampere-level current sensor inserted in series with the power module would suffer the large operational current when the power module is in the conducting on-state. The forward voltage drop under low injection current $V_{\rm sat}$ can be adopted to predict the chip temperature and monitor wire bonding lift-off [19], [20]. But precise current-injection equipment is required to ensure that the current is low enough to avoid self-heating effects. Moreover, the measurement equipment requirements are high when using I_{lk} and $V_{\rm sat}$ as TSEPs.

Unlike static parameters, dynamic parameters can be obtained during the switching transient of the power module [21]. Because the passive power P-i-N diode does not need a gate driver, the plotted TSEPs like $V_{\rm th}$ and $t_{d\_{\rm on}}/t_{d\_{\rm off}}$ are usually for used IGBT modules. Therefore, the chip temperature estimation of power P-i-N diodes should be carried out by monitoring the maximum *dv/dt* during the turn-off transition, which is sensed by a shunt-connected capacitor. Similarly, the maximum *di/dt* measurement uses a series-connected inductor. As a result, the forward voltage drop under high current injection V_F, or *di/dt* and *dv/dt* dynamic parameters can be employed to indirectly extract P-i-N diode chip temperature. However, in the case of P-i-N diodes, there is somewhat limitation on the use of V_F-based TSEP.

B. Limitation of Forward Voltage Drop for TSEP

In [22], the on-state voltage drop V_F under high current injection is used as a TSEP. However, the high-power P-i-N diode is a typical bipolar device, where the typical forward *I–V* characteristic in Fig. 2 shows the 25 and 125 °C curves intersecting, at intersection A.

As in Fig. 2, around a particular current, close to the load current, V_F has the property of both negative and positive temperature coefficients (NTC/PTC) depending on the current rating.

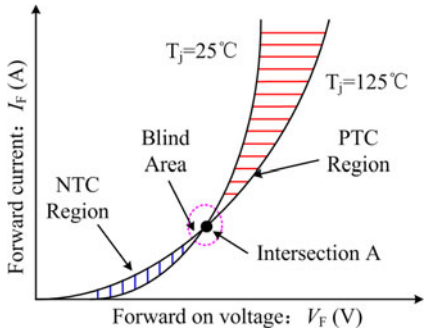

Fig. 2. Forward current versus forward on-voltage characteristics.

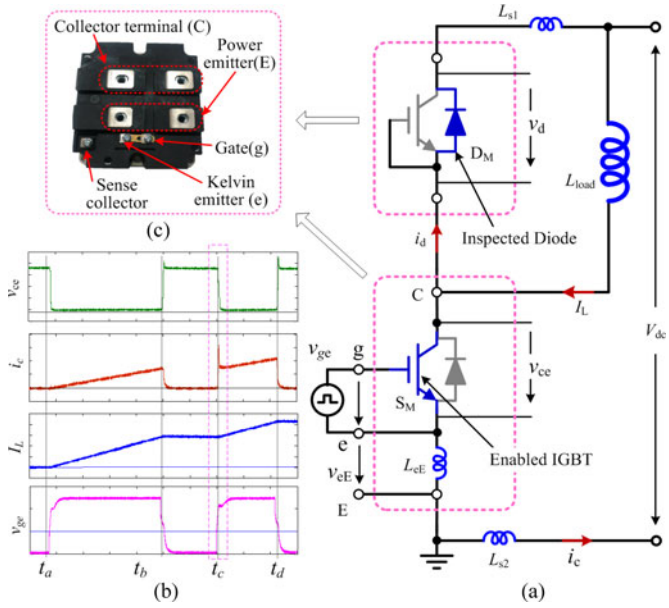

Fig. 3. Diagram of dynamic switching performance test platform with parasitic inductors and double pulse test sequence.

V_F declines as the chip temperature rises for a certain current in the NTC region, but increases in the PTC region. It can be seen the closer to intersection A, the lower the TSEP sensitivity ratio. There would be a "blind region" for the TSEP near intersection A, where it is difficult to determinate the chip temperature when only utilizing V_F. When commutating from conduction to the reverse-biased state, the charges stored in the diode base region have to be swept out during the reverse recovery process because the reverse recovery behavior is strongly affected by the P-i-N diodes chip temperature. Consequently, dynamic parameter extraction approaches based around the reverse recovery process are better candidates for TSEPs of high-power P-i-N diodes.

III. Diode Temperature Extraction Using a Dynamic TSEP

The dynamic switching performance IGBT module test platform in Fig. 3 uses the conventional double-pulse test method.

In Fig. 3(a), the half-bridge topology platform is composed of an upper IGBT module with antiparallel diode D_M which is the inspected P-i-N diode, a lower switch S_M with an antiparallel diode, and a load inductor $L_{\rm load}$. The conventional double-pulse test sequence is plotted in Fig. 3(b). The inductor $L_{\rm load}$ is energized through switch S_M to the desired current, at a certain bus voltage, in the first pulse. The current then freewheels when $S_{\rm M}$ is turned off. When the second turn on pulse is applied to switch S_M at time t_c, the switching waveforms, such as gate driver signal, chip temperature, collector voltage, and collector current are captured for power device switching performance evaluation [23]. The TSEPs of high-power P-i-N diodes can also be measured and extracted with this single-ended chopper test platform because the dynamic switching performance of the P-i-N diodes is intertwined with that of the IGBTs.

In high-power device packages, due to the connection of the aluminum wire between die and the copper layer, and the connection between the die and power terminals, there are small parasitic inductors between the output terminals and inner die in modules. Generally, there are two emitter terminals for high-power IGBTs as shown in Fig. 3(c), namely the Kelvin emitter for the gate driver and the power emitter for the power path. The inductor L_{s1} is the combination of the series parasitic inductors in the upper D_M module and the positive bus bar parasitic inductor. $L_{\rm eE}$ is the parasitic inductor between Kelvin emitter and the lower IGBT module power emitter. L_{s2} is the sum of the series parasitic inductors in the lower IGBT module and the negative bus bar parasitic inductor, excluding $L_{\rm eE}$. Together these parasitic inductors perform a turn-on snubber function. In the test bench in Fig. 3(a), for current commutation from antiparallel diode D_M to switch S_M, initially the load current I_L flows through $L_{\rm load}$, D_M, and L_{s1}, when switch S_M is in an off-state between t_b and t_c. By turning on S_M at t_c, the load current I_L begins to commutate from diode D_M to switch S_M. The reverse recovery current of diode D_M, which is dependent on chip temperature, induces a measurable voltage $v_{\rm eE}$ across the parasitic inductor $L_{\rm eE}$ during the S_M turn-on transition. Compared with *dv/dt* measurement, auxiliary sensor components are not required for *di/dt* measurement. Because the parasitic inductor is tens of nanohenries, $v_{\rm eE}$ is tens of voltages under high load current. Once the relationship between the voltage $v_{\rm eE}$ and the D_M chip temperature T_D is characterized, the chip temperature can be extracted, facilitating a measurement circuit design, at the emitter potential, without auxiliary high voltage or isolated sensors.

In former literatures, the bond wire voltage drop $v_{\rm eE}$ is actively measured and used for the estimation of IGBT chip temperature and closed-loop gate driver [24]–[26]. The voltage signal $v_{\rm eE}$ measurement can be realized with some fast operational amplifiers and can be integrated into the gate drive circuit [27]. This measurement circuit can be also directly shifted to the gate driver in Fig. 3(a) with half-bridge topology. The voltage signal $v_{\rm eE}$, containing the P-i-N diode chip temperature information, can be monitored and assessed in every switching cycle. This approach can quickly detect P-i-N diode chip temperature and quickly derate the system or increase the cooling capability. Also, the thermal swing amplitude can be limited to improve the power converter reliability. The reverse recovery time and current of silicon carbide diodes are small, so this approach for

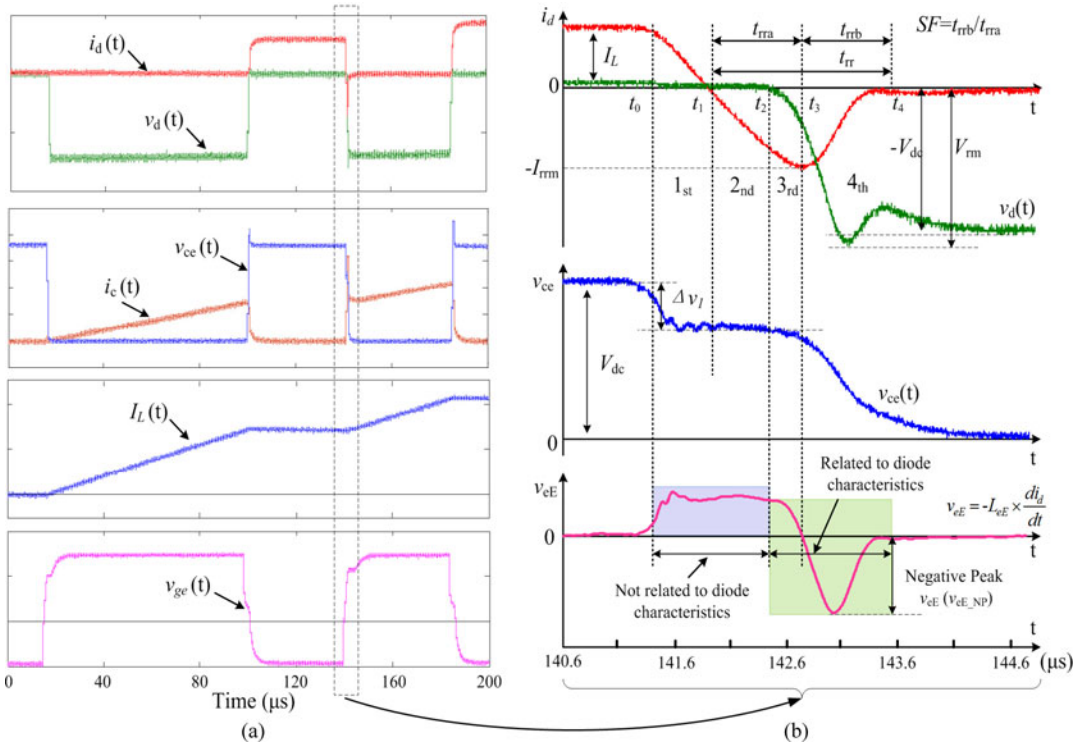

Fig. 4. Related waveforms of conventional double pulse test: (a) test sequence and measured waveforms of $L_{\rm load}$, S_M, and D_M and (b) reverses recovery waveforms and induced $v_{\rm eE}$ during the second turn-on transition.

indirect temperature extraction may not be applicable to high-power silicon carbide diodes.

IV. Diode Reverse Recovery Process With Nonideal IGBT Switching Behavior

In order to further explain the P-i-N diode reverse recovery process, in Fig. 3(a), D_M is the tested device, $V_{\rm dc}$ is the bus voltage, v_d is the diode voltage of inspected D_M, i_d is the diode current, I_L is the load current, i_c is the collector current of S_M, $v_{\rm ge}$ is the gate driver waveform, and $v_{\rm ce}$ is the collector–emitter voltage of S_M. S_M is turned on and off to form the dynamic switching test for D_M. The key waveforms of the conventional double pulse test at a certain ambient temperature are shown in Fig. 4, along with the corresponding $v_{\rm eE}$ waveforms induced by the reverse recovery current.

The complete high-power P-i-N diode turn-off transition can be divided into four periods as follows. Before time t_0, the forward current I_L flows though P-i-N diode D_M, inductor $L_{\rm load}$, and parasitic inductor L_{s1}. The D_M is in a forward-biased state with a low on-state voltage. Switch S_M is in the turn-off state, while the voltage across S_M equals the bus voltage $V_{\rm dc}$. Switch turn-on is initiated by applying gate voltage.

Stage 1 [t_0, t_1]: At t_0, the gate–emitter voltage $v_{\rm ge}$ reaches the threshold voltage $V_{\rm th}$, where the forward current of the diode i_d is equal to I_L and begins to decline with an approximately fixed linear slope. Although the diode carrier concentration decays rapidly, D_M retains a forward voltage drop. The collector–emitter voltage $v_{\rm ce}$ of S_M falls to a platform voltage Δv_1 during this stage. During this stage, following the expression:

$$v_{\rm ce}(t) = V_{\rm dc} - (L_{s2} + L_{\rm eE})\frac{di_c(t)}{dt} \tag{1}$$

where $i_c(t)$ is the collector current though S_M. The di_c/dt is determined by the bus voltage $V_{\rm dc}$, the loop parasitic inductors, and the switching speed of switch S_M.

Stage 2 [t_1, t_2]: At t_1, the forward current though diode D_M has linearly decreased to zero and a reverse recovery current occurs due to the stored charges. The P-i-N diode voltage decreases but the junction remains slightly forward biased. Because the space charge region is not completely depleted, the P-i-N diode remains in on-state with negligible forward voltage v_d. At t_2, the carrier concentration in the space charge region of the diode $\rm P^+n^-$ junction falls to zero, when the diode can support reverse voltage as the depletion region widens. The collector current i_c of IGBT S_M is composed of the reverse recovery current i_d and load current I_L

$$i_c = I_L + i_d. \tag{2}$$

Therefore, the di_c/dt is mainly due to the bus voltage $V_{\rm dc}$ and the commutation loop parasitic inductors L_{s1}, L_{s2}, and $L_{\rm eE}$ as shown in Fig. 3(a). Thus, di_c/dt during *stage 1* and *stage 2* is defined as CS_a, given by

$$CS_a = \frac{di_c}{dt} = -\frac{V_{\rm dc} - v_{\rm ce}}{L_{s1} + L_{s2} + L_{\rm eE}}. \tag{3}$$

Stage 3 [t_2, t_3]: At t_2, diode D_M begins to support reverse blocking voltage v_d which increases as the depletion region widens. Now, the di_c/dt is influenced by diode D_M

TABLE I
SUMMARY OF FACTORS AFFECTING REVERSE RECOVERY CURRENT RATE

	Stages	Parasitic inductor	Bus voltage $V_{\rm dc}$	Collector voltage $v_{\rm ce}$	Diode voltage v_d
Negative current slope di_d/dt	Stage 1	√	√	√	×
	Stage 2	√	√	√	×
	Stage 3	√	√	√	√
Positive current slope di_d/dt	Stage 4	√	√	√	√

characteristics and defined as CS_b during this stage, which is derived from

$$CS_b = \frac{di_c}{dt} = -\frac{V_{\rm dc} - v_{\rm ce} - v_d}{L_{s1} + L_{s2} + L_{\rm eE}}. \quad (4)$$

Stage 4 [t_3, t_4]: During this stage, the current $di_d(t)/dt$ is defined as the recovery *di/dt* [28], which is represented by CS_c

$$CS_c = \frac{di_d}{dt} = \frac{V_{\rm dc} - v_{\rm ce} - v_d}{L_{s1} + L_{s2} + L_{\rm eE}}. \quad (5)$$

At t_3, the reverse recovery current rate di_d/dt of diode D_M falls to zero because the diode current i_d has reached its negative peak $-I_{\rm rrm}$. Then, the diode reverse current i_d begins to fall to zero. The diode voltage v_d at t_3 is given by

$$v_d = V_{\rm dc} - v_{\rm ce}. \quad (6)$$

At the maximum di_d/dt, the voltage across diode D_M reaches its peak $V_{\rm rm}$. Since the inductance produces unexpected overshoot, $V_{\rm rm}$ is higher than $V_{\rm dc}$. Considering $v_{\rm ce}$ and v_d are influenced by the chip temperature of the power module, it can be concluded that the current rate CS_c is determined by the P-i-N diode and IGBT characteristics once the external circuit parameters are determined. From the presented analysis, Table I summarizes the relationship between P-i-N diode di_d/dt, parasitic inductor, bus voltage, diode voltage, and switch collector voltage during the diode reverse recovery process. For inductive loads, it is reasonable to assume that the load current I_L remains constant during the relative brief switching transition process.

The diode di_d/dt is equal to di_c/dt. From *stage 1* to *stage 3*, the dynamic di_d/dt may induce a positive $v_{\rm eE}$ on the parasitic inductor $L_{\rm eE}$. This measurable voltage $v_{\rm eE}$ is determined by the switch S_M turn-on behavior from *stage 1* to *stage 3* and the characteristics of diode D_M in *stage 3*. As a result, during *stage 1* and *stage 2*, the voltage $v_{\rm eE}$ cannot be used as the TSEP for the power P-i-N diode because $v_{\rm eE}$ is not related to the diode characteristics. Although the switch collector voltage $v_{\rm ce}$ and diode voltage v_d of D_M have distinct contributions to the $v_{\rm eE}$ during *stage 3*, it is difficult to accurately determine the interval when operation enters *stage 3*. Furthermore, *stage 3* is too brief to extract the voltage $v_{\rm eE}$, as seen in Fig. 4.

Fortunately, during *stage 4*, the P-i-N diode di_d/dt is positive, and has a distinct relationship with P-i-N diode voltage $v_d(t)$ and switch collector voltage $v_{\rm ce}(t)$. When di_d/dt varies from negative to positive, *stage 4* starts. This means that the accurate start instant of *stage 4* is readily captured. In *stage 4*, the relationship between the voltage $v_{\rm eE}$ and the di_d/dt can be derived from

$$v_{\rm eE} = -L_{\rm eE}\frac{di_d(t)}{dt}. \quad (7)$$

From (7), the maximum di_d/dt can be obtained by measuring the negative peak voltage $v_{\rm eE\_NP}$ during *stage 4*. From power semiconductor fundamentals, once the negative peak voltage $v_{\rm eE\_NP}$ is captured, the maximum di_d/dt is obtainable. This indicates that CS_c in *stage 4* can be employed as the TSEP to predict or estimate P-i-N diode chip temperature.

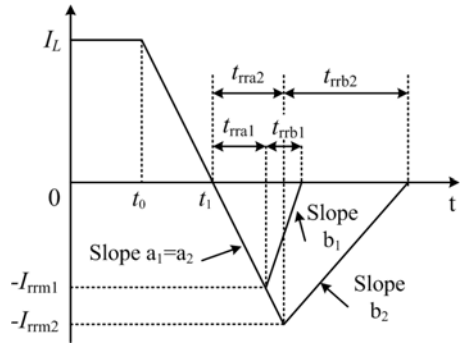

Fig. 5. Simplified diode current waveforms during turn-off process at different diode chip temperatures and a fixed IGBT temperature.

V. EXPLORATION OF THE RELATIONSHIP BETWEEN RECOVERY CURRENT RATE AND CHIP TEMPERATURE

In order to simplify P-i-N diode reverse recovery current analysis, the variation of free carrier concentration in the diode drift region can be approximated as linear. As a result, the P-i-N diode reverse recovery current from *stage 2* to *stage 4* in Fig. 4 can be substituted by a triangle [29], [30]. In the high-power and high-voltage applications, the P-i-N diode voltage v_d during *stage 3* is significantly smaller than $V_{\rm dc}$, so can be ignored. Consequently, during stages 1–3, the di_d/dt before the peak reverse recovery current is related to switch S_M conditions and external circuit parameters. Thus P-i-N diode behavior has minimal contribution to the di_d/dt. This implies that the current slopes before the peak $I_{\rm rrm}$ are the same under different P-i-N diode chip temperatures, for fixed external circuit parameters. However, after the peak reverse recovery current $I_{\rm rrm}$, during *stage 4*, the maximum di_d/dt of practical diode operation varies with P-i-N diode chip temperature. The maximum di_d/dt variation for different diode chip temperatures is reflected by current slope changes in *stage 4*. From this analysis, the simplified diagram of the P-i-N diode reverse recovery current at different chip temperatures, with a fixed IGBT temperature, is plotted in Fig. 5. The diode D_M temperature is defined as T_D and two P-i-N diode chip temperatures T_{D1} and T_{D2} are given, where T_{D2} is higher than T_{D1}. The related definitions labeled in Fig. 5 are listed in Table II.

From Figs. 4 and 5, the maximum di_d/dt after diode peak reverse recovery current can be approximated by

$$\frac{di_d}{dt}\Big|_{\rm max} \approx \frac{I_{\rm rrm}}{t_{\rm rrb}}. \quad (8)$$

TABLE II
ELECTRICAL DEFINITIONS FOR DIFFERENT DIODE TEMPERATURES

Notations	T_{Dl}	T_{D2}
Reverse peak current	$l_{\mathrm{rrm}1}$	$l_{\mathrm{rrm}2}$
Current slope before reverse peak current	a_1	a_2
Current slope after reverse peak current	b_1	b_2
Recovery time	$t_{\mathrm{rrb}1}$	$t_{\mathrm{rrb}2}$
Storage time	$t_{\mathrm{rra}1}$	$t_{\mathrm{rra}2}$
Constant load current	I_L	I_L

In the case of high-level injection current, the high-level carrier lifetime τ_{HL} of the power diode can be expressed by

$$\tau_{\mathrm{HL}} \approx \frac{Q_{\mathrm{rr}}}{I_L} \tag{9}$$

where Q_{rr} is the reverse recovery charge stored in the power diode before commutation. Because the diode carrier lifetime τ_{HL} increases with chip temperature increase, the relationship between τ_{HL} and P-i-N diode chip temperature T_D can be modeled by

$$\tau_{\mathrm{HL}} = \tau_0 \left(\frac{T_D}{300}\right)^k \tag{10}$$

where the exponent k varies from 2 to 2.5 [18]. From (9) and (10), once chip temperature T_{D2} is higher than T_{D1}, the diode stored charge Q_{rr} ($T_{\mathrm{D}2}$) at $T_{\mathrm{D}2}$ is larger than its charge at T_{D1}. Diode softness factor *SF* is defined as the ratio of the recovery time t_{rrb} to storage time t_{rra}, that is

$$SF = \frac{t_{\mathrm{rrb}}}{t_{\mathrm{rra}}}. \tag{11}$$

Since the current slope a_1 is equal to slope a_2 as plotted in Fig. 5, it can be derived from

$$\frac{I_{\mathrm{rrm}1}}{t_{\mathrm{rra}1}} = \frac{I_{\mathrm{rrm}2}}{t_{\mathrm{rra}2}} \Rightarrow I_{\mathrm{rrm}1} \cdot t_{\mathrm{rra}2} = I_{\mathrm{rrm}2} \cdot t_{\mathrm{rra}1}. \tag{12}$$

Because the softness factor *SF* increases with increased diode temperature, under fixed forward current [28], then

$$\frac{t_{\mathrm{rrb}2}}{t_{\mathrm{rra}2}} > \frac{t_{\mathrm{rrb}1}}{t_{\mathrm{rra}1}}. \tag{13}$$

From (11) and (13), the maximum di_d/dt at T_{D1} is higher than that at T_{D2}, which is given by

$$\frac{I_{\mathrm{rrm}1}}{t_{\mathrm{rrb}1}} > \frac{I_{\mathrm{rrm}2}}{t_{\mathrm{rrb}2}} \Rightarrow \frac{di_d}{dt}\Big|_{\max}(T_{D1}) > \frac{di_d}{dt}\Big|_{\max}(T_{D2}). \tag{14}$$

From (14), it can be concluded that the relationship between the maximum di_d/dt and T_D is monotonic during the recovery period (in *stage 4*). The maximum di_d/dt during the recovery period decreases as diode chip temperature increases. As a result, the maximum di_d/dt during the recovery period is an effective TSEP, which reflects P-i-N diode chip temperature variation.

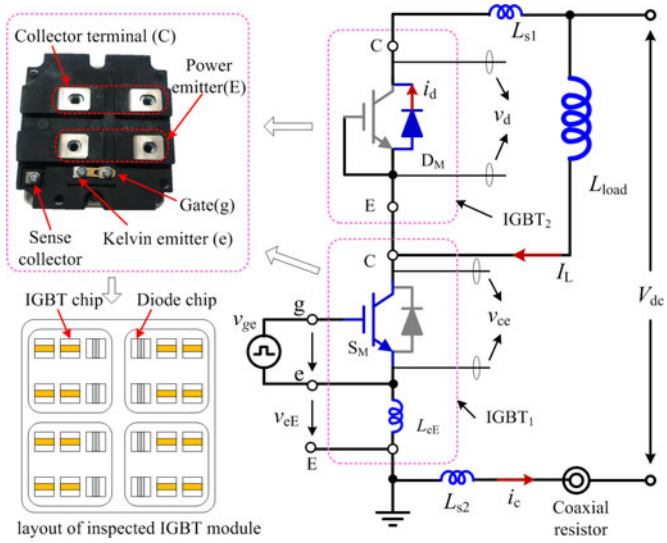

Fig. 6. Diagram of test platform and layout of an inspected power module.

TABLE III
PROTOTYPE SPECIFICATIONS

Parameters	**Value**
IGBT module	IMBI800UG-330
V_{dc}	1200–1600 V
I_L	200–500 A
Bus capacitor	1000 μF
L_{load}	400 μH
Gate driver voltage v_{ge}	+15 V on/–10 V off
Turn-on gate driver resistor	2.4 Ω
Turn-off gate driver resistor	3.75 Ω

VI. EXPERIMENTAL VERIFICATION

In order to verify the revealed relationship between the maximum di_d/dt and T_D during the recovery period, the device test requirements for Fig. 3 are expanded in Fig. 6. The antiparallel diode D_M is employed as the inspected diode and S_M is used to generate dynamic switching operation.

Two separate high-power IGBT modules with associated antiparallel diodes are mounted on two independent heat-sinks to allow independent chip temperatures. And a constant temperature box is employed the make sure the chip temperature is quite similar to the surrounding temperature. In order to minimize any self-heating caused by forward conduction losses of D_M, the time interval between the two pulses is minimized, 40 μs. A time interval between each test ensures a constant, uniform device temperature distribution. The test bed soak heats the base plate, die, and material surrounding the die, all to the required chip temperature. Given the mass around the die and its thermal time constant, in conjunction the relatively short test duration, the switching process can be considered adiabatic, with minimal self-heating because of the short duration of the test.

The associated experimental parameters are given in Table III. The Fuji Corporation 3300 V/800 A IGBT (1MBI800UG-330)

TABLE IV
CALCULATION UNDER OPERATION CONDITION

Operation condition	25 °C	75 °V	125 °C
200 A	6.63 nH	6.62 nH	6.10 nH
300 A	6.24 nH	6.55 nH	6.08 nH
400 A	6.05 nH	6.33 nH	6.37 nH
500 A	6.28 nH	6.39 nH	6.83 nH

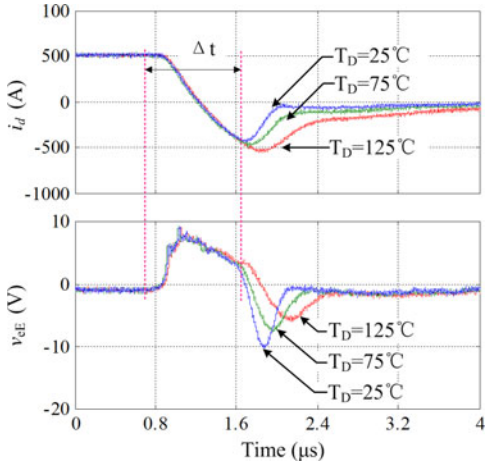

Fig. 7. Waveforms of diode current i_d and voltage v_{eE} at different T_D and constant enabling IGBT temperature ($V_{\mathrm{dc}} = 1600$ V, $I_L = 400$ A, and $T_{\mathrm{IGBT}} = 25\,^{\circ}\mathrm{C}$).

is employed to examine its antiparallel P-i-N diode behavior at different chip temperatures. It consists of eight parallel connection diode chips and 16 parallel connection IGBT chips as shown in Fig. 6. Based on the industrial applications of this IGBT module type, V_{dc} is set to 1600 V. The bus capacitors are 1000 μF, to maintain the bus voltage. The load inductor is 400 μH to ensure near constant current during the tested switching period.

A proportionality constant L_{eE} is the precondition for using di_d/dt to determine the diode chip temperature. The calculation of L_{eE} at typical operation currents and temperatures are summarized under 1600 V bus voltage in Table IV. It can be found that the value of L_{eE} is proportionality constant under different operation conditions.

The experimental waveforms of P-i-N diode reverse recovery current i_d and induced voltage v_{eE} under different P-i-N diode chip temperatures are shown in Fig. 7. The diode chip temperature is controlled and varied between 25 and 125 °C by averaging successive regulation, while the enabling IGBT module temperature is maintained at 25 °C. Thus, the influence of IGBT characteristics, on the reverse recovery process, is eliminated.

From Fig. 7, the current waveforms before the peak are the same because of the fixed enabling T_{IGBT} and the fixed external circuit parameters. The peak reverse recovery current increases from 440 A ($T_{\mathrm{D}} = 25\,^{\circ}\mathrm{C}$) to 550 A ($T_{\mathrm{D}} = 125\,^{\circ}\mathrm{C}$). Because the carrier lifetime of D_M increases as T_D increases, the reverse recovery current peak magnitude is proportional to the rise in

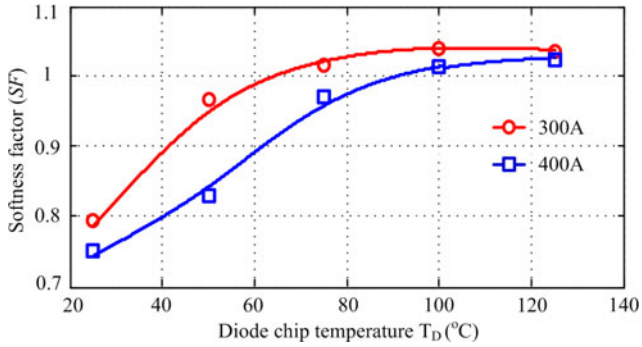

Fig. 8. Experimental results of *SF* against P-i-N diode chip temperature with varying forward diode current at $V_{\mathrm{dc}} = 1600$ V.

diode chip temperature. The time interval Δt in Fig. 7 represents the period of *stage 1* and *stage 2* in Fig. 4. Because the commutation speeds are the same during Δt, the voltage waveforms of v_{eE} are the same although the P-i-N diode chip temperatures are different. However, the voltages v_{eE} after Δt are different due to the different temperature-dependent P-i-N diode characteristics. Once the recovery current rate reaches its maximum, the induced voltage v_{eE} on the parasitic inductor L_{eE} reaches the negative peak value. As T_D increases, the current rate becomes lower in *stage 4*. Therefore, the negative peak value of v_{eE} reduces with increasing T_D although the time to the peak increases. It can be concluded that the negative peak voltage v_{eE} induced by the maximum recovery di_d/dt is an appropriate TSEP.

The diode softness factor *SF* versus T_D is shown in Fig. 8, with varying load currents and a constant 1600 V bus voltage. *SF* increases with rising T_D, at different load currents. The measured results are in agreement with the analysis in [28].

Because the value of L_{eE} is proportionality constant, $v_{\mathrm{eE\_NP}}$ is proportional to the maximum recovery current di_d/dt-based TSEP as shown in (7). The measured $v_{\mathrm{eE\_NP}}$ at different diode chip temperatures and load currents are illustrated in Fig. 9. According to the presented analysis, carrier lifetime increases with increased T_D. Consequently, more carriers need to be swept out when the temperature increases.

Therefore, the absolute value of $v_{\mathrm{eE\_NP}}$ induced by the maximum recovery current di_d/dt plotted in Fig. 9 shows a declining tendency with increasing T_D under the same load current, as from inequality (14). When the P-i-N diode chip temperature is constant, the measured $v_{\mathrm{eE\_NP}}$ is proportional to load current. The sensitivity ratio of $v_{\mathrm{eE\_NP}}$ at 200 A is about 70 mV/°C and 48 mV/°C at 500 A, as in Fig. 9(a).

The variation of $v_{\mathrm{eE\_NP}}$ with P-i-N diode chip temperature at different bus voltages is illustrated in Fig. 10. As the bus voltage increases under the same T_D, the carries stored in the P-i-N diode base region are swept out quicker. Thus, the absolute values of $v_{\mathrm{eE\_NP}}$ increase with increasing V_{dc}. In Fig. 10(a), the sensitivity is in the range 60 mV/°C ($V_{\mathrm{dc}} = 1600$ V) to 45 mV/°C ($V_{\mathrm{dc}} = 1200$ V). In Fig. 10(b), when the load current I_L increases to 400 A, the sensitivity ratio range is 62 mV/°C ($V_{\mathrm{dc}} = 1600$ V) to 39 mV/°C ($V_{\mathrm{dc}} = 1200$ V).

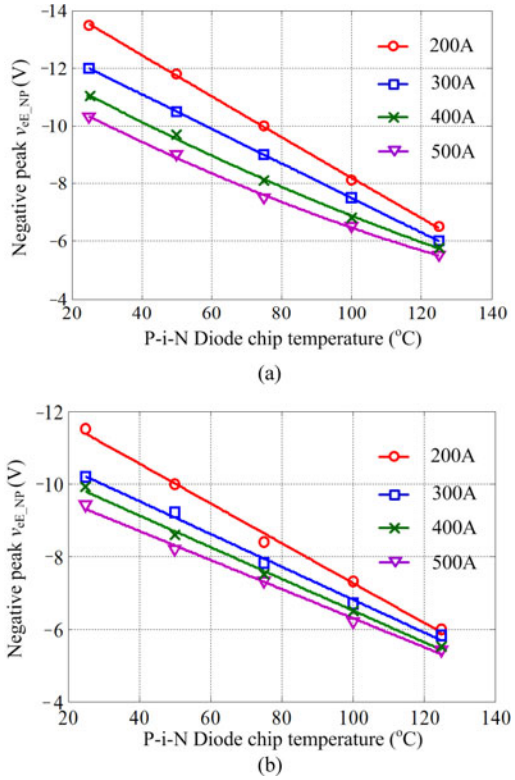

Fig. 9. Correlation between negative peak voltage of v_{eE}, P-i-N diode chip temperature, and load current: (a) bus voltage $V_{\mathrm{dc}} = 1600$ V and (b) bus voltage $V_{\mathrm{dc}} = 1400$ V.

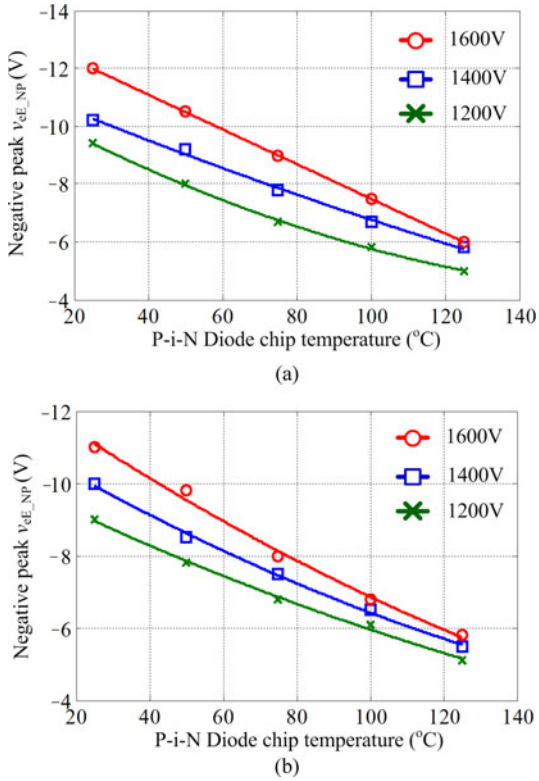

Fig. 10. Variation of $v_{\mathrm{eE\_NP}}$ with T_D and V_d: (a) load current $I_L = 300$ A, enabling IGBT temperature 25 °C and (b) load current $I_L = 400$ A, enabling IGBT temperature 25 °C.

Figs. 9 and 10 present the extracted dependences of the $v_{\mathrm{eE\_NP}}$ against P-i-N diode chip temperature, load current, and bus voltage. The experimental results expose an approximately linear relationship between T_D and $v_{\mathrm{eE\_NP}}$. The sensitivity ratio of the $v_{\mathrm{eE\_NP}}$ is several tens of millivolts per degree (mV/°C). However, the sensitivity ratio of TSEP V_F at 200 and 500 A is about -2 and 0.8 mV/°C, respectively, for a given 1MBI800UG-330 module. This sensitivity of $v_{\mathrm{eE\_NP}}$ is higher than the sensitivity of the forward voltage drop V_F-based TSEP. These two factors make $v_{\mathrm{eE\_NP}}$ induced by the maximum recovery current rate *di/di* an excellent TSEP candidate for extracting P-i-N diode temperature, T_D.

Based on presented analysis, a 3-D database can be created to reflect the relationships between $v_{\mathrm{eE\_NP}}$ across the parasitic inductor L_{eE}, T_D, and the other related factors. A 3-D database of the $v_{\mathrm{eE\_NP}}$ induced by the maximum recovery current rate di_d/dt at different P-i-N diode chip temperatures and load currents with bus voltage $V_{\mathrm{dc}} = 1600$ V and $V_{\mathrm{dc}} = 1200$ V is plotted in Fig. 11.

For a designed voltage-source converter, the gate driver, power devices, and external circuit parameters are fixed. Once the bus voltage, load current, and IGBT temperature are measured, the corresponding P-i-N diode chip temperature can be derived from the 3-D lookup table in Fig. 11. This means that the 3-D database can be used as a lookup table to estimate online, P-i-N diode chip temperature.

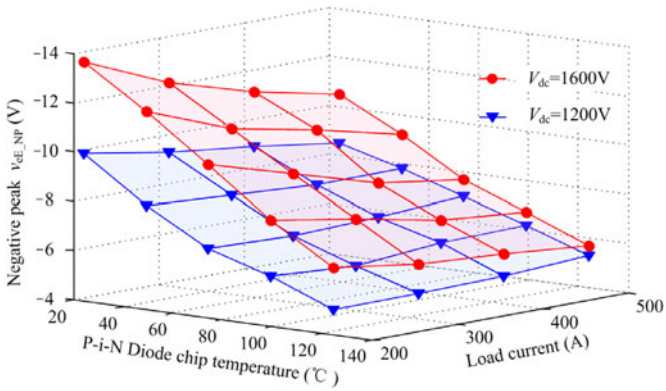

Fig. 11. Three-dimensional database of $v_{\mathrm{eE\_NP}}$ with variety of P-i-N diode chip temperature and load current: (a) bus voltage $V_{\mathrm{dc}} = 1600$ V, IGBT temperature $T_{\mathrm{IGBT}} = 25$ °C and (b) bus voltage $V_{\mathrm{dc}} = 1200$ V, IGBT temperature $T_{\mathrm{IGBT}} = 25$ °C.

VII. Conclusion

This paper proposed a chip temperature extraction method for high-power P-i-N diode modules that utilized the maximum recovery current rate di_d/dt. The measurement feasibility of using the maximum recovery current rate di_d/dt was discussed. It is deduced that the maximum reverse recovery current rate di_d/dt decreases with P-i-N diode chip temperature increase. Consequently, the maximum recovery current rate di_d/dt can

be used as a TSEP for P-i-N diode chip noninvasive temperature extraction.

An experimental platform based on half-bridge topology was used for switching characteristic tests of a high-power device module, there from verifying the theoretical analysis. A constant parasitic inductor between the Kelvin emitter and power emitter terminal L_{eE}, used to measure the negative peak voltage $v_{\mathrm{eE\_NP}}$ on L_{eE}, provides a flexible approach for monitoring the maximum recovery rate di_d/dt. The experimental results show an approximately linear dependence between the P-i-N diode chip temperature and negative peak voltage $v_{\mathrm{eE\_NP}}$. The sensitivity ratio of a $v_{\mathrm{eE\_NP}}$-based TSEP is higher than that of previous TSEP using forward voltage drop. A 3-D database of $v_{\mathrm{eE\_NP}}$ with varying temperature and other relevant factors is invaluable for online chip temperature prediction of P-i-N diodes in real-time operation.

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Haoze Luo was born in Jiangxi, China, in 1986. He received the B.S. and M.S. degrees from the Department of Electrical Engineering, Hefei University of Technology, Hefei, China, in 2008 and 2011, respectively. Since 2011, he has been working toward the Ph.D. degree in the College of Electrical Engineering, Zhejiang University, Hangzhou, China.

His research interests include high-power converters and reliability of high-power modules.

Wuhua Li (M'09) received the B.Sc. and Ph.D. degrees in applied power electronics and electrical engineering from Zhejiang University, Hangzhou, China, in 2002 and 2008, respectively.

From September 2004 to March 2005, he was a Research Intern, and from January 2007 to June 2008, a Research Assistant in GE Global Research Center, Shanghai, China. From July 2008 to April 2010, he joined the College of Electrical Engineering, Zhejiang University, as a Postdoctoral Researcher. In May 2010, he became a faculty member in Zhejiang University as a Lecturer. In December 2010, he was promoted as an Associate Professor. Since December 2013, he has been a Full Professor in the College of Electrical Engineering, Zhejiang University. From July 2010 to September 2011, he was a Ryerson University Postdoctoral Fellow with the Department of Electrical and Computer Engineering, Ryerson University, Toronto, ON, Canada. He has published more than 100 peer-reviewed technical papers and holds more than 30 issued/pending patents. His research interests include high efficiency power converters and renewable energy power conversion system.

Dr. Li received the 2011 Top Ten Excellent Young Staff Award and the 2012 Distinguished Young Scholar from Zhejiang University, the 2012 Outstanding Young Researcher Award from Zhejiang Province, and the 2012 Delta Young Scholar from Delta Environmental & Educational Foundation for his excellent teaching and research contributions. He received three Scientific and Technological Achievements Awards from Zhejiang Provincial Government and the State Educational Ministry of China in 2009 and 2011, respectively.

Xiangning He (M'95–SM'96–F'10) received the B.Sc. and M.Sc. degrees from the Nanjing University of Aeronautical and Astronautical, Nanjing, China, in 1982 and 1985, respectively, and the Ph.D. degree from Zhejiang University, Hangzhou, China, in 1989.

From 1985 to 1986, he was an Assistant Engineer at the 608 Institute of Aeronautical Industrial General Company, Zhuzhou, China. From 1989 to 1991, he was a Lecturer at Zhejiang University. In 1991, he obtained a Fellowship from the Royal Society of U.K., and conducted research in the Department of Computing and Electrical Engineering, Heriot-Watt University, Edinburgh, U.K., as a Postdoctoral Research Fellow for two years. In 1994, he joined Zhejiang University as an Associate Professor. Since 1996, he has been a Full Professor in the College of Electrical Engineering, Zhejiang University. He was the Director of the Power Electronics Research Institute and the Head of the Department of Applied Electronics, and he is currently the Vice Dean of the College of Electrical Engineering, Zhejiang University. He is the author or coauthor of more than 280 papers and one book *Theory and Applications of Multi-level Converters* (Beijing, China: China Machine Press, 2006). He holds 22 patents. His research interests include power electronics and their industrial applications.

Dr. He received the 1989 Excellent Ph.D. Graduate Award, the 1995 Elite Prize Excellence Award, the 1996 Outstanding Young Staff Member Award, and 2006 Excellent Staff Award from Zhejiang University for his teaching and research contributions. He received seven Scientific and Technological Achievements Awards from Zhejiang Provincial Government and the State Educational Ministry of China in 1998, 2002, 2009, and 2011, respectively, and six Excellent Paper Awards. He has been appointed as the IEEE Distinguished Lecturer by the IEEE Power Electronics Society in 2011. He is a Fellow of the Institution of Engineering and Technology (formerly IEE), U.K.