Gate Oxide Reliability Issues of SiC MOSFETs Under Short-Circuit Operation

Thanh-That Nguyen, Ashraf Ahmed, *Member, IEEE*, T. V. Thang, *Member, IEEE*, and Joung-Hu Park, *Senior Member, IEEE*

***Abstract*—Silicon-Carbide (SiC) MOSFETs, due to material properties, are designed with smaller thickness in the gate oxide and a higher electric field compared to Si MOSFETs. Consequently, the SiC MOSFETs have a worse reliability which causes higher leakage currents during instantaneous abnormal operating conditions. This paper investigates the reliability issues of the SiC MOSFET gate oxide under standard short-circuit test conditions. In this paper, 1200-V SiC MOSFETs are newly modeled, and also their short-circuit sustainability (tolerance) have been studied at different drain–source and gate–source voltages. A hardware tester circuit was designed and developed to test the devices under such extreme circuit conditions. Then, the gate reliability of SiC MOSFET devices have been compared to that of Si power devices of similar ratings. The results reveal a higher reduction in the instantaneous gate–source voltage of SiC MOSFETs compared to that of Si devices under the same operating conditions. The gate–voltage reduction phenomenon results from the higher leakage currents through the gate. Furthermore, it was found that the gate–source voltage reduction during the test depends on the gate structures. The gate voltage reduction of SiC MOSFETs with planar gate is higher than that of MOSFETs with shield planar gate. As the pulse duration increases in short-circuit tests, the leakage current in the gate-source of SiC devices increases. The results show that even though the SiC MOSFETs are very capable of processing long pulses and high power in the drain–source, the gate–source side is highly degraded by these pulses in the test. Moreover, whenever a small number of the short-circuit tests are applied, the gate structure of SiC MOSFETs becomes broken while the drain–source is still able to block the dc-link voltage. The paper concludes that the short-circuit reliability of the gate was found to be worse compared with commercial Si devices with similar rating.**

***Index Terms*—Gate leakage current, gate oxide reliability, SiC MOSFET, short-circuit test.**

I. Introduction

THE development of power semiconductor devices has always been a driving force for power electronic fields. For a long time, silicon-based power devices have dominated the power electronics semiconductor market and power system applications. Furthermore, silicon (Si) devices are widely used in the field of home appliance applications, power supplies, and information technology equipment. Therefore, the cost of Si MOSFETs has already stabilized with high operational reliability. However, market demands of higher voltage, power, and efficiency of emerging power electronic systems have been faced with performance limitation of Si material properties. SiC technology proposes a solution for many of the issues by superior material properties with regards to Si. After years of research on device physics and manufacturing technology, silicon-carbide (SiC) semiconductor devices for high-power applications have become commercially available as switching discrete devices such as Thyristors, JFETs, and MOSFETs [1]. The demand is strongly growing for these devices in high-voltage and high-temperature applications [2], [3]. SiC material offers a number of advantages compared to Si: SiC has ten times higher dielectric-breakdown field strength, three times the band gap, and three times the thermal conductivity [4]. These properties make SiC an attractive material that can far exceed the performance of their Si counterparts.

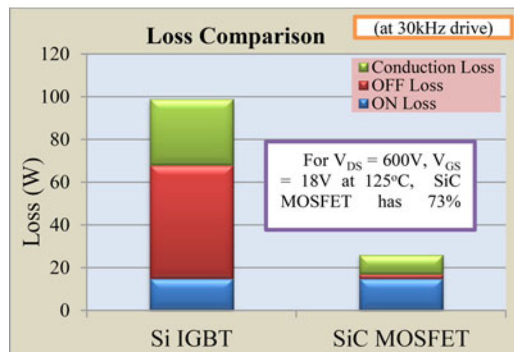

Fig. 1. Loss comparisons between Si IGBT and SiC MOSFET.

The main advantage of SiC is associated with the high electric field rating of the gate oxide. The high critical electric-field strength can be used to design very fast switching devices with much lower power losses than Si-based devices, for both conduction and switching losses, as shown in Fig. 1 [5]–[7]. Among the many papers discussing the switching characteristics under the maximum current and voltage stresses of SiC MOSFETs, some have dealt with high-frequency inverter circuits that employ SiC power devices to improve the efficiency and power capacity.

However, the reliability of SiC MOSFETs has not been verified fully under extreme operating conditions such as long time testing with higher temperatures, overload conditions, and short-circuit operations. Among these characteristics, short-circuit

Manuscript received April 1, 2014; revised June 16, 2014 and August 10, 2014; accepted August 14, 2014. Date of publication August 29, 2014; date of current version December 23, 2014. This work was supported by the Human Resources Development Program (20124010203160) of Korea Institute of Energy Technology Evaluation and Planning grant by the Korea Government Ministry of Knowledge Economy. Recommended for publication by Associate Editor T. M. Lebey.

The authors are with the Department of Electrical Engineering, Soongsil University, Seoul 156-743, Korea (e-mail: nguyenthanhthat777@gmail.com; ashraf_rshwan@yahoo.com; tranvietthang.utc@gmail.com; wait4u@ssu.ac.kr).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2014.2353417

capability of high-power switches is critical for fault protection and device failure prevention. The short-circuit test is a reliability standard test mandatory for high-power devices such as IGBTs [8]–[16]. This phenomenon happens in every switching converter or inverter during transient operating modes. The test allows data about capability of SiC MOSFETs under short-circuit operation to be obtained. These data provide key information about how to design the gate driver circuit for SiC MOSFET, which can limit the effects of short circuit on the devices and provide protection for the power circuit. Furthermore, in order to improve the reliability of the switching characteristics of SiC MOSFET, extreme operation should be discussed, such as overload turn-off, high-temperature operations, short-circuit conditions. These characterizations should be analyzed to assess realistic design limits, safety margins, and to highlight technology improvement requirements [10], [17].

Xing *et al*. [8] and [9] have discussed the effects on the current waveforms during short-circuit operation. Krishnaswami *et al*. [10]–[12] have presented gate oxide reliability assessment of SiC MOSFET under high-temperature operation. These papers have discussed the thermal effects on the gate oxide reliability, especially for long-time operation in normal conditions. However, the reduction in gate–source voltage during the short-circuit operation has never been presented in detail in these papers.

In this paper, the reduction on the gate–source voltage will be investigated during short-circuit condition for both SiC and Si power MOSFETs. A gate oxide reliability assessment for a “planar” SiC MOSFET structure under short-circuit operation will also be presented and compared to a “shield planar” SiC MOSFET structure.

The remainder of this study is organized as follows. Section II provides some background about the differences in physical structures and the operating principles between Si and SiC devices. It also presents the advantages and challenges of fabrication technology in SiC MOSFET, compared to Si devices. In addition, a comparison between gate oxide construction of planar SiC MOSFET and that of the shield planar will be proposed. The design process of the short-circuit tester and the operating principle will be presented in Section III. Section IV presents a theoretical study of SiC MOSFETs under short-circuit operation in PSIM simulation. Section V shows experimental results and some discussions about the effect on gate–source voltage under short-circuit conditions. These results will be compared to Si power devices. In addition, experimental results under short-circuit tests from two kinds of SiC MOSFET are presented. Finally, conclusions are given in Section VI.

II. BACKGROUND

A. Comparison of Planar SiC MOSFET With Si MOSFET

The electric field developed in the gate oxide is related to the electric field in the underlying semiconductor by Gauss’s Law [18]–[22]

$$E_{\text{oxide}} = \frac{\varepsilon_{\text{semi}}}{\varepsilon_{\text{oxide}}} E_{\text{semi}} \cong 3E_{\text{semi}} \tag{1}$$

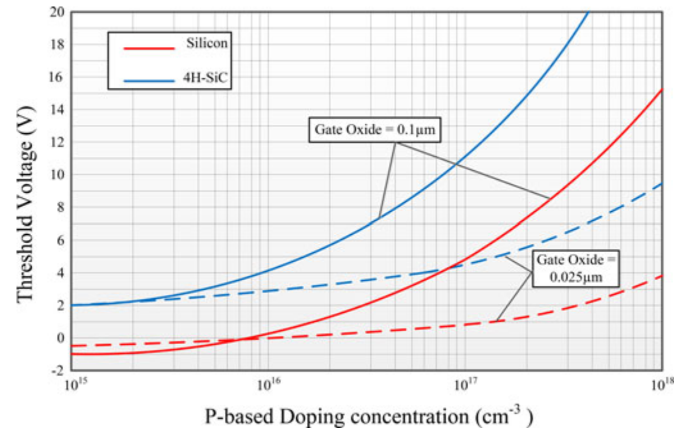

Fig. 2. Threshold voltage of SiC MOSFET compared to Si MOSFET (includes the impact of N^+ Polysilicon gate and an oxide fixed charge of 2×10^{11} cm^{-2}).

where $\varepsilon_{\text{semi}}$ and $\varepsilon_{\text{oxide}}$ are the dielectric constants of the semiconductor and the oxide, respectively, while E_{semi} is the electric field in the semiconductor. According to (1), the electric field in the oxide layer in case of silicon material is always in the reliability limit as silicon has maximum electric field of 3×10^5 V/cm. However, for silicon carbide devices, the maximum electric field is around ten times stronger than that of silicon-based devices. Therefore, the oxide could reach easily its reliability limits.

In planar MOSFET, when a drain–source voltage is applied, the maximum electric field occurs at the P-base/N-drift junction. The depletion width through the P-base region is related to the maximum electric field by

$$W_p = \frac{\varepsilon_{\text{semi}} E_m}{qN_A} \tag{2}$$

where N_A: doping concentration in P-base region, E_m: maximum electric field, and $\varepsilon_{\text{semi}}$: the dielectric constant. From (1), the doping concentration and P-base thickness are designed to prevent a P-base reach-through breakdown which is the cause of high-leakage currents on the gate. The threshold voltage is designed to keep the channel resistance as small as possible. Relationship of the gate oxide thickness with the threshold voltage and P-base doping concentration is presented in Fig. 2 [18]. For Si devices, for a P-base doping concentration of 10^{17} cm^{-3}, the threshold voltage is about 3 V, and the depletion width in the P-base region is less than 0.5 μm. As a result, a channel length less than 0.5 μm could be achieved without encountering reach-through breakdown limitations. Whereas, in case of 4H-SiC, to keep the P-base depletion width less than 1 μm, the doping concentration is around 3×10^{17} cm^{-3} when the electric field through the semiconductor approaches its critical value. With these conditions, the threshold voltage would reach as high as 20 V. However, the desirable value of the threshold voltage is around 6 V, so the gate oxide thickness is designed thinner. The thin layer can cause a reliability problem on the gate, especially when an extreme operating mode is applied such as a short circuit.

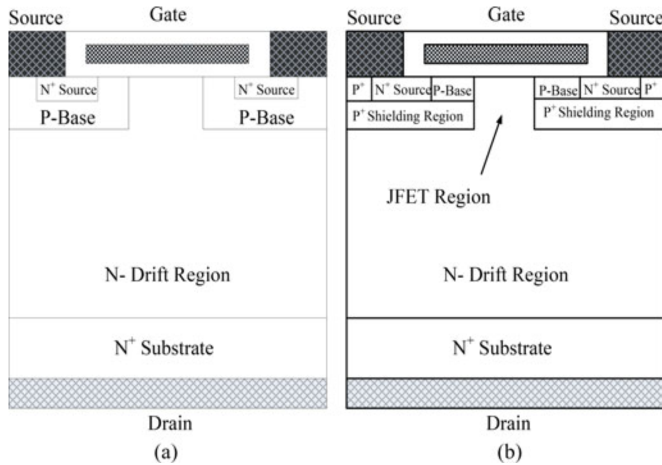

Fig. 3. Structures of Si and SiC MOSFETs (a) Planar MOSFET structure (b) Shield planar MOSFET structure.

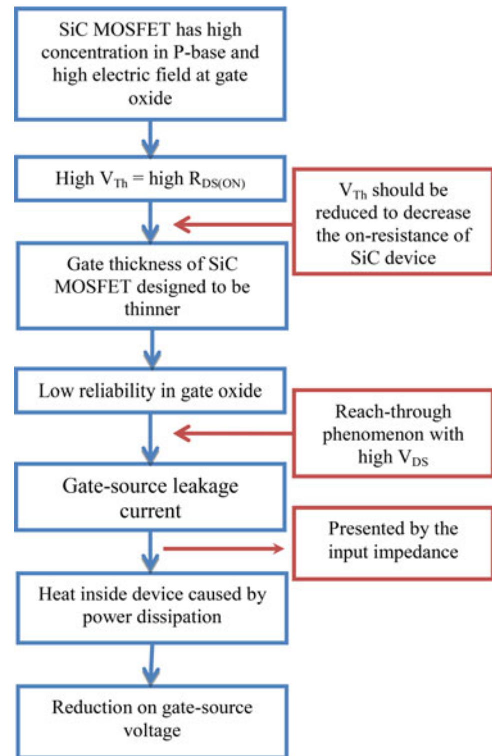

Fig. 4. Summary of the gate-oxide breakdown mechanism in short-circuit test.

B. Short-Circuit Operation

The short-circuit test, a standard regulation for the reliability of high-power devices, is performed with a positive voltage applied to the gate of the device under test (DUT). In order to make the tester circuit operate under the short-circuit conditions, the inductor should be set to very low value (see Fig. 5). Then, the MOSFET drain–source current reaches a very high value due to the high dI/dt ratios during the short-circuit test time, even just several microseconds. Almost spontaneously, the drain–source voltage drops down due to the potential through the inductance and recovers again to the input source voltage quickly. As a result, the temperature rising inside the device becomes quite severe due to the large power dissipation. As the temperature increases, the impedance inside the device also rise quickly, causing thermally negative feedback which acts to reduce the drain-to-source current.

C. Shield Planar MOSFET Structure

From the previous discussion, when a high-powered MOSFET drain–source voltage is applied, a gate-leakage reach-through phenomenon might happen, causing a gate reliability problem for the planar SiC MOSFET. The reach-through in MOSFETs can be reduced by shielding the channel against the high electric field developed in the drift region. The shielding is accomplished by the formation of either a P-type region under the channel or by creating a high-resistivity conduction barrier under the channel, which cannot be observed in planar Si MOSFET and planar SiC MOSFET, as referred in Fig 3(b). While Fig. 3(a) shows a planar MOSFET structure that represents both Si MOSFET and SiC MOSFET, which were discussed in Section II-A [18]. A potential barrier is formed when the JFET region becomes depleted with the applied drain bias. This barrier prevents the strong electric field from extending the effective area up to the gate oxide region. If the doping concentration of the shielding region is high, the reach-through breakdown problem discussed in the previous section can be limited.

D. Problem of Gate–Source Leakage Current During the Short-Circuit Operation

As aforementioned in Section II-A, the gate oxide thickness of SiC MOSFETs is thinner than that of typical Si MOSFETs. Furthermore, the electric field through the gate oxide is higher compared to typical silicon devices. During the short-circuit test, the device endures the whole dc source voltage with an excessive short-circuit current. Such increase in drain-to-source voltage leads to a high electric field at the P-base/N-drift region causing an increase in the depletion layer thickness in the P-base region. As a result, a reach-through phenomenon seems to happen causing a large leakage current to flow from the gate-to-source. The higher electric field inside and the smaller thickness of the gate oxide causes the leakage current to increase. The excessive increase in temperature during short-circuit operation would also increase the leakage current. Therefore, even with a small short-circuit pulse, the produced gate leakage current during the short-circuit operation will significantly reduce the reliability of the gate and the device. This paper proves that the reliability of the gate is affected by the operating condition, and also after a small number of short-circuit tests, the gate can be broken. According to the operating principles of the gate structure, the shield planar MOSFET is supposed to have a better performance and a higher reliability than conventional planar MOSFETs.

E. Summary of the Gate Reliability Degradation Mechanism

Summary of the breakdown mechanism investigated in this paper is presented in Fig. 4. The physical descriptions discussed

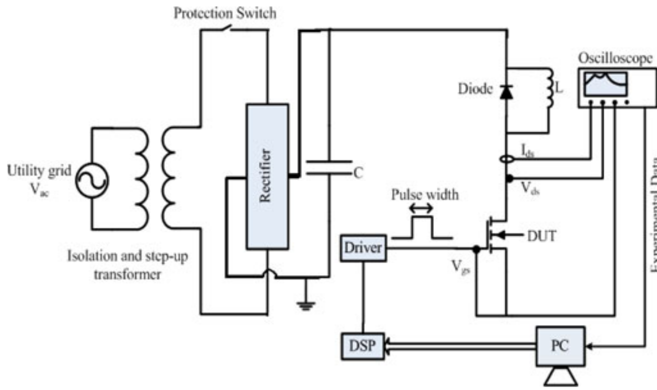

Fig. 5. High power clamped inductive load tester for a semiconductor power devices under test.

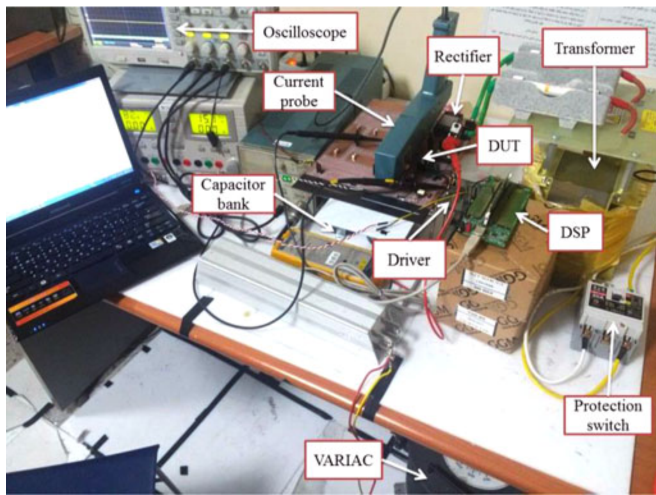

Fig. 6. Experimental setup.

in previous sections apply to the part from the beginning of the figure to the "gate–source leakage current." The remaining part will be mentioned in detail in following sections.

III. Description of the Experimental Setup

A. Construction of Tester

For the short-circuit test, a high-power clamped inductive load tester is used. Fig. 5 shows the high-power clamped inductive load tester for SiC semiconductor power devices. A 3.3-kV transformer is connected to the main grid through a variable ac voltage (VARIAC) to provide the ac power to the dc capacitor (C in Fig. 5). The VARIAC is used to manually control the voltage level. A high-power rectifier is connected to the secondary high-voltage terminal of the transformer to provide the required dc voltage level on the capacitor bank of 850 μF with a 1.6-kV rating. A TI28335 DSP controller is used to control the gate driver PWM signal. A protection switch is used to separate the power stage of the tester circuit from the electrical grid to prevent the circuit damage during the failure. An experimental setup photograph of the proposed tester is shown in Fig. 6.

B. Operation Principle of the Tester

The short-circuit test can cause the failure of the power semiconductor devices, especially when the circuit operates at high voltage, high current [1]. In fact, the test can induce a thermal failure on the DUT by the heat inside the devices during the short-circuit operation. Also, the devices can blow up due to overrating conditions in breakdown mode.

The test needs a preliminary procedure with the protection switch turn-on for charging-up the input capacitor. After a drain voltage is applied, the protection switch is turned OFF. Then, the gate driver provides a single pulse signal and the DUT turns ON with conducting a current in the loop of capacitor (C)—inductor (L)—DUT. After few microseconds of the pulsewidth, the DUT turns OFF [23], [24]. Actually, the inductance is very small less than 1 μH, thus the DUT suffers nearly short-circuit conduction between $V_{\rm dc}$ and the ground. Then, the input capacitor sustains the dc voltage against the huge short-circuit current as a charge buffer.

IV. Modeling and Simulation of SiC MOSFET

A. Modeling of Gate Drive Circuit

Fig. 7 shows the equivalent circuit of a general SiC MOSFET gate driver with small parasitic components. The gate drive IC is connected to 18-V dc power supply. A single pulse is given to drive the IC for the short-circuit test. This signal is delivered to the gate of SiC MOSFET. In this figure, the key measurement points for simulation are shown as $\rm I_{GS}$ and $\rm V_{GS}$ for the gate current and the voltage, respectively.

B. Modeling of the Tester for SiC MOSFET Under Short-Circuit Operation

In this section, input impedance model at the gate oxide is proposed to study the effect of the short-circuit operation on the gate of SiC MOSFETs, which is supposed to be less reliable than that of Si MOSFET from the analysis in previous sections. When the short circuit happens, it makes negative effects on the isolation of the gate oxide of the SiC MOSFET due to the extreme conditions. Actually, the hardware experiments show that the short-circuit condition causes a large gate–source leakage current, leading to the breakdown of the gate isolation. Fig. 8 shows the circuit diagram of the short-circuit tester with a proposed SiC MOSFET model. The gate drive circuit shown in Fig. 7 is used to provide the single pulse signal. In the SiC MOSFET model, the input impedance part is divided into two parameters of $\rm C_{GS}$, which means the gate isolation of the input resistance and the gate–source leakage current mentioned in Section II-C.

An equation is derived to model the effects of short-circuit bias on the input impedance of the device from the hardware test results (see figures in Section V). The gate–source voltage equation during the test is expressed as a function of the gate current as

$$v_{\rm GS} = -(53.64\,{\rm V/A})i_{\rm leak} + 18\,{\rm V} \tag{3}$$

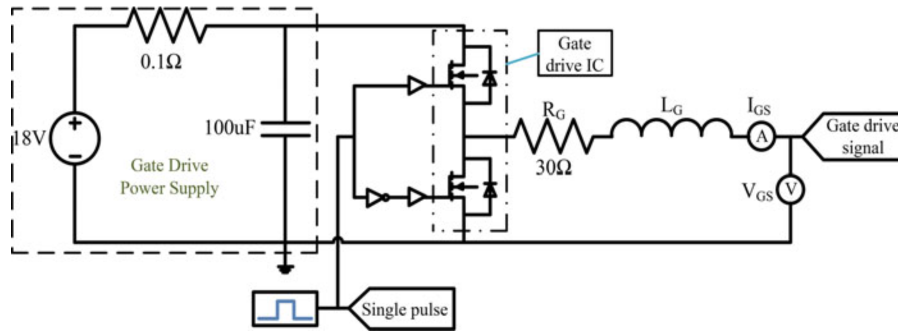

Fig. 7. Circuit model of the gate driver.

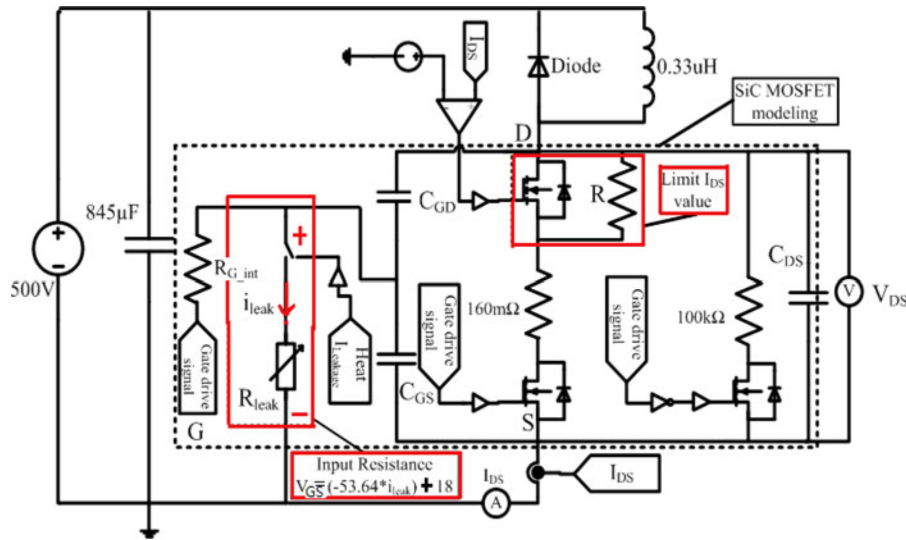

Fig. 8. Circuit diagram of the short-circuit tester with a proposed circuit model of the SiC MOSFET (DUT).

where $i_{\rm leak}$ is the leakage current flow through the input resistance, which presents the gate leakage effect and $v_{\rm GS}$ is the value of gate–source voltage, affected by $i_{\rm leak}$. From the equation, it can be seen that the gate impedance has a negative value, which means that the voltage and current are positive feedback to each other. This means that if a current disturbance triggers the voltage drop at the gate, then the voltage drop also induces a higher gate current, accelerating the effects of each other. For a new model, an extra drain–source resistance *R* is modeled to represent the drain–source current variation from the thermal effects during the test, exactly matching to the experimental results (see $I_{\rm DS}$ in Fig. 12), the value of *R* is set to 2.5 Ω.

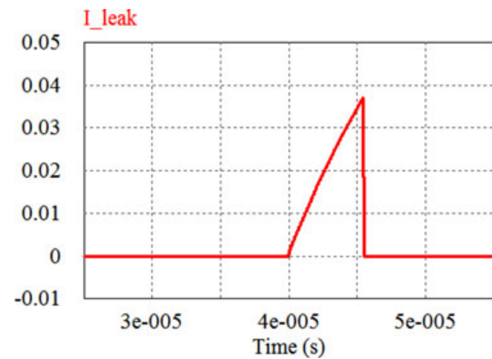

Fig. 9. Current flow through the input resistance simulated from the proposed circuit model.

C. Simulation Results

As proposed in above sections, the reach-through phenomenon can occur when a high-drain–source voltage is applied to the SiC MOSFET devices with a thin gate-oxide layer. Hence, the gate oxide can cause reliability issues when it operates under high-voltage stresses. The phenomenon is reflected in the input-impedance part of Fig. 8 as the input resistance is shunt-connected with $C_{\rm GS}$. From the model, when a high-drain–source voltage is applied, a gradually increasing current flow through input resistance of DUT, as shown in Fig. 9 (measured by $I_{\rm GS}$ in Fig. 7), is observed.

Fig. 9 shows the leakage current waveform conducting the input resistance of DUT ($I_{\rm GS}$ in Fig. 7). The current has a relationship with the gate–source voltage through the negative impedance characteristic [see (3)]. With the conduction time, the leakage current increases at the input resistance, causing a

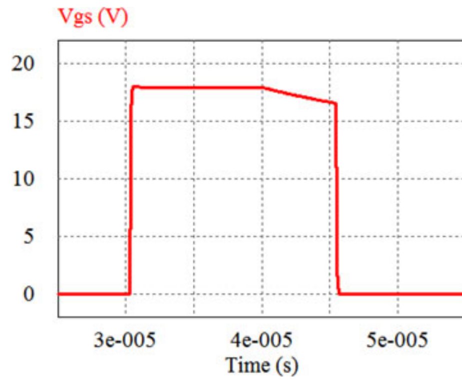

Fig. 10. Gate–source voltage reduction of SiC MOSFET in PSIM.

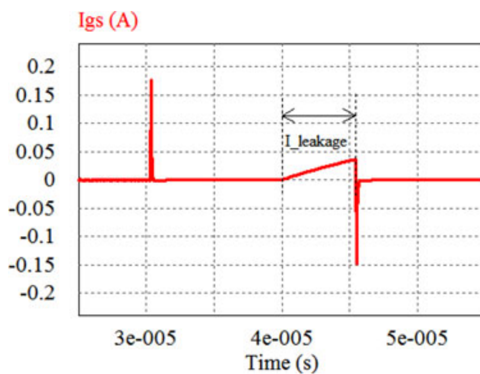

Fig. 11. Gate–source current of SiC MOSFET in PSIM.

significant voltage drop in the gate–source voltage, as shown in Fig. 10. This is an extraordinary phenomenon, which is supposed to be gate-isolation degradation, hardly seen in the tests of commercial Si MOSFETs. Using the leakage current in Fig. 9, the total gate–source current can be predicted through PSIM simulation, as shown in Fig. 11. Actually, the gate–source leakage current explains well the theoretical analysis discussed in Section II, and also it matches exactly with the hardware results given in following sections.

V. Experimental Results and Discussion

Three kinds of samples of a commercially available planar SiC MOSFET (CMF10120D) rated at 1200 V/24 A, a shield planar SiC MOSFET (SCT2080KE) rated at 1200 V/35 A, and a Si MOSFET (IXTK22N100L) rated at 1000 V/22 A were tested and compared under a variable 500-V dc-link voltage during short-circuit operation. The variation parameters for the tests are input dc voltage $V_{\rm dc}$ (equal to drain-to-source voltage V_{ds}), gate-to-source voltage $V_{\rm GS}$, and the pulsewidth of the single pulse. The test is carried out through the experimental tests by applying a single pulse and then the device was left for several minutes—hours, required to complete the heat sinking, before applying the next pulse. The pulsewidth is longer than the reliability standard range to accelerate the degradation.

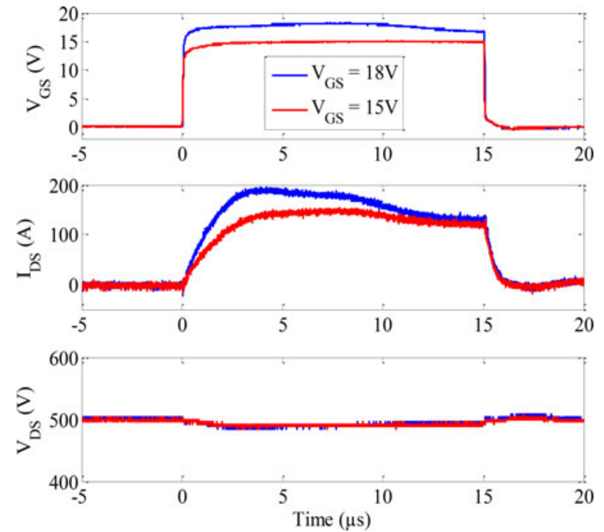

Fig. 12. Effect of $V_{\rm GS}$ for planar SiC MOSFET under short-circuit operation.

A. Comparison of the Reduction on the Gate–Source Voltage Between Planar Si and Planar SiC MOSFETs

Fig. 12 shows the drain–source voltage and current waveforms during the short-circuit operation for SiC MOSFET in the cases of $V_{\rm GS} = 15$ V and $V_{\rm GS} = 18$ V, $V_{\rm DS} = 500$ V, the pulsewidth $= 15\ \mu$s. According to discussion in Section II, when a short circuit happens, the drain current continuously increases and reaches the peak value about 150 A with $V_{\rm GS} = 15$ V at 4.3 μs, then it begins to reduce smoothly afterward. In spite of the large short current, the dc voltage ($V_{\rm DS}$) is maintained successfully by the charge buffer of the input capacitor. At higher gate voltage $V_{\rm GS} = 18$ V, the electric field under the gate oxide becomes stronger due to the higher electron–hole density in the channel, leading to an extension of the depletion layer. As a result, the peak current value increases and equals to 195 A at 3.7 μs from the rising edge of the single pulse. At $V_{\rm GS} =$ 18 V, the gate–source $V_{\rm GS}$ reduction is clearly observed during a time span from 10 μs to the falling edge. That is supposed to be caused by the negative resistance from the leakage current at the gate oxide (see (3)). The waveform agrees well with that of the SiC MOSFET model in Fig. 10.

Fig. 13 shows the gate–source voltage waveforms of a planar Si and a planar SiC MOSFETs during the short-circuit operation with variation of $V_{\rm GS}$. The pulsewidth is 15 μs. In case of Si MOSFET, the gate–source voltage sustains its initial value during the entire pulsewidth, even with the variation of $V_{\rm GS}$ from 15 to 18 V. In case of a planar SiC MOSFET, whereas, a gradual reduction on the gate–source voltage happens during the conduction. From the hardware results, it can also be seen that the increase of the gate–source bias leads to the clear failure of the constant gate voltage. One of the main factors intermediating between the parameter $V_{\rm GS}$ and the negative resistance effects is the heat generation inside the planar SiC MOSFET. As discussed in previous section, when the gate–source voltage increases, the drain–source current also increases as shown in Fig. 12, which causes the power dissipation increase inside the device. From

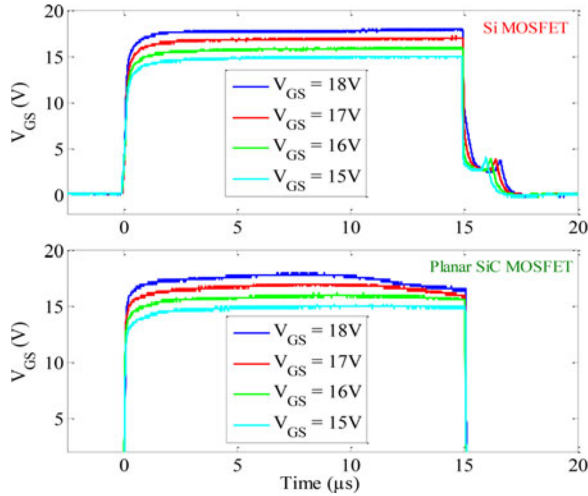

Fig. 13. Gate–source voltages of a Si and a planar SiC MOSFETs during the short-circuit test.

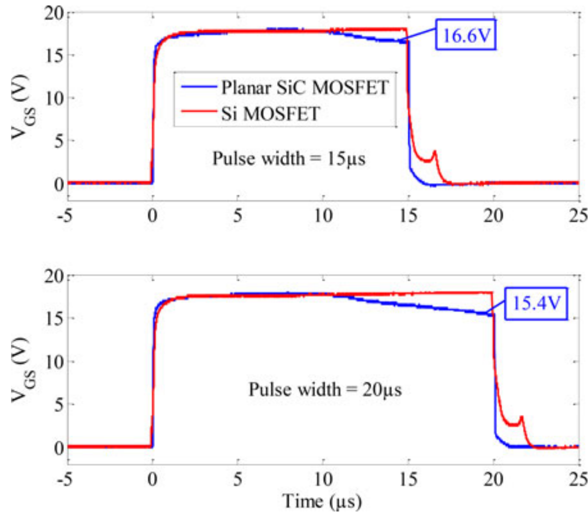

Fig. 14. Gate–source voltage waveforms of a Si and a planar SiC MOSFETs under the test with different pulsewidths.

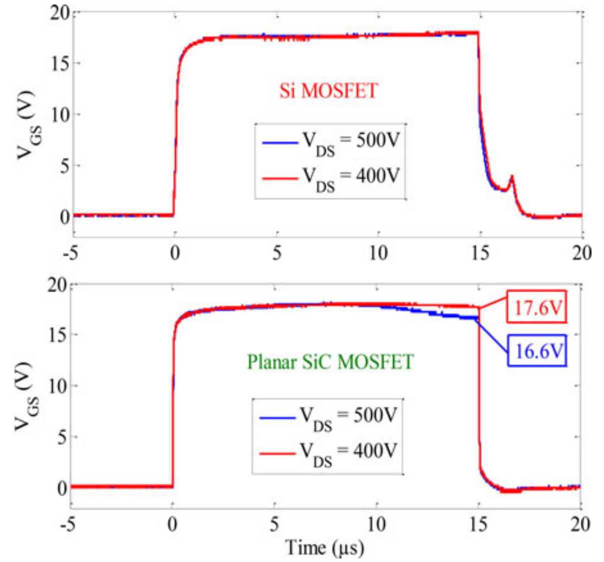

Fig. 15. Effects of V_{DS} on gate–source voltage of a Si and a planar SiC MOSFETs during the short-circuit test.

the temperature rising, the leakage current effect becomes more serious, and then the negative input impedance reduces the gate–source voltage in case of the planar SiC MOSFET. This effect will be analyzed more in detail in following sections.

Fig. 14 presents the waveforms when the single pulsewidth increased to 20 μs. The operating condition is $V_{\mathrm{DS}} = 500$ V, $V_{\mathrm{GS}} = 18$ V, $R_g = 30\ \Omega$. The reduction in gate–source voltage happens only in case of SiC MOSFET, not in Si, the same as the previous result. From the test, it can be seen that the reduction on V_{GS} starts at 10 μs and continuously decreases until the falling edge. Compared to the 15 μs pulsewidth, the 20 μs pulse has a more serious voltage reduction to from 16.6-V V_{GS} to 15.4 V. As a result, the increase of the short-circuit state induces more serious voltage reduction as expected.

Fig. 15 presents the effects of drain–source voltage on the reduction of gate–source voltage for the case of planar SiC MOSFET under short-circuit operation. In this test, the short circuit is performed with a variation of V_{DS} at the gate–source voltage $V_{\mathrm{GS}} = 18$ V, $R_g = 30\ \Omega$, and single pulsewidth equal to 15 μs. When the drain–source voltage decreases from $V_{\mathrm{DS}} = 500$ V to $V_{\mathrm{DS}} = 400$ V, the reduction in gate–source voltage becomes slightly relieved from 16.6 V V_{GS} to 17.6 V. This phenomenon is caused by the reduction of the power dissipation with change of the drain–source voltage. The thermal stress reduction from the small dissipation attenuates the negative-impedance effect as aforementioned in spite of the same value of the peak drain–source current in the cases.

As for the comparison between Si and SiC MOSFETs, since the gate oxide of SiC MOSFET is thinner than Si, the reach-through phenomenon happens more seriously when the same drain–source voltage is applied, causing a greater gate–source leakage current. This current affects the reliability of the gate, significantly presenting a reduction of the gate–source voltage through the negative impedance. In Si MOSFET, the reduction in gate–source voltage is negligible even when the value of drain–source voltage is changed under short-circuit operation.

B. Comparison the Reduction on Gate–Source Voltage Between "Planar" SiC and "Shield Planar" SiC MOSFETs

From the previous results, it is known that planar SiC MOSFETs have a negative resistance effect from the smaller gate thickness which would affect gate reliability. A further investigation for this phenomenon is performed with a shield planar SiC MOSFET in this section.

Fig. 16 presents the reduction in gate–source voltage of a planar SiC MOSFET compared to a shield planar SiC MOSFET. The operating condition is $V_{\mathrm{DS}} = 500$ V, $V_{\mathrm{GS}} = 18$ V, $R_g = 30\ \Omega$, and the pulsewidth $= 15\ \mu$s. As a result, the voltage reduction of the planar SiC and the shield planar SiC MOSFETs equals to 1.4 and 0.4 V, respectively, under the same conditions. The reduction in gate–source voltage of the shield planar SiC MOSFET is lower than the planar SiC MOSFET. This

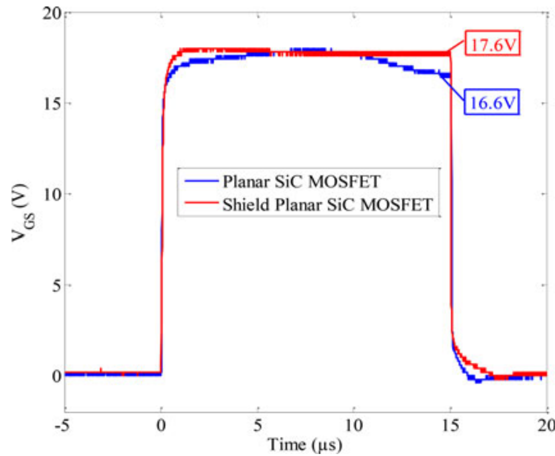

Fig. 16. Reduction in gate–source voltage for planar SiC MOSFET and Shield planar SiC MOSFET.

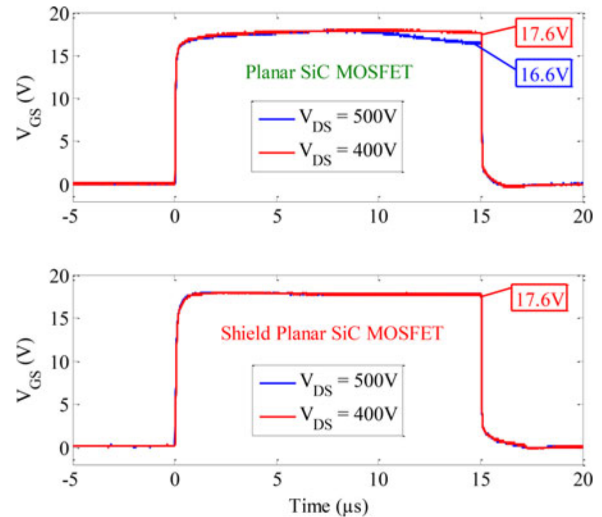

Fig. 17. Comparison of the effect of the bias V_{DS} on the reduction of gate–source voltage between a planar SiC MOSFET and a shield planar SiC MOSFET.

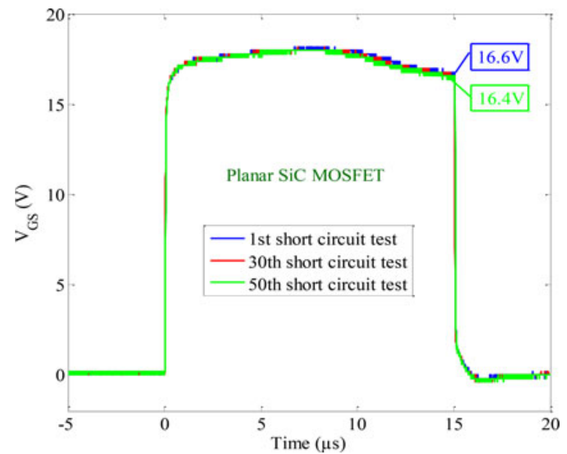

Fig. 18. Gate–source voltage characteristic of planar SiC MOSFET during multiple short-circuit tests, $V_{\mathrm{DS}} = 500$ V.

phenomenon happens due to the difference in the structure of the gate oxide of SiC MOSFETs, as per previous discussion in Section II-D. The shield planar SiC MOSFET has a shielding gate oxide layer, which makes the gate of shield planar more reliable than that of the planar SiC MOSFET. In addition, the shielding structure can limit the reach-through phenomenon which substantially causes the leakage current and more serious gate–source voltage reduction for planar SiC MOSFETs. Due to the reach-through limitation of the shielded MOSFET, the leakage current can affect the gate reduction less than the case of planar SiC MOSFETs.

However, since the shield planar SiC device also has a thinner gate oxide layer than that of Si devices, it can be concluded that the reduction in gate–source voltage still remains from the inherent gate structure (thickness) of shield planar SiC MOSFETs, even though the effect is attenuated much. As per previous discussion, the reduction in the gate–source voltage is triggered by the effect of the heat accumulated inside SiC MOSFETs. Thus, from all the statements and results above, it can be summarized that SiC MOSFETs have a vulnerable gate structure to the thermal effects resulting from the short-circuit test.

A further experimental result is shown in Fig. 17, which is obtained with the variation of V_{DS}. Still the reduction at 400-V bias remains as much as that of 500-V case in the shield planar MOSFET.

C. Device Degradation

There have been several papers discussing the reliability issues of the SiC MOSFETs [24], [25] under normal operating conditions. They introduce many degradation mechanisms under the normal condition, such as tunneling into and through gate oxide, stacking faults mechanism, so on. This paper proposes degradation phenomenon of SiC MOSFETs under short-circuit operation.

Permanent device degradation can be observed after several short-circuit tests. Fig. 18 exhibits the gate voltage characteristics of a planar SiC MOSFET during multiple short-circuit tests. The DUT is switched up to 500-V dc voltage with 18-V gate bias voltage and single pulsewidth equal to 15 μs. From the figure, it can be seen that the gate–source voltage slightly decreases after 50 short-circuit tests. For the first short-circuit test, the gate–source voltage drops to 16.6 V, and after the 50th short-circuit test the gate–source voltage drops to 16.4 V. Since the reduction in gate–source voltage is caused by the gate leakage current, the voltage reduction is closely related to gate oxide defects. After a number of short-circuit tests, the degradation becomes clear at the gate of the SiC device by the accumulation of defects. This permanent degradation can be explained by tunneling into and through gate oxide as mentioned above. As mentioned in previous sections, the SiC MOSFETs are designed with small gate oxide thickness and that causes high electric field across the oxide. When a positive bias is applied to the gate, due to the small oxide thickness, which results in a small width of the potential barrier, the electrons at the strongly inverted surface can tunnel into or through the SiO_2 layer. As a result, the gate oxide tunneling leakage current appears. The tunneling

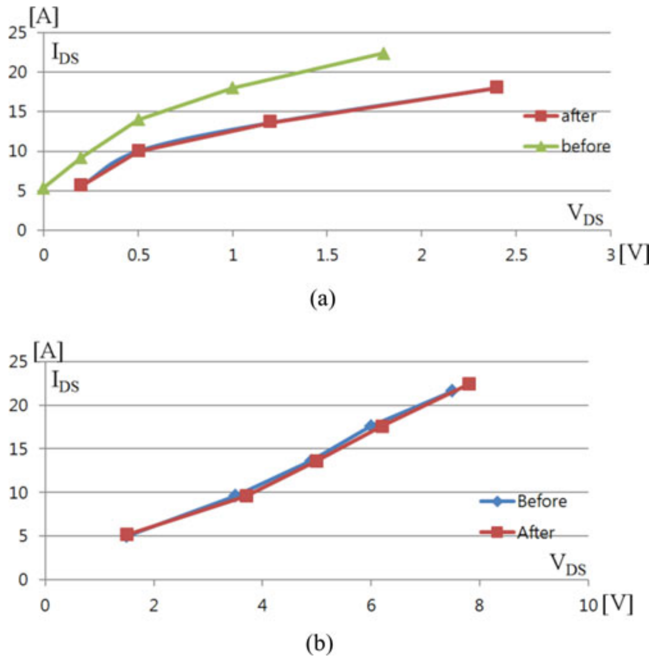

Fig. 19. Comparison of the $V_{\rm DS} - I_{\rm DS}$ characteristic curves before and after the short-circuit test ($V_{\rm GS} = 20$ V, 20 times short-circuit tests with 8 μs pulse). (a) Planar SiC MOSFET. (b) Si MOSFET.

mechanism between substrate and gate polysilicon can be divided into two parts, namely: Fowler–Nordheim tunneling and direct tunneling. More explanation for these two kinds of tunneling is proposed in [26]. The resulting leakage current affects the isolation of the gate oxide causing the gate degradation during short-circuit operation.

A further experiment was performed to investigate the effect of short-circuit operation on the normal operating characteristics. The drain–source voltage and current (*V–I*) curves of the SiC MOSFET have been sketched before and after the short-circuit tests [27], [28]. The experimental test results are shown in Fig. 19. This figure contains the drain–source resistance variation of the planar SiC and Si MOSFET before and after 20 times short-circuit tests. It can be seen that the variation of the Si MOSFETs are negligible, whereas the planar SiC MOSFET has a significant change in the *V–I* characteristics such as almost twice the resistance after a number of the short-circuit tests. The results show that planar SiC MOSFETs have a weaker short-circuit ruggedness compared to Si MOSFETs. The resistance increment can work as a positive feedback to the reliability of SiC MOSFETs through a thermal effect that have the higher resistance as the temperature increases.

A further experiment was done with a number of short-circuit tests for the gate reliability check. The result is shown in Fig. 20. This figure shows the gate–source voltage waveform of the planar SiC MOSFET before (blue curve) and after 50 times short-circuit tests (red curve). The key feature of the test is that the gate of SiC MOSFET operates with no dc bias on the drain–source, meaning a free running of the device away from any power (thermal) stress. It can be seen that, before the short-circuit tests, the gate–source voltage reaches 18 V fully (blue

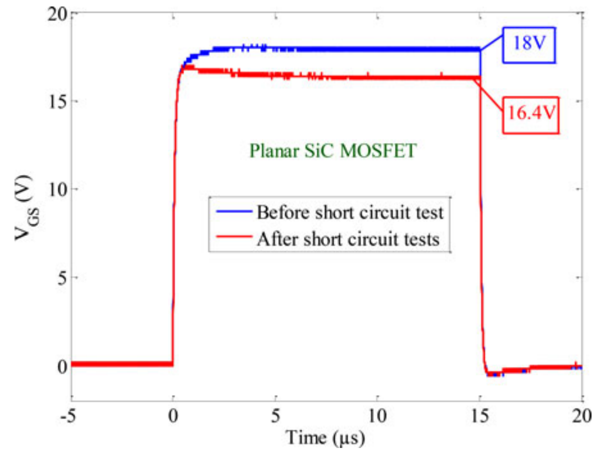

Fig. 20. Comparison of the gate of a planar SiC MOSFET before and after short-circuit tests without the input voltage.

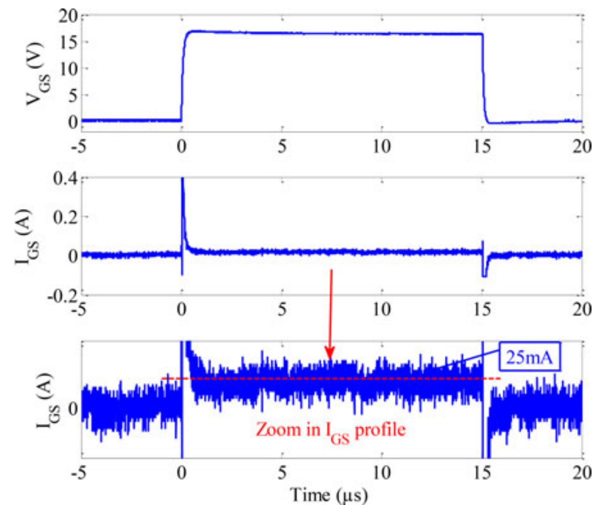

Fig. 21. DC current waveform at the gate of a planar SiC MOSFET sample having an experience of multiple short tests.

curve). Then, after several short-circuit tests, the plateau of the gate–source voltage sinks down to 16.4 V (red curve). The result means that the reliability of the gate structure of the device suffers a permanent change under the test. The influence can lead the destructive breakdown of MOSFET easily because the short-circuit condition occurs frequently in high-frequency switching operation of the switching power conversion circuits.

Finally, a hardware measurement with an aged device with a 50 times short-circuit test was attempted to directly detect the gate current. As shown in Fig. 21, a dc current injected into the gate is measured even under free-running with zero dc link voltage ($V_{\rm DS} = 0$ V). As aforementioned, the gate of SiC MOSFET cannot reach fully 18 V due to the degradation. The result shows that a dc current of 25 mA permanently flows through the gate. This means that the gate isolation has already been partially damaged, and the gate is already broken.

VI. Conclusion

Commercially available 1200-V/24-A planar SiC MOSFETs were tested for a short-circuit operation. The test results were compared to 1000-V/22-A Si MOSFET. Furthermore, another SiC MOSFET (Shield planar SiC MOSFET) was tested and compared to planar SiC MOSFET under extreme short-circuit conditions to accelerate the degradation. A proposed model and the simulation results of planar SiC MOSFETs were presented. These results have provided important information for the reliability estimation of SiC MOSFETs under the short-circuit condition. The experimental results have also shown a gradual reduction in $V_{\rm GS}$ in both cases of a planar and shield planar SiC MOSFETs, which is not shown with Si devices. This phenomenon is caused by the gate leakage current due to the smaller gate thicknesses of SiC MOSFETs, and then triggered by the high-power dissipation from the short-circuit condition, which results in lower reliability of the gate oxide.

In this study, a planar SiC MOSFET can withstand a short-circuit time of 15 μs at $V_{\rm GS} = 18$ V. After 30 repeated events of the short-circuit test, the device starts to degrade. When the single pulse is increased up to 20 μs, the gate of planar SiC MOSFET was totally broken by only one further short-circuit test. However, for a case of shield planar SiC MOSFETs, the gate was still alive with the same testing conditions. These different results are caused by the differences in gate oxide or doping structure of two kinds of SiC MOSFET. These results have shown that the gate reliability of SiC MOSFETs is not as good as that of Si MOSFETs, and also shown that some more methodology is necessary in fabrication technologies or in the driving circuit technology for the gate reliability improvement of SiC power devices. In future work, a number of devices will be tested to further investigate the average number of short-circuit tests before a permanent gate side breakdown occurs.

References

[1] C. Abbate, G. Busatto, and F. Iannuzzo, “Unclamped repetitive stress on 1200 V normally-off SiC JFETs,” *Microelectron. Rel.*, vol. 52, no. 9/10, pp. 2420–2425, Sep./Oct. 2012.

[2] W. Zhou, X. Zhong, and K. Sheng, “High temperature stability and the performance degradation of SiC MOSFETs,” *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2329–2337, May 2014.

[3] X. Zhong, X. Wu, W. Zhou, and K. Sheng, “An all-SiC high-frequency boost DC–DC converter operating at 320 °C junction temperature,” *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5091–5096, Oct. 2014.

[4] W. Guannan, Y.-C. Liang, and G. S. Samudra, “Realistic simulation on reverse characteristics of SiC/GaN p-n junctions for high power semiconductor devices,” in *Proc. IEEE 8th Int. Conf. Power Electron. ECCE Asia*, May/Jun. 2011, pp. 1464–1468.

[5] ROHM Semiconductor Company, 1200 V SiC MOSFETs [Online]. Available: http://www.rohm.com/web/global/sic-mosfet

[6] A. Merkert, T. Krone, and A. Merten, “Characterization and scalable modeling of power semiconductors for optimized design of traction inverters with Si- and SiC-devices,” *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2238–2245, May 2014.

[7] P. Ranstad, H.-P. Nee, J. Linner, and D. Peftitsis, “An experimental evaluation of SiC switches in soft-switching converters,” *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2527–2538, May 2014.

[8] X. Huang, G. Wang, Y. Li, A. O. Huang, and B. Baliga Jayant, “Short-circuit capability of 1200 V SiC MOSFET and JFET for fault protection,” in *Proc. IEEE 28th Annu. Appl. Power Electron. Conf. Expo.*, Mar. 17–21, 2013, pp. 197–200.

[9] A. Castellazzi, T. Funaki, T. Kimoto, and T. Hikihara, “Short-circuit tests on SiC power MOSFETs,” in *Proc. IEEE 10th Int. Conf. Power Electron. Drive Syst.*, Apr. 22–25, 2013, pp. 1297–1300.

[10] S. Krishnaswami, M. Das, B. Hull, S.-H. Ryu, J. Scofield, A. Agarwal, and J. Palmour, “Gate oxide reliability of 4H-SiC MOS devices,” in *Proc. 43rd Annu. Int Rel. Phys. Symp.*, Apr. 17–21, 2005, pp. 592–593.

[11] T. Santini, M. Sebastien, M. Florent, L.-V. Phung, and B. Allard, “Gate oxide reliability assessment of a SiC MOSFET for high temperature aeronautic applications,” in *Proc. IEEE ECCE Asia Downunder*, Jun. 3–6, 2013, pp. 385–391.

[12] L. C. Yu, G. T. Dunne, K. S. Matocha, K. P. Cheung, J. S. Suehle, and S., Kuang, “Reliability issues of SiC MOSFETs: A technology for high-temperature environments,” *IEEE Trans. Device Mater. Rel.*, vol. 10, no. 4, pp. 418–426, Dec. 2010.

[13] W. Hermansson, F. Chimento, and T. Jonsson, “Robustness evaluation of high voltage Press Pack IGBT modules in enhanced short circuit test,” in *Proc.IEEE. Energy Convers. Congr. Expo.*, Sep. 12–16, 2010, pp. 92–99.

[14] X. Zhuxian and F. Wang, “Experimental investigation of Si IGBT short circuit capability at 200 °C,” in *Proc. IEEE 28th Annu. Appl. Power Electron. Conf. Expo.*, Feb. 5–9, 2012, pp. 162–168.

[15] M. J. Barnes, E. Blackmore, G. D. Wait, J. Lemire-Elmore, B. Rablah, G. Leyh, M. N. Nguyen, and C. Pappas, “Analysis of high-power IGBT short circuit failures,” *IEEE Trans. Plasma Sci.*, vol. 33, no. 4, pp. 1252–1261, Aug. 2005.

[16] R. Pagano, Y. Chen, K. Smedley, S. Musumeci, and A. Raciti, “Short circuit analysis and protection of power module IGBTs.” in *Proc. IEEE 28th Appl. Power Electron. Conf. Expo.*, Mar. 6–10, 2005, vol. 2, pp. 777–783.

[17] W. Keiji, N. Shin-ichi, and O. Hiromichi, “Design and implementation of a non-destructive test circuit for SiC-MOSFETs,” in *Proc. 7th Int. Power Electron. Motion Control Conf.*, Jun. 2–5, 2012, vol. 1, pp. 10–15.

[18] B. Jayant Baliga. (2005). *Silicon Carbide Power Devices*. 1st ed. Singapore: World Scientific [Online]. Available: https://www.worldscientific.com

[19] Y.-C. Yeo, T.-J. King, and C. Hu, “MOSFET gate leakage modeling and selection guide for alternative gate dielectrics based on leakage considerations,” *IEEE Trans. Electron Devices*, vol. 50, no. 4, pp. 1027–1035, Apr. 2003.

[20] K. Y. Cheong, S. Dimitrijev, and Jisheng Han, “Investigation of ultralow leakage in MOS capacitors on 4H SiC,” *IEEE Trans. Electron Devices*, vol. 51, no. 9, pp. 1361–1365, Sep. 2004.

[21] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, “Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits,” *Proc. IEEE*, vol. 91, no. 2, pp. 305–327, Feb. 2003.

[22] G. Busatto, C. Abbate, F. Iannuzzo, and P. Cristofaro, “Instable mechanisms during unclamped operation of high power IGBT modules,” *Microelectron. Rel.*, vol. 49, no. 9–11, pp. 1363–1369, Sep.–Nov. 2009.

[23] A. Ahmed, A. Castellazzi, L. Coulbeck, and M. C. Johnson, “Circuit design and experimental test of a high power IGBT non-destructive tester,” *Microelectron. Rel.*, vol. 52, no. 11, pp. 2609–2616, Nov. 2012.

[24] A. Agarwal, H. Fatima, S. Haney, and R. Sei-Hyung, “A new degradation mechanism in high-voltage SiC power MOSFETs,” *IEEE Electron Device Lett.*, vol. 28, no. 7, pp. 587–589, Jul. 2007.

[25] R. Singh and Allen R. Hefner, “Reliability of SiC MOS devices,” *Solid-State Electron.*, vol. 48, no. 10/11, pp. 1717–1720, Oct./Nov. 2004.

[26] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, “Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuit,” *Proc. IEEE*, vol. 91, no. 2, pp. 305–327, Feb. 2003.

[27] M. Mudholkar, S. Ahmed, M. Nance Ericson, S. Shane Frank, C. L. Britton, Jr., and H. Alan Mantooth, “Datasheet driven silicon carbide power MOSFET model,” *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2220–2228, May 2014.

[28] G. Cao and H.-J. Kim, “A novel circuit for characteristics measurement of SiC transistors,” *J. Elect. Eng. Technol.*, vol. 9, no. 4, pp. 1332–1342, Jul. 2014.

Thanh-That Nguyen received the B.Sc. degree from the Department of Physics and Engineering Physics, University of Science (Vietnam National University-HoChiMinh City) in 2010. He also received the M.S degree in electrical engineering from Soongsil University, Seoul, Korea, in 2014.

His research interests include structure and characterizations of power semiconductor devices, apply to high power, high voltage applications.

T. V. Thang (M'14) received the B.S. degree from the University of Transport and Communication, Hanoi, Vietnam, in 2007, and the M.S. degree from the Department of Electrical Engineering, Soongsil University, Seoul, Korea, in 2013. He is currently working toward the Ph.D. degree at the Power Electronics Laboratory, Soongsil University, Seoul, Korea.

His research interests include the modeling, analysis and control of power converter.

Ashraf Ahmed (M'09) received the B.Sc. and M.Sc. degrees in electrical engineering from Assiut University, Assiut, Egypt, and Cairo University, Giza, Egypt, in 1999 and 2005, respectively. He received the Ph.D. degree from University of Durham, Durham, U.K., in 2011, in the field of renewable energy control and power electronics.

He is currently an Assistant Professor at Soongsil University, Seoul, Korea. His research interests include the analysis and design of switching power converters for renewable energy applications.

Joung-Hu Park (S'02–M'06–SM'13) received the B.S., M.S., and Ph.D. degrees from the Department of Electrical Engineering and Computer Science, Seoul National University, Seoul, Korea, in 1999, 2001, and 2006, respectively.

He is currently an Assistant Professor at Soongsil University, Seoul, Korea. His current research interests include the analysis of high-frequency switching converters and renewable energy applications.