A Fault-Tolerant Three-Phase Adjustable Speed Drive Topology With Active Common-Mode Voltage Suppression

Pawan Garg, *Member, IEEE*, Somasundaram Essakiappan, *Member, IEEE*, Harish S. Krishnamoorthy, *Student Member, IEEE*, and Prasad N. Enjeti, *Fellow, IEEE*

***Abstract*—A fault-tolerant adjustable speed drive (ASD) topology is introduced in this paper. A conventional ASD topology is modified to address: 1) drive vulnerability to semiconductor device faults; 2) input voltage sags; 3) motor vulnerability to effects of long leads; and 4) minimization of common-mode (CM) voltage applied to the motor terminals. These objectives are attained by inclusion of an auxiliary IGBT inverter leg, three auxiliary diodes, and isolation–reconfiguration circuit. The design and operation of the proposed topology modifications are described for different modes: 1) fault mode, 2) active CM suppression mode, and 3) auxiliary sag compensation (ASC) mode. In case of fault and sag, the isolation and hardware reconfiguration are performed in a controlled manner using triacs/antiparallel thyristors. In normal operation, the auxiliary leg is controlled to actively suppress CM voltage. For inverter IGBT failures (short circuit and open circuit), the auxiliary leg is used as a redundant leg. During voltage sags, the auxiliary leg, along with auxiliary diodes, is operated as a boost converter. A current-shaping control strategy is proposed for the ASC mode. A detailed analysis of CM performance of the proposed topology is provided, and a new figure of merit, CM distortion ratio (CMDR), is introduced to compare the attenuation of CM voltage with that of a conventional ASD topology. The output filter design procedure is outlined. A design example is presented for an 80 kW ASD system, and simulation results validate the proposed auxiliary leg based fault-tolerant scheme. Experimental results from a scaled prototype rated at 1 hp are discussed in this paper.**

***Index Terms*—Adjustable speed drive (ASD), CM distortion ratio (CMDR), common-mode (CM) suppression, fault-tolerant, voltage sag compensation.**

I. Introduction

A MOTOR drive system (MDS) consists of an adjustable speed drive (ASD), a motor, and the grid supply. The use of MDS is widespread in applications like water pumping stations, compressor, crusher, and steel rolling mills in petrochemical, cement industry, and steel industry [1]. In a number of these applications, MDS is integral part of a continuous process [2]. Any interruption of the manufacturing process is expensive because of production loss and follow-up costs [3], [4]. Therefore, the availability of MDS in such applications has an immense financial impact. This has triggered interest in failure modes of both ASDs and motors [1], [5]–[8]. Other power interruption phenomena like voltage sag/ swells have also been studied extensively [9]–[11]. These and other factors which affect the reliability of individual subsystems of an MDS are summarized in Fig. 1. A detailed review of these issues and existing solutions has been presented in this section.

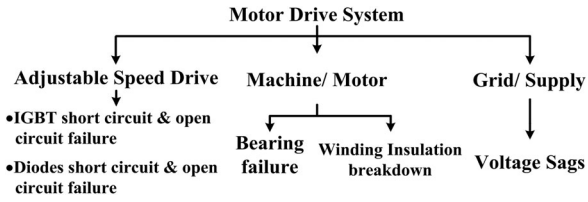

Fig. 1. Issues affecting MDS availability and reliability.

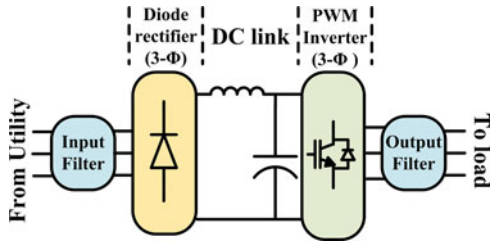

Fig. 2. Conventional ASD topology with input and output filter.

A. ASD Failure Modes

A conventional ASD topology is shown in Fig. 2. The failure modes of ASD have been studied in various surveys. According to [12], power semiconductor device faults account for about 35% of all ASD faults. In [13], up to 40% of the three-phase inverter failures in the field are attributed to power transistor failures. Other surveys have estimated that, of all components, power semiconductor device failures cause the most number of ASD failures [13].

Semiconductor Devices: Modern drives use highly integrated power modules which utilize different materials in their construction [14]. This leads to nonuniform thermomechanical stresses and consequently fatigue-induced failures [15]. Other

Manuscript received April 4, 2014; revised June 13, 2014 and August 14, 2014; accepted September 22, 2014. Date of publication October 14, 2014; date of current version December 23, 2014. Recommended for publication by Associate Editor Dr. D. O. Neacsu

P. Garg was with the Department of Electrical Engineering, Texas A&M University, College Station, TX 77843 USA. He is now with International Rectifier, El Segundo, CA 90245 USA (e-mail: pg978.iitkgp@gmail.com).

S. Essakiappan, H. S. Krishnamoorthy, and P. Enjeti are with the Department of Electrical Engineering, Texas A&M University, College Station, TX 77843 USA (e-mail: e.somasundaram@gmail.com; harishsarmak@gmail.com; enjeti@tamu.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2014.2361905

failure mechanisms for IGBT due parasitic BJT latch up, $V_{\rm CE}$ overvoltage breakdown due to high *dV/dt* spikes during turn off, and thermal breakdown have been discussed in [16].

Existing Solutions: A number of techniques have been proposed to detect [17]–[19] and mitigate effects of semiconductor device failures [20], [21] in voltage source inverters. A detailed review of published fault detection techniques is provided in [22] and fault-tolerant inverter topologies have been presented in [6] and [23]. Fault tolerance is typically achieved by introducing redundancy or added complexity. Among them three techniques are popular. First approach is to connect the faulty phase to dc link midpoint using triacs [24]. Second approach is to isolate the faulty phase and connect the motor neutral to the dc link midpoint [25]. A third approach is to introduce an additional leg which is connected to the motor neutral [26]. In all these cases, the semiconductor devices are oversized and the inverter output power during fault-mode operation is limited and the dc-bus capacitors need to be oversized. In the first and second approaches, access to dc bus midpoint is required, whereas the third approach handles only open-circuit faults and a fourth wire is needed, which adds to the cost. More recently, phase-redundant approaches [13], [27]–[29] have gained popularity due to 100% postfault output capabilities without drive overrating. A detailed cost and feature comparison of different fault-tolerant topologies is presented in [5].

B. Motor Failure Modes

Motor failures also affect the availability of an MDS. According to the data from commercial installations [8], bearing and winding failures together account for 70% of machine failures. High-frequency bearing currents contribute to bearing failures and large voltage overshoots result in winding insulation breakdown.

1) Motor Bearing Failures: A modern motor drive uses high-frequency PWM which results in high-frequency common-mode (CM) neutral-ground voltage. This voltage induces high-frequency motor bearing currents [30], [31], which gradually erode the bearing races [8], [32] and lead to early mechanical failures. Electrical grounding also plays a vital role in determining the magnitude and generation mechanism of bearing currents [33], [34].

Existing solutions: The existing solutions to the problems of bearing currents and CM voltage fall under one of the following two categories. First, the motor installation could feature: insulated or ceramic bearings, grounding brush contact and insulated coupling methods [34]. Additional filter components (*dV/dt* or sinusoidal output filters) can also be installed to modify the shape of inverter output. Second, modification to the inverter could be made, such as: a dual inverter bridge approach open winding [35], [36] and double winding machines [37]. Alternative approaches involving auxiliary inverter have been illustrated in [38], [39]. Another method proposed in [40] involves the use of an additional half bridge to actively cancel CM voltage.

2) Motor Winding: High-frequency PWM inverters with long lead cables can cause large voltage overshoots at the motor terminals. Magnetic wire insulation life curves shown in [41] illustrate the effect of increasing cable length and switching frequency. Prolonged voltage stresses lead to gradual deterioration of the insulation material and ultimately result in catastrophic failures.

Existing solutions: Three methods are widely used to mitigate the effect of high voltage stresses- inverter output reactors, inverter output filters [42]–[44] and cable termination filters [45]. The *dV/dt* limit is dependent on the length and electrical properties of the cable and reflection coefficient of the load. For instance, in [37] critical rise time is restricted to 2.5 μs for a 30 m cable. A review of different mitigation techniques has been presented in [46].

C. Grid Power Interruption

1) Voltage Sag: Based on power quality surveys [11] and standards [47]–[49], an input voltage drop by more than 13% and longer than one half cycle can lead to MDS trips. Although a trip protects the power electronic components during sag, it can lead to production loss [3], [4], [47], [49]. In continuous process industry applications, this could have a significant financial impact.

2) Existing Solutions: An overview of voltage sag compensation techniques has been presented in [50]. Hardware-intensive techniques such as auxiliary boost converter, a two-stage ac–dc conversion (diode rectifier followed by boost converter), pulsewidth-modulated (PWM) rectifier front end and energy-storage-based topologies use additional components [4], [50]. At the distribution level, dynamic voltage restorer (DVR) compensates for upstream disturbances using energy storage [51].

As discussed earlier, the factors affecting MDS failure modes (see Fig. 1) have been studied rigorously in the literature. Though a number of different solutions exist, which address these problems separately, none of the discussed approaches tackle all these issues with a single solution. In order to simultaneously address the issues of fault tolerance, CM voltage, overvoltage at motor terminal and grid voltage sags, a combination of approaches discussed in Section I-A–C is required, which makes the system design complex. This paper develops a single approach to mitigate all these factors by modifying a conventional drive topology.

The fault-tolerant nonregenerative AC MDS proposed in this paper is shown in Fig. 3. The topology consists of a three-phase diode rectifier (D1–D6) and auxiliary diodes (D7–D9) followed by a four-leg inverter ($S_{\rm 1A–D}$ and $S_{\rm 4A–D}$) along with isolation ($T_{\rm si}$ and $T_{{\rm fia}-d}$) and reconfiguration ($T_{\rm sr}$ and $T_{{\rm fra}-d}$) circuits for sag and fault-mode operations. During normal operation the fourth leg, hereby known as auxiliary leg ($S_{\rm 1D}$ and $S_{\rm 4D}$), is coupled to the conventional three-phase inverter topology using the output filter. This auxiliary leg enables active CM suppression by imposing a voltage at the inverter output, which is equal but opposite to the CM voltage magnitude. In grid phase voltage sag scenario, this auxiliary leg ($S_{\rm 1D}$ and $S_{\rm 4D}$) and diodes (D7–D9) form a boost converter to achieve sag compensation. For fault-mode operation, this auxiliary leg replaces the faulty leg after hardware reconfiguration. The output filter on

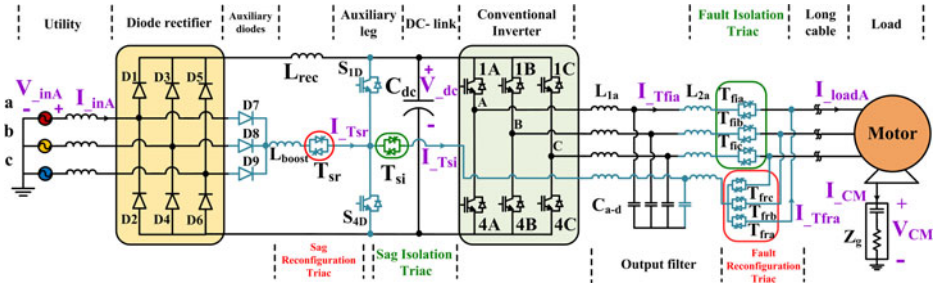

Fig. 3. Proposed fault-tolerant ASD topology with auxiliary leg (S_{1D}, S_{4D}) and diodes (D7, D8, D9), isolation (T_{si}, T_{fia}, T_{fib}, T_{fic}) and reconfiguration (T_{sr}, T_{fra}, T_{frb}, and T_{frc}) circuit.

the inverter side smoothens out *dV/dt* transitions, which reduces voltage overshoots at motor terminals. Thus, the proposed system reduces vulnerability to device faults, bearing currents, winding breakdown, and voltage sag. This system has various advantages:

1) a single auxiliary half bridge (S_{1D} and S_{4D}) performs multiple tasks: a) fault tolerance capability during open and short-circuit device faults, i.e., S_{1D} and S_{4D} along with T_{si}, T_{fib}, T_{fic}, T_{fra} (all on assuming inverter phase A is faulty); b) active CM suppression during normal operation: i.e., with S_{1D} and S_{4D} along with T_{fia}, T_{fib}, T_{fic} and T_{si} (all on); and c) sag compensation during voltage sags, i.e., with S_{1D} and S_{4D} along with T_{sr}, T_{fia}, T_{fib}, and T_{fic} (all on);
2) modular design of proposed fault-tolerant modifications and simple control strategy enables retrofit capability;
3) active CM suppression reduces the size of the CM filters;
4) operation at full-load even under fault conditions;
5) the inverter output filter reduces *dV/dt* at motor terminals for long motor leads;
6) use of antiparallel thyristors/triacs/solid-state relays allow fast and controlled system reconfiguration in case of faults and minimize conduction losses [52]. The choice of an appropriate device will depend on the power ratings and conduction loss performances of available options. Recently, reverse blocking bidirectional IGBTs were integrated into an IGBT module, which could also be an option in the future. Henceforth, the term "Triac" has been used for the sake of simplicity.

II. Proposed Topology

The design and operation of the proposed fault-tolerant ASD topology in Fig. 3 is covered in this section and may be best understood by studying it in four detailed sections: (A) fault-mode operation, (B) active CM suppression (ACMS) operation with modulation strategy and filter design, (C) auxiliary sag compensation (ASC) operation with current-shaping control strategy, (D) comparative CM voltage analysis for three-leg and four-leg modulation strategies. The state transition diagram for handover between different operating modes is shown in Fig. 4. It is noted that in postfault or ASC operation, ACMS is unavailable. The simulation and experimental results are discussed in the following sections.

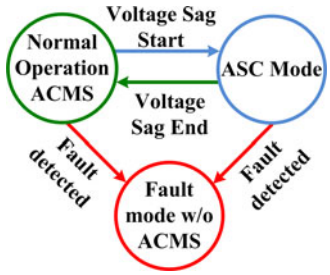

Fig. 4. State transition diagram for different operating modes.

A. Fault-Mode Operation

Fault-tolerant capability is added to a conventional ASD topology by introducing a redundant auxiliary leg (S_{1A} and S_{1D}). This provides fault tolerance in case of open and short-circuit failures of inverter IGBTs and antiparallel diodes. However, failures in the inverter IGBTs and antiparallel diodes—hereby called devices—are treated as the same in this discussion as they have similar effects on the inverter operation. Fault-tolerant operation includes three distinct steps: 1) fault isolation, 2) hardware reconfiguration, and 3) postfault control. The proposed topology implements these steps for both open and short-circuit device failures.

Typical device open-circuit fault detection time for a three-phase inverter is in the order of milliseconds [22]. Most of the published methods rely on sensing inverter phase currents and their deviation from normal operation to detect open-circuit faults. Recently, faster methods have been published, which use V_{CE} voltage of the low-side device to detect open-circuit fault [53]. Since the focus of this paper is not fault diagnosis, the detection time for open-circuit fault is taken to be 2 ms. For short-circuit failure a detection time of 4 μs is used, as modern gate drives employ schemes such as desaturation protection, which can complete fault detection in less than 5 μs [54]. Also, the open-circuit and short-circuit faults are discussed for IGBT S_{1A} only; however, the same discussion is applicable in case of failures in other devices.

The topology schematic in Fig. 3 has been simplified (see Fig. 5) for better understanding of failure mode operation for IGBT S_{1A}. First, the open-circuit device failure is discussed. During normal operation, triac T_{fia} (fault isolation triac for phase A) is turned on while T_{fra} (fault reconfiguration triac for phase A) is off. When a fault is detected, T_{fia}, T_{fra}, and all the inverter

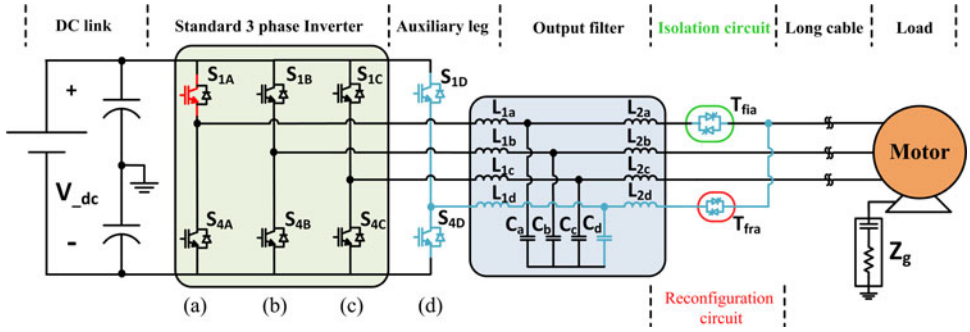

Fig. 5. Simplified schematic of the proposed topology to illustrate inverter switch $S_{1\mathrm{A}}$ failure ride-through.

switches are turned off. This is done to avoid any catastrophic transients. After a preset wait time of a few hundred microseconds, T_{fra} is turned on, and the gating signals of $S_{1\mathrm{A}}$ and $S_{4\mathrm{A}}$ are applied to $S_{1\mathrm{D}}$ and $S_{4\mathrm{D}}$, respectively. This completes reconfiguration and update of control strategy. The control of healthy legs (B and C) in postfault operation is unaltered.

The operation under short-circuit failure is similar to the earlier discussion, except for the fault detection time. As discussed before, the detection time for short-circuit faults is 4 μs. Once a short-circuit failure is detected, the desaturation protection turns off $S_{4\mathrm{A}}$ immediately, and controller temporarily turns off all other switches. The reconfiguration and postfault control strategy is same as the open-circuit failure case.

B. Active CM Suppression Operation

In a conventional three-phase sinusoidal PWM inverter, three switches are on at any time. This leads to a CM voltage on the output terminals at each time instant. With an even number of legs and with an appropriate switching strategy, it is possible to ensure that an equal number of output terminals are connected to positive and negative of the dc bus. So if higher order effects like dead-time and dc ripple are neglected, the CM voltage on the output terminals is zero at each instant. The CM suppression scheme proposed in [40] is based on this principle. This modulation strategy is used in the proposed topology.

1) Modulation Strategy: Different modulation schemes have been proposed to improve the CM performance of three-phase voltage source inverters [55]–[58]. The modulation strategy used in this paper is referred to as active zero state PWM (AZSPWM). In AZSPWM strategy, zero states of a conventional space-vector PWM are replaced with the nonadjacent nonzero vectors [59], [60]. This is illustrated in Fig. 6. AZSPWM contains the third-harmonic component, which introduces CM voltage on the output terminals; however, this low-frequency component has minimal effect on CM current. This generates the gating signals for three inverter legs. The gating signals for $S_{1\mathrm{D}}$ and $S_{4\mathrm{D}}$ are generated using logic equation given as follows:

$$S_{1\mathrm{D}} = S_{1\mathrm{A}} \oplus S_{1\mathrm{B}} \oplus S_{1\mathrm{C}} \tag{1}$$

2) Inverter Output Filter: The auxiliary leg is coupled to the three-phase inverter by using an output filter shown in Fig. 7. The output filter has two functions. Primary function of $L_{1a\text{–}d}$

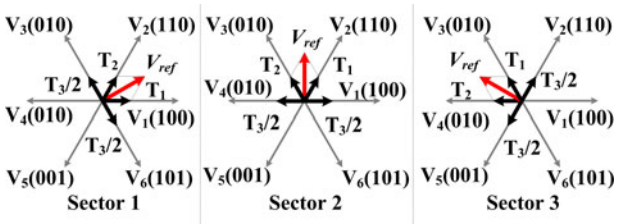

Fig. 6. Modulation strategy (AZSPWM) in sectors 1–3 (sectors 4, 5, and 6 are not shown).

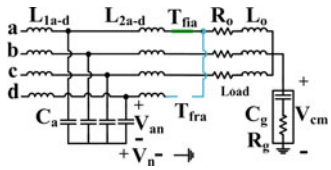

Fig. 7. Inverter output filter structure.

and $C_{a\text{–}d}$ is to attenuate the switching frequency (f_{sw}) harmonics and suppress CM voltage. As the higher frequency components are significantly attenuated, the effect of *dV/dt* on motor terminals is minimized [44]. If all the inductors $L_{1a\text{–}d}$ (L_f) and capacitors $C_{a\text{–}d}$ (C_f) are identical, it can be shown by mathematical analysis that CM voltages at the load neutral (V_{cm}) and is related to the filtered phase voltages. The transfer function is given by

$$V_{\mathrm{cm}} = \frac{4 \cdot (V_{an} + V_{bn} + V_{cn})}{3s^2 L_f C_g + 4(s^2 L_o C_g + s R_o C_g + 3)} \tag{2}$$

From (2), V_{cm} decreases when $(V_{an} + V_{bn} + V_{cn})$ is reduced. As the sum of filtered phase voltages tends to zero, the CM voltage will tend to zero. This can be achieved by balancing the phase voltage at fundamental frequency and filtering higher frequency switching harmonics.

The modulation scheme has been analyzed for calculating ripple current (see Fig. 8). The $I_{\mathrm{pk\text{–}pk}}$ ripple is maximum when the volt-sec applied across the inductor L_f is maximum [61]. This occurs when reference vector (V_{ref}) is aligned with V_1, i.e., $T_2 = 0$. Using the volt-sec balance principle, the peak-to-peak

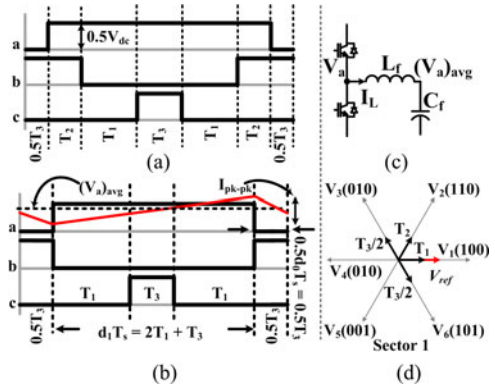

Fig. 8. Ripple current analysis for AZSPWM modulation scheme (a) switching in sector 1, (b) switching sequence when reference vector is aligned to V_1, (c) half-bridge representation with filter components, and (d) reference vector ($V_{\rm ref}$) aligned to V_1.

ripple current at switching frequency is given by

$$I_{\rm pk-pk} = \frac{d_0 d_1 V_{\rm dc}}{2 L_f f_{\rm sw}} \tag{3}$$

When the reference vector is aligned with V_1 and modulation index is maximum i.e., 1.15, then d_0 and d_1 are given by (4) and (5)

$$d_1 = 2 \times \left(\frac{0.866}{2} \times \frac{\sin(60^\circ - 0^\circ)}{\sin 60^\circ} \right) + \left(\frac{1}{2} - \frac{0.866}{2} \times \frac{\sin(60^\circ - 0^\circ)}{\sin 60^\circ} \right) \tag{4}$$

$$d_0 = \left(\frac{1}{2} - \frac{0.866}{2} \times \frac{\sin(60^\circ - 0^\circ)}{\sin 60^\circ} \right) \tag{5}$$

In order to remove switching frequency ($f_{\rm sw}$) harmonics, the value of filter components are chosen using the following:

$$\frac{1}{2\pi\sqrt{L_f C_f}} \leq \frac{f_{\rm sw}}{3} \tag{6}$$

Another factor to consider while designing the filter is the damping coefficient. The damping coefficient for series *RLC* circuit is given by (7). The value of $R_{\rm damp}$ is chosen to minimize overshoot and power loss

$$\zeta = \frac{R_{\rm damp}}{2} \sqrt{\frac{C_f}{L_f}} \tag{7}$$

The second function of the filter is to limit the current flow between two filter capacitors during transients. In case of a fault in $S_{1\rm A}$, during reconfiguration $T_{\rm fia}$ and $T_{\rm fra}$ are both ON for a brief period. Charge exchange between the faulty phase capacitor (C_a) and healthy auxiliary phase capacitor (C_d) takes place and inductors L_{2a}, L_{2d} limit this current transient. The worst-case voltage difference between the two filter capacitors ($V_{\rm dc}$) is used to choose the inductor value (L_2) for limiting this current *di/dt* transient

$$L_2 \frac{\Delta i}{\Delta t} = V_{\rm dc} \tag{8}$$

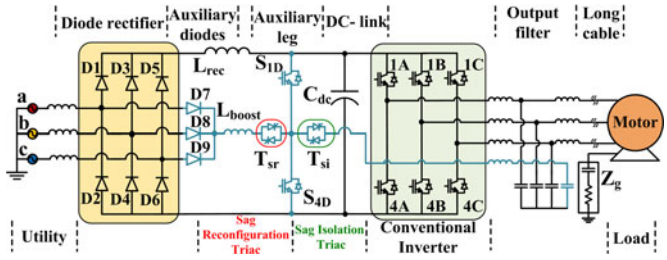

Fig. 9. Proposed topology simplified to emphasize sag compensation mode of operation. Components added for sag mode operation are highlighted in blue.

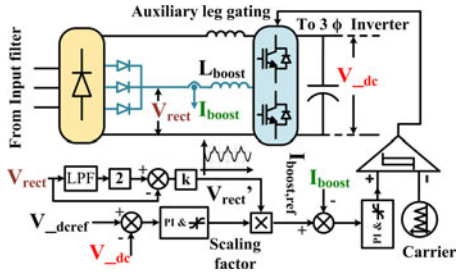

Fig. 10. Current-shaping-based control strategy for ASC-mode operation.

C. ASC Operation

In the proposed topology, sag ride through is achieved by integrating a boost converter in a typical ASD topology [9]. For better understanding of ASC operation, the proposed topology is simplified (see Fig. 9) to illustrate sag compensation. The components (in blue) added to implement ride through are three auxiliary diodes (D7, D8, D9), two triacs ($T_{\rm si}$ and $T_{\rm sr}$), and a boost inductor. The sag isolation triac ($T_{\rm si}$) disconnects the auxiliary leg from output filter. Sag reconfiguration triac ($T_{\rm sr}$) enables boost converter operation by connecting the auxiliary diodes to the midpoint of the auxiliary leg.

Input-line voltages are continuously monitored for detecting voltage sag. When a voltage sag is detected, $T_{\rm si}$ is turned off and $T_{\rm sr}$ is turned on. The front-end circuit is now reconfigured with two possible paths. In addition to the regular path through D1, D3, and D5, a secondary path is established through the integrated boost converter consisting of D7, D8, D9, boost inductor ($L_{\rm boost}$), $T_{\rm sr}$, $S_{1\rm D}$, and $S_{4\rm D}$.

A current-shaping control strategy (see Fig. 10) is proposed for the ASC mode operation. The conventional voltage and current control loops with PI controller are used. The reference dc-bus voltage ($V_{\rm \_dcref}$) is compared with the sensed dc-bus voltage ($V_{\rm \_dc}$). This error is the input to a PI controller which generates a scaling factor. The reference current shape $V'_{\rm rect}$ is obtained from the ASC rectified voltage ($V_{\rm rect}$) as shown in Fig. 10.

The LPF block in Fig. 10 extracts the dc component of $V_{\rm rect}$. This shape ($V'_{\rm rect}$) provides a current reference with a dc value superimposed on a low-frequency ac component. A factor of 2 allows this shape ($V'_{\rm rect}$) to represent an inverse of $V_{\rm rect}$ or the required boost inductor current shape behavior, i.e., when the voltage is low the boost current should be higher and vice versa. The boost inductor operates in continuous conduction mode.

TABLE I
SIMULATION PARAMETERS FOR COMPARISON OF SINE PWM AND AZSPWM STRATEGIES

Simulation Parameter	Value	Simulation Parameter	Value
Output Power	1 p.u.	Load	0.81 Ω, 1.04 mH
Output Line–Line voltage	1 p.u.	L_f, C_f	7 μH, 580 μF
Load power factor	0.9	$V_{\rm dc}$	1.633 p.u.

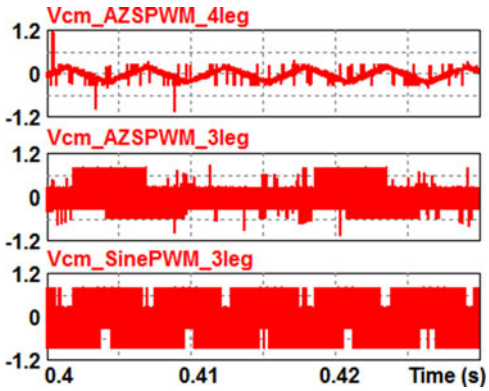

Fig. 11. Comparison of CM voltage for AZSPWM in four-leg and three-leg inverter and sine PWM in three-leg inverter.

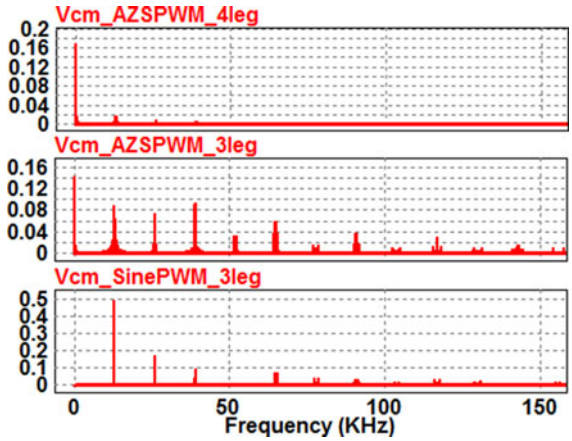

Fig. 12. FFT of CM voltage for AZSPWM in four-leg and three-leg inverter and sine PWM in three-leg inverter.

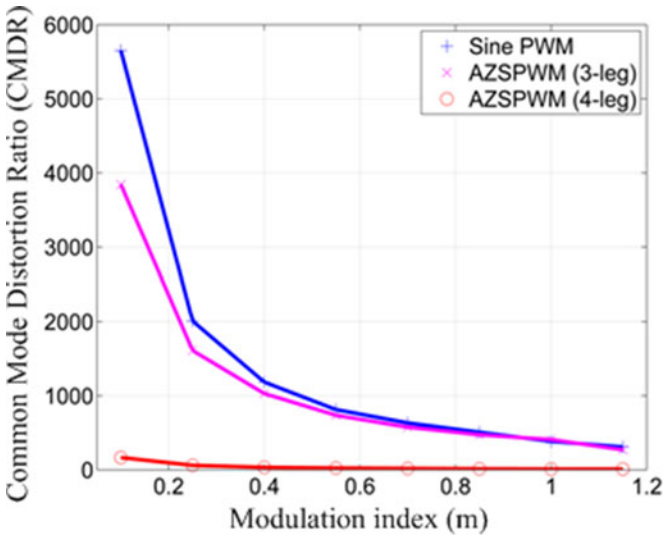

Fig. 13. Variation of CMDR with modulation index for Sine PWM (three-leg) and AZSPWM (three-leg and four-leg) strategies.

TABLE II
ONE HUNDRED HORSEPOWER THREE-PHASE INDUCTION MACHINE PARAMETERS

Motor Parameter	Value	Motor Parameter	Value
Power (in horsepower)	100	r_r (p.u.)	0.015
Stator line–line voltage	460 Vrms	X_{ls}	0.10 p.u.
Poles	4	X_{lr}	0.10 p.u.
Rated slip	0.0175	X_m	3.0 p.u.
r_s (p.u)	0.010		

TABLE III
PASSIVE COMPONENT VALUES SELECTED FOR SYSTEM SIMULATION

Line Side	Value	DC Bus	Value	Motor Side	Value
$Z_{\rm base}$	3.1 Ω	$Z_{\rm base}$	5.6 Ω	$Z_{\rm base}$	2.8 Ω
$L_{\rm in}$ (60 Hz)	0.25 mH (3%)	$L_{\rm rec}$	220 μH	L_{1a-d} (60 Hz)	40 μH (0.5%)
		$C_{\rm dc}$	15 mF	C_{fa-d} (60 Hz)	40 μF
		$L_{\rm boost}$	250 μH	L_{2a-d}	160 μH (2%)
				C_g, R_g	1 nF, 200 Ω

This shape is scaled to obtain the reference current. This reference is compared with $I_{\rm boost}$ to generate the error signal which is the input to a PI controller. The output of the PI controller is the duty cycle of $S_{4\rm D}$. The voltage $V_{\rm \_dcref}$ is chosen to be higher than dc-bus voltage under normal operation. This helps to reduce the input currents during transients as well as during ASC mode operation and enables lower device ratings.

D. CM Voltage Analysis for Three-Leg and Four-Leg Modulation Strategies

The AZSPWM strategy used in the proposed topology reduces CM voltage significantly. Sinusoidal PWM with conventional three-leg inverter, AZPWM with conventional three-leg inverter and AZPWM with four-leg inverter are simulated to compare the CM performance of these topologies. The system parameters are summarized in Table I. The filter parameters are chosen to achieve output power and line-to-line voltage of 1 p.u.

For modulation index $= 1$, the common voltages of three modulation strategies for the two studied topologies are shown in Fig. 11. It is evident that CM voltage is significantly reduced in case of AZSPWM (four legs). It is also observed that the higher frequency content of the CM voltage is reduced. The frequency spectra of the three waveforms shown in Fig. 12 clearly illustrate this. A new figure of merit called CM distortion ratio (CMDR) is introduced to compare the CM performance of these three strategies. CMDR defined in (9) is the square root of weighted sum of square of CM voltage, normalized to

TABLE IV
SUMMARY OF COMPONENT VOLTAGE AND CURRENT RATINGS

Device	Rating	Device	Rating	Device	Rating
Rectifier diode (D1–D6)	180 Arms (2 p.u.) 1200 V (4.33 p.u.)	$C_{\rm dc}$	1200 V (4.33 p.u.)	IGBT ($S_{1\rm A-D}$ to $S_{4\rm A-D}$)	1200 V (4.33 p.u.) 200 Arms (2.22 p.u.)
Auxiliary diodes (D7–D9)	180 Arms (2 p.u.), 1200 V (4.33 p.u.)	$T_{\rm si}$	200 Arms (2.22 p.u.) 600 V (2.22 p.u.)	L_{1a} to L_{1d}	200 Arms (2.22 p.u.)
$L_{\rm boost}$	180 Arms (2 p.u.)	$T_{\rm sr}$	180 Arms (2 p.u.) 600 V (2.16 p.u.)	L_{2a} to L_{2d}	200 Arms (2.22 p.u.)
$T_{\rm fia}$ to $T_{\rm fid}$	1200 V (4.33 p.u.) 200 Arms (2.22 p.u.)	$T_{\rm fra}$ to $T_{\rm frd}$	1200 V (4.33 p.u.) 200 Arms (2.22 p.u.)	C_{fa} to C_{fd}	≥600 V (2.16 p.u.) 100 Arms (1.11 p.u.)
$f_{\rm sw\_inv}$	13 kHz	$f_{\rm sw\_boost}$	10 kHz		

fundamental component of differential mode phase voltage

$$\text{CMDR} = \frac{1}{V_{\rm dm,1}}\sqrt{\sum_{h=1}^{\infty}(h\cdot V_{{\rm cm},h})^2} \tag{9}$$

The variation of CMDR is plotted (see Fig. 13) with varying modulation index for sinusoidal PWM strategy in three-leg inverter and AZSPWM strategy in four-leg and three-leg inverter. The figure of merit CMDR is helpful to compare the performances of different modulation strategies and their effects on CM currents. For better CM voltage performance, a lower CMDR value is desirable.

III. DESIGN EXAMPLE AND SIMULATION RESULTS

A. Design Example and Component Sizing

An 80 kW ASD system is designed for a 100 hp three-phase induction machine. The motor parameters are summarized in Table II.

The undervoltage lock out condition for the drive has been assumed to be 87% of the nominal dc-bus voltage. The drive input overcurrent limit has been taken to be two times the peak unfiltered input current ($I_{\rm \_inA}$) under regular operation. For the output current ($I_{\rm \_loadA}$), an instantaneous overcurrent limit of two times the peak load current is set to avoid nuisance tripping during fault transients. The input voltage to the drive is 480 V (line–line rms) and dc-link voltage ($V_{\rm \_dc}$) is 650 V. The values of different passive components are tabulated in Table III. The dc-bus capacitor ($C_{\rm dc}$) has been overrated to limit the input and output currents during faults. For Z_g, C_g has been calculated from the graph given in [31] and R_g is deduced from impedance measurements between shaft and frame on a motor using *LCR* meter.

The ratings for various devices are summarized in Table IV. All the ratings are based on $I_{\rm base,rms} = 90$ A and $V_{\rm base} = 480$ V . All devices have been derated accounting for increased current during full-load operation under sag condition. It is noted that if $L_{\rm rec}$ is split between the positive and negative buses, the required $L_{\rm boost}$ value is effectively reduced by $L_{\rm rec}/2$.

B. Simulation Results

The proposed topology was simulated for 80 kW ASD system with the parameters in Tables II and III. This discussion is divided into three parts: 1) fault-mode operation, 2) sag mode operation, and 3) CM performance. A description of current and voltage parameters, and device labels can be found in Fig. 3.

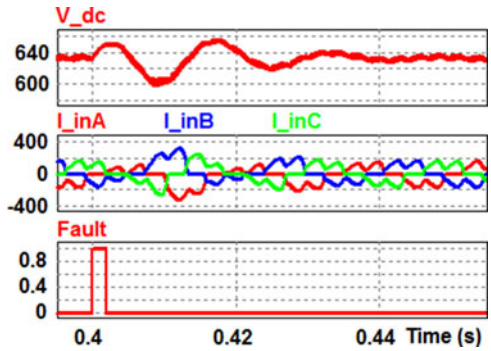

Fig. 14. Fault-mode operation under open-circuit fault introduced at $t = 0.4$ s. DC-bus voltage (in volts), unfiltered input currents (in amperes) and fault signal are shown.

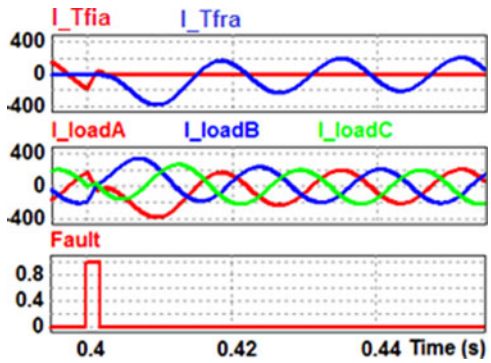

Fig. 15. Fault-mode operation under open-circuit fault introduced at $t = 0.4$ s. Isolation ($T_{\rm fia}$) and reconfiguration ($T_{\rm fra}$) triac currents (in amperes), load currents (in amperes) and fault signal are shown.

1) Fault-Mode Operation: The operation of the topology in fault mode was verified for the cases of open-circuit fault in $S_{1\rm A}$ (see Figs. 14 and 15) and short-circuit fault in $S_{1\rm A}$ (see Figs. 16 and 17). The rising edge of the "Fault" pulse in Figs.14–17 indicates the start of fault. The falling edge shows the completion of detection. The transient waveforms illustrate that the overcurrent and undervoltage performance of the topology are well within the defined specifications.

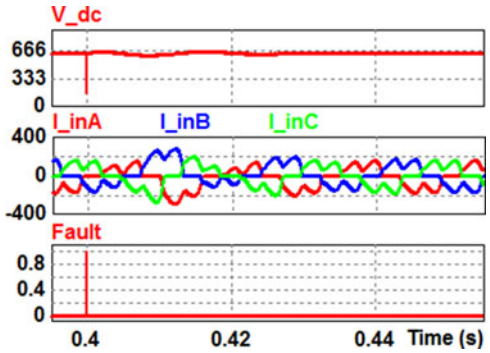

Fig. 16. Fault-mode operation under short-circuit fault at $t = 0.4$ s. DC-bus voltage (in volts), unfiltered line currents (in amperes), and fault signals are shown.

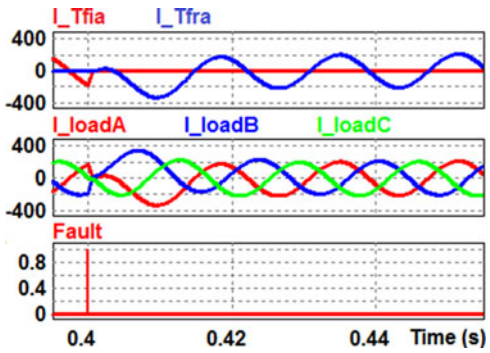

Fig. 17. Fault-mode operation under short-circuit fault at $t = 0.4$ s. Isolation ($T_{\rm fia}$) and reconfiguration ($T_{\rm fra}$) triac current (in amperes), load currents (in amperes) and fault signal are shown.

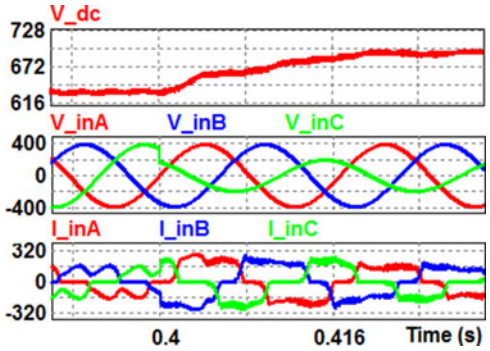

Fig. 18. ASC operation with phase to neutral sag of phase C to 50% introduced at $t = 0.4$ s. DC-bus voltage (in volts), line voltages (in volts), and unfiltered drive input currents (in amperes) are shown.

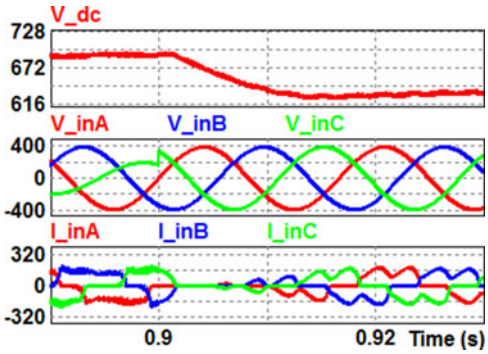

Fig. 19. ASC operation with phase C returning to normal operation at $t = 0.9$ s. DC-bus voltage (in volts), line voltages (in volts), and unfiltered drive input currents (in amperes) are shown.

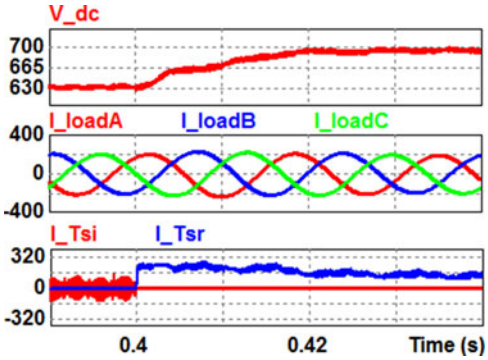

Fig. 20. ASC operation with phase to neutral sag of phase C to 50% introduced at $t = 0.4$ s. DC-bus voltage (in volts), load currents (in amperes), sag isolation ($T_{\rm si}$), and reconfiguration ($T_{\rm sr}$) triac currents (in amperes) are shown

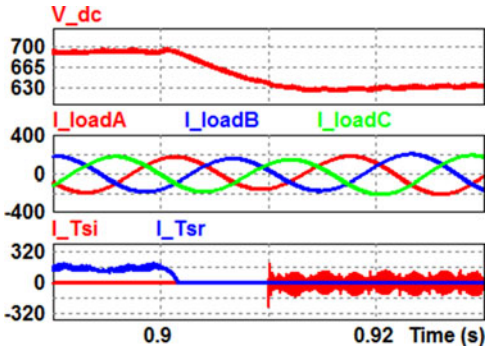

Fig. 21. ASC operation with phase C returning to normal operation at $t = 0.9$ s. DC-bus voltage (in volts), load currents (in amperes), sag isolation ($T_{\rm si}$), and reconfiguration ($T_{\rm sr}$) triac currents (in amperes) are shown.

The detection times for open-circuit and short-circuit faults are 2 ms and 4 μs, respectively. It is observed in Fig. 16 that the dc-bus voltage ($V_{\rm dc}$) falls below the undervoltage limit during a short-circuit fault transient. When the fault is detected, the gating signals to all the devices are turned off for a period of 10–20 μs. This period ensures that the controller can complete all diagnostic checks before returning to normal operation. It may be seen from Figs. 15 and 17 that following a fault, the ASD supplies nominal load current within two cycles (60 Hz).

2) ASC Operation: The ASC operation is studied for a phase to neutral sag to 50% and 500 ms long. When a voltage sag is detected, the auxiliary leg and auxiliary diodes are reconfigured to form a boost converter that supplies the dc link capacitor. The boost converter operates at a switching frequency of 10 kHz. The transient performance in ASC operation are shown in Figs. 18–21.

At $t = 0.4$ s, input phase C-to-neutral voltage sags to 50% of nominal value and at $t = 0.9$ s returns to nominal value. In sag

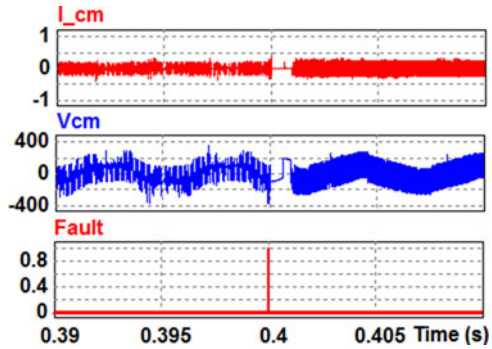

Fig. 22. CM current (in amperes) and voltage (in volts) before and after fault.

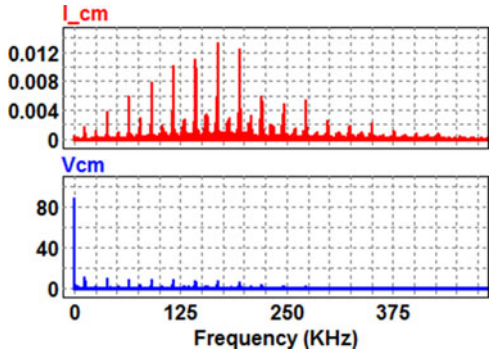

Fig. 23. CM current (in amperes) and voltage (in volts) frequency for normal operation.

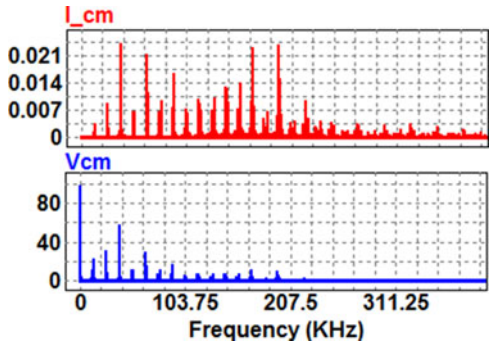

Fig. 24. CM current (in amperes) and voltage (in volts) frequency spectrum for postfault operation.

compensation operation, the dc bus is regulated at 690 V, i.e., approximately 7% higher than regular operation. This restricts the input and output current transients to within the overcurrent limit specified. It can be observed that the input current quality degrades during sag operation, but returns to normal under regular operation. It is to be noted that these currents discussed here are unfiltered input currents and the grid-side filtered currents are expected to be of much better quality.

3) ACMS Mode Operation: The state transition diagram discussed in Fig. 4 illustrated that the ACMS mode is the normal mode of operation in the absence of sags and faults. Fig. 22 shows the CM current and voltage in normal and fault-mode operations. It may be seen from the voltage waveform that

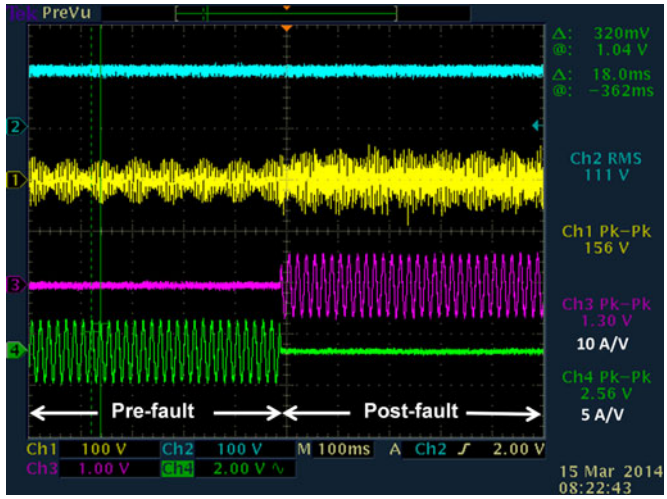

Fig. 25. Experimental result for open-circuit fault. Ch1: CM voltage at load neutral (V_{CM}), Ch2: dc-bus voltage ($V_{\_\mathrm{dc}}$), Ch3: T_{fra} current ($I_{\_T_{\mathrm{fra}}}$), and Ch4: T_{fia} current ($I_{\_T_{\mathrm{fia}}}$).

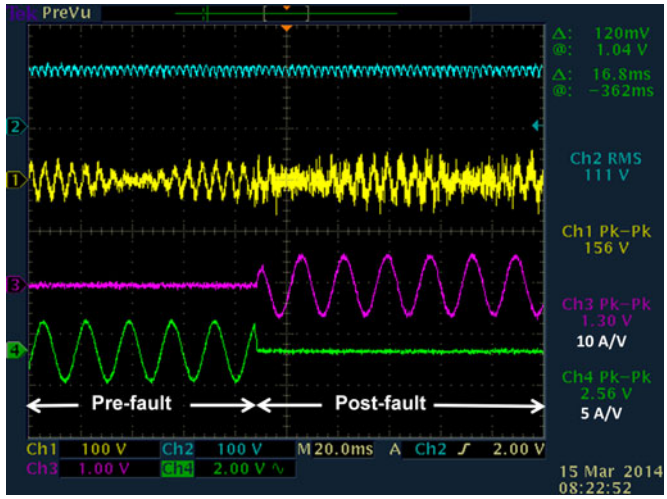

Fig. 26. Zoomed in waveforms for open-circuit fault, Ch1: CM voltage at load neutral (V_{CM}), CH2: dc-bus voltage ($V_{\_\mathrm{dc}}$), Ch3: T_{fra} current ($I_{\_T_{\mathrm{fra}}}$), and Ch4: T_{fia} current ($I_{\_T_{\mathrm{fia}}}$).

ACMS, under normal operation, attenuates switching frequency harmonics in the CM voltage. The normal and postfault CM current and voltage performances may be compared in Figs. 23 and 24. It is observed that high-frequency switching harmonics play a great role in determining the CM current magnitude.

IV. Experimental Results

The experimental results obtained for CM performance and fault-mode operation are discussed in this section. The open-circuit fault operation of the proposed topology is verified on a 1 hp rated experimental prototype constructed using Si-IGBT modules, with an *R–L* load standing in for the electric motor (power factor = 0.9). The control is implemented using TI TMS320F28335 microcontroller and ALTERA Cyclone II FPGA. For the implementation, random turn-on solid-state

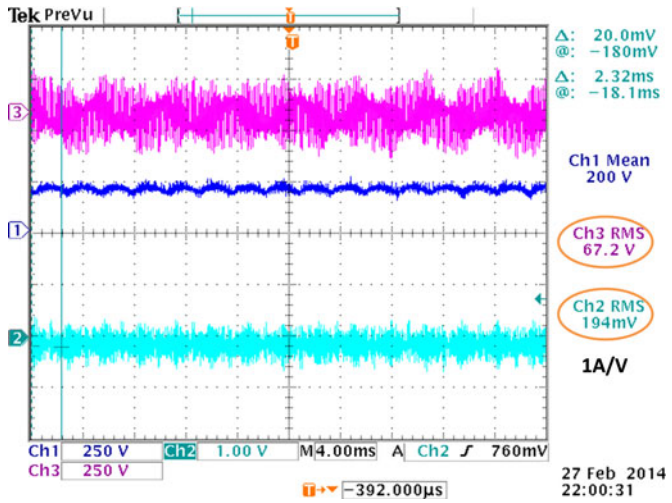

Fig. 27. CM performance in Sine PWM (three-leg). Ch1: dc-bus voltage ($V_{\_\mathrm{dc}}$), Ch2: CM ground current ($I_{\_\mathrm{CM}}$), Ch3: CM voltage at load neutral (V_{CM}).

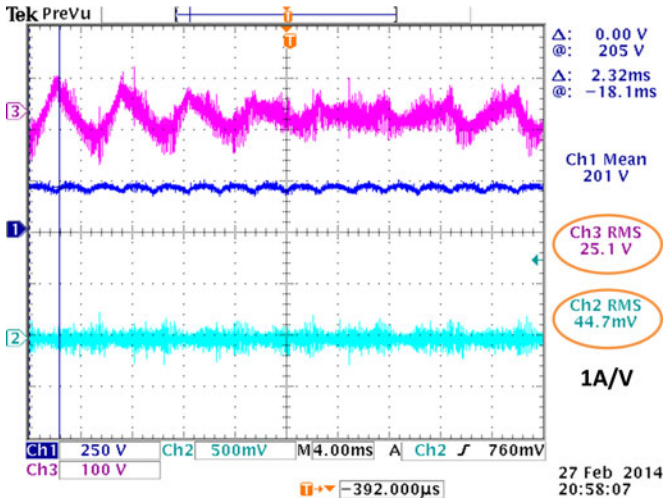

Fig. 28. CM performance in AZSPWM (four-leg) (scales different from Fig. 27). Ch1: dc-bus voltage ($V_{\_\mathrm{dc}}$), Ch2: CM ground current ($I_{\_\mathrm{CM}}$), and Ch3: CM voltage at load neutral (V_{CM}).

relays are used in place of triacs. A description of current and voltage parameters, and device labels can be found in Fig. 3.

The open-circuit fault is emulated by turning off the gating signal to $S_{1\mathrm{A}}$ at an arbitrary moment using an SPST switch on the FPGA board. After a detection time of 2 ms, hardware reconfiguration is activated by the controller, switching off triac T_{fia} and switching on triac T_{fra} to replace the faulty leg with the healthy auxiliary leg.

After a predefined wait period (100 μs), the gating signals for the remaining two unfaulted legs and the auxiliary leg are updated, and the inverter enters fault-mode operation. The operation of the system in open-circuit fault mode is shown in Figs. 25 and 26. In the case of a 100-hp practical system, the handover of output current from isolation traic (T_{fia}) to reconfiguration triac (T_{fra}) is expected to be slower. The waveform for dc-bus voltage ($V_{\_\mathrm{dc}}$), CM voltage (V_{CM}), triac T_{fra} current ($I_{\_T_{\mathrm{fra}}}$), and triac T_{fia} current ($I_{\_T_{\mathrm{fia}}}$) are shown.

It can be seen that the load current is transferred from triac T_{fia} (conducting prefault) to triac T_{fra} (conducting postfault), which demonstrates completion of the reconfiguration process. The beat frequency observed in the CM voltage is due to the difference (≈5 Hz) in inverter output fundamental frequency and grid frequency. In the prefault condition, the system operates in AZSPWM four legs with active CM voltage suppression. In the postfault operation, the active CM voltage suppression ability is lost and the system operates in AZSPWM three legs. It can be observed that CM performance degrades in the postfault condition, since the three-leg operation increases switching frequency harmonic components in the CM voltage.

The CM performances of the AZSPWM modulation strategy (four legs) and sinusoidal PWM (three legs) have been verified on the 1 hp rated experimental prototype. A dc-bus voltage of 200 V is used with a resistive load. A ground coupling capacitor (C_g) of 10 nF is used between load neutral and ground. The load neutral voltage and the ground current through coupling capacitor are shown in Figs. 27 and 28 for three-leg Sine PWM and four-leg AZPWM operation, respectively. As in previous results, the beat frequency observed in the CM voltage is due to the difference (≈5 Hz) in inverter fundamental frequency and supply frequency. It can be seen that there is a significant reduction in rms value CM voltage (∼60%) and ground current (∼80%) in the AZPWM case. As shown in the analysis Section II-D, there is a third harmonic component in CM voltage and high-frequency components have been significantly attenuated.

V. Conclusion

A fault-tolerant ASD topology for MDS was proposed in this paper to mitigate the effect of CM voltage, voltage sags, and device failures. An auxiliary inverter leg, three auxiliary diodes, and an isolation–reconfiguration circuit were added to a conventional ASD topology. The topology was discussed for three different modes of operation. The isolation and reconfiguration strategy for both voltage sags and device faults were described. Fault-mode operation was discussed for both open and short-circuit device failures. Once a failure was detected, the auxiliary leg was used to replace the faulted leg. A current-shaping control was proposed for the ASC mode. The CM voltage performance for the proposed topology was analyzed and it was verified that CMDR performance was superior for four-leg AZPWM for all modulation indices. Simulation results for a design example rated at 80 kW were presented for different modes of operation. Experimental results on a 1 hp system demonstrate the validity of the proposed auxiliary leg based system. The fault tolerance scheme was verified for open-circuit fault. A significant reduction in CM voltage of up to 60% and up to 80% reduction in ground current were achieved.

References

[1] S. Yantao and W. Bingsen, "Survey on reliability of power electronic systems," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 591–604, Jan. 2013.

[2] R. A. Epperly, F. L. Hoadley, and R. W. Piefer, "Considerations when applying ASDs in continuous processes," *IEEE Trans. Ind. Appl.*, vol. 33, no. 2, pp. 389–396, Mar./Apr. 1997.

[3] J. Douglas, "Power quality solutions," *IEEE Power Eng. Rev.*, vol. 14, no. 3, pp. 3–7, Mar. 1994.

[4] A. Von Jouanne and P. Enjeti, "ASD ride-through technology alternatives and development," Electric Power Res. Inst., Palo Alto, CA, USA, EPRI Final Rep., Dec. 1997.

[5] B. A. Welchko, T. A. Lipo, T. M. Jahns, and S. E. Schulz, "Fault tolerant three-phase AC motor drive topologies: A comparison of features, cost, and limitations," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 1108–1116, Jul. 2004.

[6] W. Zhang, D. Xu, P. Enjeti, H. Li, J. Hawke, and H. Krishnamoorthy, "Survey on fault-tolerant techniques for power electronic converters," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6319–6331, Dec. 2014.

[7] D. K. Kastha and B. K. Bose, "Investigation of fault modes of voltage-fed inverter system for induction motor drive," *IEEE Trans. Ind. Appl.*, vol. 30, no. 4, pp. 1028–1038, Jul./Aug. 1994.

[8] R. H. Charles, E. L. Walter, R. H. Charle, R. G. Smiley, V. B. Stewart, and J. K. Russell, "Reliability," *Handbook of Electric Motors*, vol. 120, 2 ed. CRC Press, 2004, pp. 655–691.

[9] J. L. Duran-Gomez, "New approaches to improve the performance of adjustable speed drive (ASD) systems under power quality disturbances," Ph.D. dissertation, Texas A&M Univ., College Station, TX, USA, 2000.

[10] J. L. Duran-Gomez and P. Enjeti, "A low cost approach to improve the performance of an adjustable speed drive (ASD) under voltage sags and short-term power interruptions," in *Proc. Conf. 13th Annu. Appl. Power Electron. Expo.*, 1998, pp. 587–591, vol. 2.

[11] J. L. Duran-Gomez, P. N. Enjeti, and W. B. Ok, "Effect of voltage sags on adjustable-speed drives: A critical evaluation and an approach to improve performance," *IEEE Trans. Ind. Appl.*, vol. 35, no. 6, pp. 1440–1449, Nov./Dec. 1999.

[12] Y. Chia-Chou and N. A. O. Demerdash, "Induction motor-drive systems with fault tolerant inverter-motor capabilities," in *Proc. IEEE Int. Electric Machines Drives Conf.*, 2007, pp. 1451–1458.

[13] R. R. Errabelli and P. Mutschler, "Fault-tolerant voltage source inverter for permanent magnet drives," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 500–508, Feb. 2012.

[14] J. Bing, V. Pickert, C. Wenping, and B. Zahawi, "In situ diagnostics and prognostics of wire bonding faults in IGBT modules for electric vehicle drives," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5568–5577, Dec. 2013.

[15] M. Ciappa, "Selected failure mechanisms of modern power modules," *Microelectron. Rel.*, vol. 42, pp. 653–667, 2002.

[16] W. Rui, F. Blaabjerg, W. Huai, M. Liserre, and F. Iannuzzo, "Catastrophic failure and fault-tolerant design of IGBT power electronic converters—An overview," in *Proc. 39th Annu. Conf. IEEE Ind. Electron. Soc.*, 2013, pp. 507–513.

[17] J. Zhang, J. Zhao, D. Zhou, and C. Huang, "High performance fault diagnosis in PWM voltage-source inverters for vector controlled induction," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 1–1, Nov. 2014.

[18] Y. Shaoyong, X. Dawei, A. Bryant, P. Mawby, L. Ran, and P. Tavner, "Condition monitoring for device reliability in power electronic converters: A review," *IEEE Trans. Power Electron.*, vol. 25, no. 11, pp. 2734–2752, Nov. 2010.

[19] J. Shin-Myung, P. Jin-Sik, K. Hag-Wone, C. Kwan-Yuhl, and Y. Myung-Joong, "An MRAS-based diagnosis of open-circuit fault in PWM voltage-source inverters for PM synchronous motor drive systems," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2514–2526, May 2013.

[20] W. Huai, M. Liserre, F. Blaabjerg, P. De Place Rimmen, J. B. Jacobsen, T. Kvisgaard, and J. Landkildehus, "Transitioning to physics-of-failure as a reliability driver in power electronics," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 1, pp. 97–114, Mar. 2014.

[21] M. Pulvirenti, G. Scarcella, G. Scelba, M. Cacciato, and A. Testa, "Fault-tolerant AC multidrive system," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 2, pp. 224–235, Jun. 2014.

[22] L. Bin and S. K. Sharma, "A Literature review of IGBT fault diagnostic and protection methods for power inverters," *IEEE Trans. Ind. Appl.*, vol. 45, no. 5, pp. 1770–1777, Sep./Oct. 2009.

[23] B. Mirafzal, "Survey of fault-tolerance techniques for three-phase voltage source inverters," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 1–1, Oct. 2014.

[24] F. Jen-Ren and T. A. Lipo, "A strategy to isolate the switching device fault of a current regulated motor drive," in *Proc. Conf. Rec. IEEE Ind. Appl. Soc. Annu. Meeting*, 1993, vol. 2, pp. 1015–1020.

[25] L. Tian-Hua, F. Jen-Ren, and T. A. Lipo, "A Strategy for improving reliability of field-oriented controlled induction motor drives," *IEEE Trans. Ind. Appl.*, vol. 29, no. 5, pp. 910–918, Sep./Oct. 1993.

[26] S. Bolognani, M. Zordan, and M. Zigliotto, "Experimental fault-tolerant control of a PMSM drive," *IEEE Trans. Ind. Electron.*, vol. 47, no. 5, pp. 1134–1141, Oct. 2000.

[27] S. Yantao and W. Bingsen, "Analysis and experimental verification of a fault-tolerant HEV power train," *IEEE Trans Power Electron.*, vol. 28, no. 12, pp. 5854–5864, Dec. 2013.

[28] R. L. De Araujo Ribeiro, C. B. Jacobina, E. R. C. Da Silva, and A. M. N. Lima, "Fault-tolerant voltage-fed PWM inverter AC motor drive systems," *IEEE Trans. Ind. Electron.*, vol. 51, no. 2, pp. 439–446, Apr. 2004.

[29] M. A. Rodriguez, A. Claudio, D. Theilliol, L. G. Vela, and L. Hernandez, "Strategy to replace the damaged power device for fault-tolerant induction motor drive," in *Proc. 24th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2009, pp. 343–346.

[30] S. Ogasawara and H. Akagi, "Modeling and damping of high-frequency leakage currents in PWM inverter-fed AC motor drive systems," *IEEE Trans. Ind. Appl.*, vol. 32, no. 5, pp. 1105–1114, Sep./Oct. 1996.

[31] D. Busse, J. Erdman, R. J. Kerkman, D. Schlegel, and G. Skibinski, "System electrical parameters and their effects on bearing currents," *IEEE Trans. Ind. Appl.*, vol. 33, no. 2, pp. 577–584, Mar./Apr. 1997.

[32] J. M. Erdman, R. J. Kerkman, D. W. Schlegel, and G. L. Skibinski, "Effect of PWM inverters on AC motor bearing currents and shaft voltages," *IEEE Trans. Ind. Appl.*, vol. 32, no. 2, pp. 250–259, Mar./Apr. 1996.

[33] ABB Drives. *Technical guide no. 5—Bearing currents in modern AC drive systems* (2011). [Online]. Available: http://www05.abb.com/global/scot/scot201.nsf/veritydisplay/8c253c2417ed0238c125788f003cca8e/$file/abb_technical_guide_no5_revc.pdf

[34] GAMBICA Variable Speed Drives Group. *Variable speed drives and motors—Motor shaft voltages and bearing currents under PWM inverter operation*, ed. 2, 2006. [Online]. Available: http://www.gambica.org.uk/web_images/documents/publications/GAMBICA_Motor_Shaft_Voltages_Bearing_Currents_Report2_2nd_ed.pdf

[35] M. R. Baiju, K. K. Mohapatra, R. S. Kanchan, and K. Gopakumar, "A dual two-level inverter scheme with common mode voltage elimination for an induction motor drive," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 794–805, May 2004.

[36] J. A. Restrepo, A. Berzoy, A. E. Ginart, J. M. Aller, R. G. Harley, and T. G. Habetler, "Switching strategies for fault tolerant operation of single DC-link dual converters," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 509–518, Feb. 2012.

[37] A. Von Jauanne and Z. Haoran, "A dual-bridge inverter approach to eliminating common-mode voltages and bearing and leakage currents," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 43–48, Jan. 1999.

[38] N. Aizawa and K. Kubota, "Analysis of common-mode voltage elimination of PWM inverter with auxiliary inverter," in *Proc. Int. Conf. Electrical Machines Syst.*, 2010, pp. 889–893.

[39] M. Kikuchi, N. Aizawa, K. Kubota, I. Miki, and K. Matsuse, "Investigation of common-mode voltages of PWM inverter with a small capacity auxiliary inverter," in *Proc. Int. Conf. Electrical Machines Syst.*, 2009, pp. 1–6.

[40] A. L. Julian, G. Oriti, and T. A. Lipo, "Elimination of common-mode voltage in three-phase sinusoidal power converters," *IEEE Trans. Power Electron.*, vol. 14, no. 5, pp. 982–989, Sep. 1999.

[41] ABB Industrial Systems, Inc. *Effects of AC drives on motor insulation* (1998, Apr.). [Online]. Available: http://www.aic-controls.com/fullpanel/uploads/files/abb-technical-guide-us102-motor-cable-lengths.pdf

[42] K. Sung-Jun and S. Seung-Ki, "A novel filter design for suppression of high voltage gradient in voltage-fed PWM inverter," in *Proc. Conf. 12th Annu. Appl. Power Electron. Expo.*, 1997, vol. 1, pp. 122–127.

[43] D. A. Rendusara and P. N. Enjeti, "An improved inverter output filter configuration reduces common and differential modes dv/dt at the motor terminals in PWM drive systems," *IEEE Trans. Power Electron.*, vol. 13, no. 6, pp. 1135–1143, 1998.

[44] A. Von Jouanne and P. N. Enjeti, "Design considerations for an inverter output filter to mitigate the effects of long motor leads in ASD applications," *IEEE Trans. Ind. Appl.*, vol. 33, no. 5, pp. 1138–1145, Sep./Oct. 1997.

[45] A. Von Jouanne, D. A. Rendusara, P. N. Enjeti, and J. W. Gray, "Filtering techniques to minimize the effect of long motor leads on PWM inverter-fed AC motor drive systems," *IEEE Trans. Ind. Appl.*, vol. 32, no. 4, pp. 919–926, 1996.

[46] H. Jiangbiao, G. Y. Sizov, Z. Peng, and N. A. O. Demerdash, "A review of mitigation methods for overvoltage in long-cable-fed PWM AC drives," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2011, pp. 2160–2166.
[47] D. J. Carnovale, J. Biternas, T. J. Dionise, and D. D. Shipp, "Design, development and testing of a voltage ride-thru solution for variable speed drives in oil field applications," in *Proc. IEEE Petroleum Chemical Ind. Tech. Conf.*, 2007, pp. 1–7.
[48] K. Stockman, F. D'Hulster, K. Verhaege, M. Didden, and R. Belmans, "Ride-through of adjustable speed drives during voltage dips," *Electric Power Syst. Res.*, vol. 66, pp. 49–58, Jul. 2003.
[49] M. Radmehr, S. Farhangi, and A. Nasiri, "Effects of power quality distortions on electrical drives and transformer life in paper industries: simulations and real time measurements," in *Proc. Conf. Rec. Annu. Pulp Paper Ind. Tech.*, 2006, pp. 1–9.
[50] A. Von Jouanne, P. N. Enjeti, and B. Banerjee, "Assessment of ride-through alternatives for adjustable-speed drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 4, pp. 908–916, Jul./Aug. 1999.
[51] N. Abi-Samra, D. Carnovale, A. Sundaram, and W. Malcolm, "The role of the distribution system dynamic voltage restorer in enhancing the power at sensitive facilities," in *Proc. WESCON*, 1996, pp. 167–181.
[52] K. Kriegel, A. Melkonyan, M. Galek, and J. Rackles, "Power module with solid state circuit breakers for fault-tolerant applications," in *Proc. 6th Int. Conf. Integr. Power Electron. Syst.*, 2010, pp. 1–6.
[53] A. Qun-Tao, S. Li-Zhi, Z. Ke, and S. Li, "Switching function model-based fast-diagnostic method of open-switch faults in inverters without sensors," *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 119–126, Jan. 2011.
[54] W. Zhiqiang, S. Xiaojie, L. M. Tolbert, W. Fei, and B. J. Blalock, "A di/dt feedback-based active gate driver for smart switching and fast overcurrent protection of IGBT modules," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3720–3732, Jul. 2014.
[55] A. M. Hava and N. O. Cetin, "A generalized scalar PWM approach with easy implementation features for three-phase, three-wire voltage-source inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1385–1395, May 2011.
[56] L. Kai, L. Ting, Z. Zhengming, Y. Lu, L. Fang, and Y. Liqiang, "Carrier based implementation of reduced common mode voltage PWM strategies," in *Proc. IEEE ECCE Asia Downunder (ECCE Asia)*, 2013, pp. 578–584.
[57] C. Jettanasen, "Reduction of common-mode voltage generated by voltage-source inverter using proper PWM strategy," in *Proc. Asia-Pacific Symp. Electromagn. Compat.*, 2012, pp. 297–300.
[58] E. Un and A. M. Hava, "A high-performance PWM algorithm for common-mode voltage reduction in three-phase voltage source inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1998–2008, Jul. 2011.
[59] Z. Yonggao, K. Guangjian, and L. Lizhong, "Research on reduced common-mode voltage nonzero vector pulse width modulation technique for three-phase inverters," in *Proc. 7th Int. Power Electron. Motion Control Conf.*, 2012, pp. 2349–2352.
[60] L. Yen-Shin, "Investigations into the effects of PWM techniques on common mode voltage for inverter-controlled induction motor drives," in *Proc. IEEE Power Eng. Soc. (Winter Meeting)*, 1999, vol. 1, pp. 35–40.
[61] V. H. Prasad, "Analysis and comparison of space vector modulation schemes for three-leg and four-leg voltage source inverters," *Master Sci., Elect. Eng.*, Virginia Tech., Blacksburg, VA, USA, 1997.

Pawan Garg (S'13–M'14) received the B.Tech. degree in instrumentation engineering from Indian Institute of Technology, Kharagpur, India, in 2009, and the M.S. degree in electrical engineering from Texas A&M University, College Station, TX, USA, in 2014.

From 2009 to 2011, he was an Engineer in Steel Authority of India Ltd. and GAIL India Ltd. He is currently a R&D Engineer with International Rectifier, El Segundo, CA, USA.

Somasundaram Essakiappan (S'10–M'14) received the B.E. degree in electrical engineering from the College of Engineering Guindy, Chennai, India, in 2007, and the M.S. degree and the Ph.D. degree in power electronics from Texas A&M University, College Station, TX, USA, in 2010 and 2014, respectively.

He is currently with the Department of Electrical and Computer Engineering, Texas A&M University. His current research interests include power electronics for renewable energy grid integration, power quality, and switching power converters.

Harish S. Krishnamoorthy (S'12) received the B.Tech. degree in electrical and electronics engineering from the National Institute of Technology, Tiruchirappalli, India, in 2008. He is currently working toward the Ph.D. degree in electrical engineering at Texas A&M University, College Station, TX, USA.

From 2008 to 2010, he was an Engineer in General Electric (GE) Energy, India. His current research interests include high power density converter design, renewable energy conversion, etc. He holds a U.S. patent and several international publications under his name.

Prasad N. Enjeti (M'85–SM'88–F'00) received the B.E. degree from Osmania University, Hyderabad, India, in 1980, the M.Tech. degree from the Indian Institute of Technology, Kanpur, India, in 1982, and the Ph.D. degree from Concordia University, Montreal, QC, Canada, in 1988, all in electrical engineering.

In 1988, he joined, as an Assistant Professor, the Department of Electrical Engineering Department, Texas A&M University, College Station, USA. In 1994, he was promoted to Associate Professor and in 1998 he became a Full Professor. He holds four U.S. patents and has licensed two new technologies to the industry so far. He is the lead developer of the Power Electronics/Power Quality and Fuel Cell Power Conditioning Laboratories, Texas A&M University, where he is actively involved in many projects with industries while involved in teaching, research, and consulting in the area of power electronics, motor drives, power quality, and clean power utility interface issues. His current research interests include advance converters for power supplies and motor drives; power quality issues and active power filter development; converters for fuel cells, wind energy systems, power electronic hardware for flywheel, ultra-capacitor-type energy storage/discharge devices for ride-through, and utility interface issues.

Dr. Enjeti received the inaugural R. David Middlebrook Technical Achievement Award from the IEEE Power Electronics Society in 2012. He received the IEEE-IAS Second and Third Best Paper Awards in 1993, 1998, 1999, 2001, and 1996, respectively; the Second Best IEEE-IA Transactions paper published in midyear 1994 to midyear 1995, the IEEE-IAS Magazine Prize Article Award in 1996, the Class of 2001 Texas A&M University Faculty Fellow Award for demonstrated achievement of excellence in research, scholarship and leadership in the field, and he directed a team of students to design and build a low-cost fuel cell inverter for residential applications, which won the 2001 future energy challenge award, grand prize, from the Department of Energy (DOE). He is a Registered Professional Engineer in the state of Texas.