Optically Switched-Drive-Based Unified Independent *dv/dt* and *di/dt* Control for Turn-Off Transition of Power MOSFETs

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***Abstract*—To control the switching dynamics of an optically triggered hybrid device, a photonic-control mechanism is outlined. The optically triggered hybrid device comprises a power MOSFET, as the main power semiconductor device (PSD), and a pair of GaAs-based optically triggered power transistors (OTPTs), serving as the driver for the power MOSFET. The switching-transition controller modulates the turn-off transition of the power MOSFET by modulating the optical intensity of the OTPTs. The independent and unified dv/dt and di/dt control of the PSD is achieved using a single control circuit which also predicts the onset of transition between the di/dt and the dv/dt regions of control. Experimental control results validating the OTPT-based dynamical modulation of the turn-off characteristic of the power MOSFET are provided. In this study, the power MOSFET is chosen to be a SiC MOSFET. However, the proposed photonic-control mechanism can be extended to Si power MOSFETs as well.**

***Index Terms*—Active gate drive, *di/dt*, *dv/dt*, electromagnetic interference (EMI), gallium arsenide (GaAs), IGBT, optical gate drive, optically triggered power transistor (OTPT), power MOSFET, silicon carbide (SiC), switching loss, switching transients.**

I. Introduction

As the industry moves toward to high-frequency and high-power-density applications, controlling the switching-transition dynamics of power semiconductor devices (PSDs) attains importance. Those applications include: switched mode power supplies, motor drives, solar inverters, battery chargers etc., [1]–[6]. As the switching frequency increases, the duration of the switching transition needs to be decreased to reduce the switching losses. However, this leads to higher di/dt and dv/dt, which in turn, causes higher electromagnetic interference (EMI) and device stress. Unification of the dv/dt and di/dt controls enables a high-frequency power-electronics system to achieve controllability and performance optimization over a wide operating range. Even though dv/dt and di/dt are intertwined, ability to control them independently provides a pathway toward total performance optimization with regard to switching loss, device stress, and EMI for any given operating condition.

In recent years, there has been growing interest to control the turn-off transition behavior of electrically triggered (ET) PSDs in the literature [7]–[17]. Modulation of the gate resistance has been proposed in [7]–[9]. In this scheme, different gate resistors are inserted in the discharging path of the gate circuit of the PSD during switching transition. Because only discrete values for the gate resistances are attainable, the optimized switching performance is not achievable over a wide operating range. Other approaches like controlling the gate current of the PSD or introducing an intermediate voltage to the gate of the PSD at selected intervals during turn-off transition has been proposed in [11]–[15]. However, work on control of both dv/dt and di/dt has been limited [16], [17]. Independent control of turn-off dv/dt and di/dt of a PSD, by controlling the gate current, is outlined in [16]. However, unification of the control approach has not been achieved because two individual circuits are used to control di/dt and dv/dt. Unified closed-loop di/dt-and-dv/dt control mechanism has been proposed in [17]. The di/dt and dv/dt are individually controlled by a reference voltage and circuit-dependent feedback gains. However, using the same reference voltage for both di/dt and dv/dt along with the constant feedback gains in each switching-transition period makes it difficult to adjust dv/dt without bounding adjustability of di/dt and vice-versa.

Although controlling the switching transitions of ET PSDs has been explored, limited work has been conducted on the switching-transition control of optically triggered (OT) PSDs [18]–[20]. Recent work on monolithic and hybrid OT PSDs [21]–[27] have demonstrated the feasibility of using a single optical link for both pulse-width modulation (PWM) and switching-transition control of a PSD using a controller, which is spatially separated from the PSD power stage. However, the optical-to-electrical conversion delay is appreciable as compared to the total duration of the switching transition which adversely affects the performance of the transition controller with feedback [21], [23].

In this paper, turn-off switching-transition control of an OT hybrid PSD, comprising two GaAs-based optically triggered power transistors (OTPTs) and a SiC MOSFET, is outlined. The outlined mechanism for optical control can be extended to Si power MOSFETs as well because of similarities in device behavioral dynamics [28], [29]. The OTPTs are placed in the charging (turn-on) and discharging (turn-off) paths of the gate of the SiC

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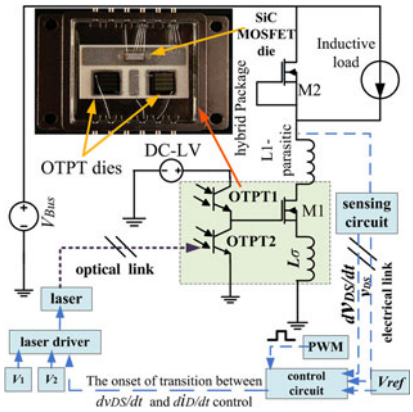

Fig. 1. Test circuit and control block diagram. *V*1 and *V*2, respectively, control $dv_{\rm DS}/dt$ and di_D/dt of M1 in the $dv_{\rm DS}/dt$- and di_D/dt-control regions of operation as illustrated in Fig. 2. The threshold condition, for the onset of transition between the $dv_{\rm DS}/dt$- and di_D/dt-control regions, is provided in Section II-A.

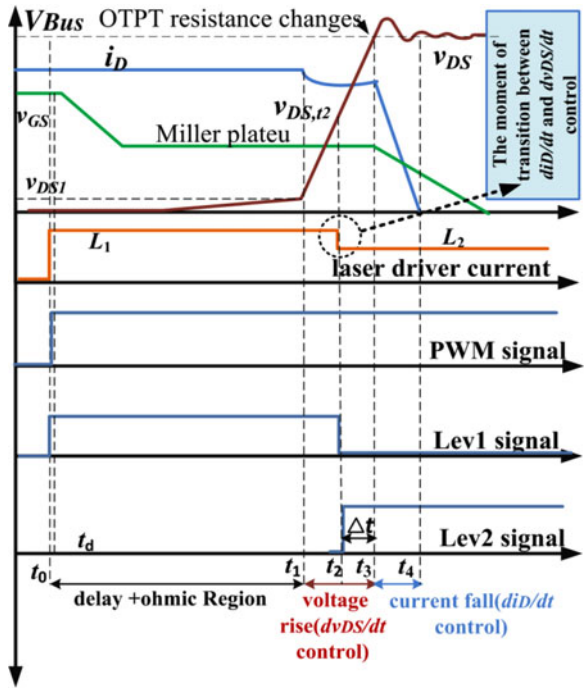

Fig. 2. Turn-off behavior of the MOSFET and control circuit key waveforms. The output currents L_1 and L_2 of the laser driver are proportional to the voltage commands V_1 and V_2, which dictate the $dv_{\rm DS}/dt$ and di_D/dt dynamics of M1 in the $dv_{\rm DS}/dt$ and di_D/dt control regions.

MOSFET. Unified turn-off dv/dt and di/dt control are achieved using a single circuit by modulating the intensity of the optical beam that triggers the OTPT, which controls the turn-off of the SiC MOSFET. A laser driver is designed to dynamically adjust the optical intensities for dv/dt and di/dt control. The independent control of turn-off dv/dt and di/dt is achieved by means of a control circuit which compensates for the total delay in the control loop. It also predicts the moment of transition between dv/dt and di/dt regions of control.

The rest of the paper is organized as follows: in Section II, initially the principle of optical control of turn-off dv/dt and turn-off di/dt of an OT SiC MOSFET is illustrated. Subsequently, the threshold condition and control concept for predicting the onset of transition from the dv/dt to the di/dt control region, which ensures the independent controllability of the two regions of control, is outlined. Then, mathematical analyses for availability of the independent control of turn-off *dv/dt* and *di/dt* are provided. Finally, the experimental results validating feasibility of the proposed control under different operating conditions are demonstrated in Section III. It is noted that, in the remaining paper, the terms dv/dt and di/dt are used to represent the rate of change of voltage across and the rate of change of current through a general PSD. While, $dv_{\rm DS}/dt$ and di_D/dt are used to represent the rate of change of voltage across and the rate of change of current through the SiC MOSFET (M1) shown in Fig. 1.

II. Turn-Off Transition Behavior and Control

The standard clamped-inductive test circuit and control block diagram for optical transition control are shown in Fig. 1. The test circuit comprises a bridge leg with the hybrid device package (comprising M1 and the two OTPTs) placed in the low side and a self-gated SiC MOSFET (M2) in the high side. MOSFET M2 has characteristics similar to the characteristics of the SiC MOSFET in the hybrid package. OTPT1 and OTPT2 work complementarily and turn the SiC MOSFET (M1) on and off, respectively.

As indicated in Fig. 2, when the turn-off command is initiated by the PWM signal at t_0, the laser driver provides the current level L_1 (proportional to the external voltage control command V_1 shown in Fig. 1) for the laser with its wavelength centered at 808 nm. The laser delivers an optical power corresponding to the current level L_1 to the base region of the OTPT2 via an optical link. OTPT2 then turns-on, after some delay, at t_d, allowing the gate charge of M1 to be discharged through it. The turn-on delay of OTPT as a function of optical power has been measured using the resistive circuit of Fig. 3 employing the point to point method. The results are then plotted in Fig. 3. The higher optical intensity results in smaller turn-on delay due to the higher rate of photo-generated carrier density inside the OTPT as shown in Fig. 3. More information about the characteristics and behavior of OTPT is provided in [30] and [31]. After the OTPT is turned on, the gate-to-source voltage ($v_{\rm GS}$) of M1 starts to fall until it reaches the Miller plateau voltage ($V_{\rm Miller}$); subsequently, the drain-to-source voltage ($v_{\rm DS}$) of M1 begins to rise. The slope of $v_{\rm DS}$ is approximated using the following relation:

$$dv_{\rm DS}/dt \approx \frac{v_{\rm GS,TH} + i_D/g_{fs}}{R_G C_{\rm GD}} = \frac{V_{\rm Miller}}{R_G C_{\rm GD}}. \qquad (1)$$

In (1), g_{fs} is the forward transconductance of M1, i_D is the drain current, $C_{\rm GD}$ is the gate-to-drain capacitance of M1 also known as Miller capacitance,R_G is the gate resistance, and $v_{\rm GS,TH}$ is the threshold voltage of M1. However, the gate-to-drain capacitance of MOSFETs is a nonlinear function of $v_{\rm DS}$. $C_{\rm GD}$ of M1 is approximated as a two-step function of

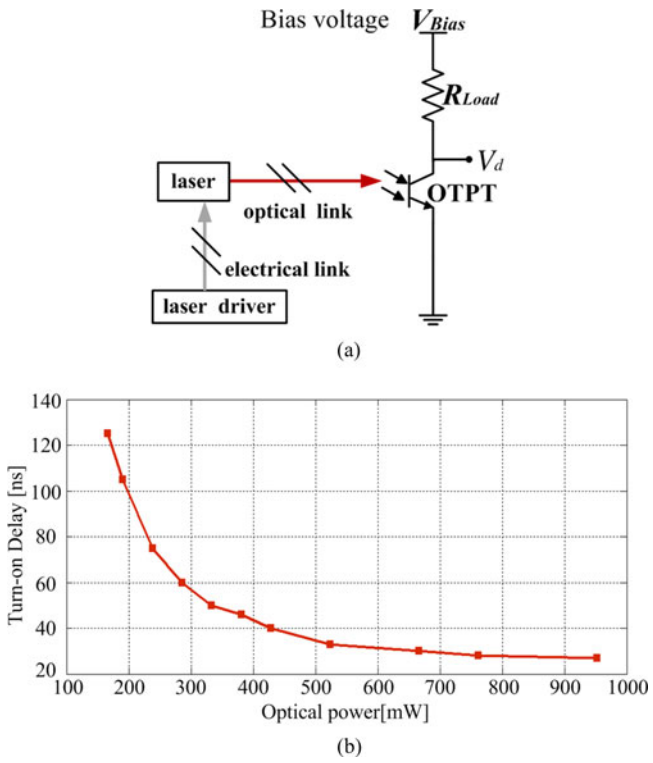

Fig. 3. (a) Resistive load test circuit and (b) turn-on delay of OTPT versus the optical power, using the resistive-load circuit. $V_{\rm Bias} = 10\,V$, $R_{\rm Load} = 200\,\Omega$, frequency = 50 kHz, and duty cycle = 50%.

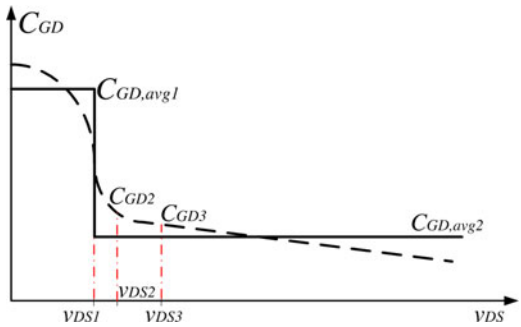

Fig. 4. Gate-to-drain capacitance of M1 (also known as Miller capacitance) as a function of drain-to-source voltage.

drain-to-source voltage of M1 as shown in Fig. 4:

$$C_{\rm GD} = \begin{cases} C_{\rm GD,avg1}, & v_{\rm DS} < v_{\rm DS1} \\ C_{\rm GD,avg2}, & v_{\rm DS} \geq v_{\rm DS1}. \end{cases} \tag{2}$$

Equation (2) is mostly true for other types of power MOSFETs and even IGBTs, as well [32]. Typically, $C_{\rm GD,avg1}$ is dramatically higher than $C_{\rm GD,avg2}$. Therefore, slope of the drain-to-source voltage of M1 before $v_{\rm DS}$ reaches the turning point $v_{\rm DS1}$ (corresponding to the time t_1 in Fig. 2), is significantly lower as compared to the duration in which $v_{\rm DS} \geq v_{\rm DS1}$. The interval in which $v_{\rm DS}$ is lower than $v_{\rm DS1}$ is referred as ohmic region, as shown in Fig. 2. Furthermore, the interval in which $v_{\rm DS}$ is higher than $v_{\rm DS1}$ and lower than the bus voltage

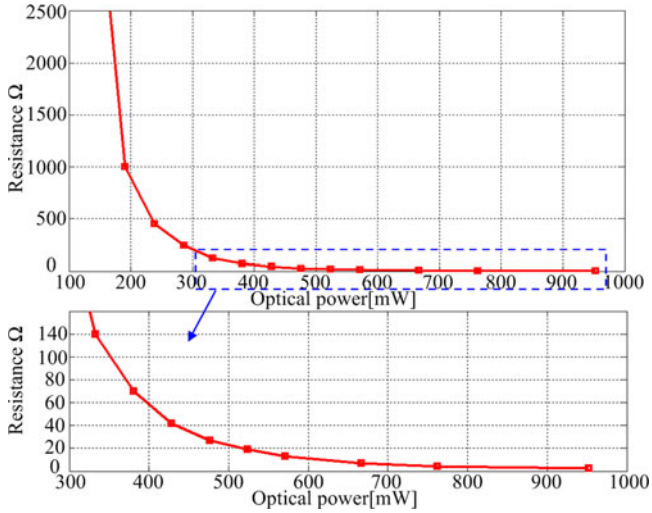

Fig. 5. Resistance of OTPT versus the optical power, using the resistive-load circuit of Fig. 3.

($V_{\rm Bus}$) is referred as $dv_{\rm DS}/dt$ control region (corresponding to the interval between t_1 and t_3 in Fig. 2).

According to (1), the $dv_{\rm DS}/dt$ can be controlled by varying the resistance in the discharging path of the gate. The latter in turn is adjusted by changing the optical intensity of OTPT2. Current level L_1 of the laser driver sets the optical intensity in the $dv_{\rm DS}/dt$ control region. Resistance of OTPT as a function of optical power is measured using the resistive circuit of Fig. 3 and data are plotted in Fig. 5.

When $v_{\rm DS}$ matches the bus voltage ($V_{\rm Bus}$) at t_3, current i_D falls which causes an overvoltage across M1 due to the parasitic inductances in the commutation path. This region is referred to as the di_D/dt control region. The overvoltage (Δv_{ov}) across the drain-to-source terminals of M1 is given by the following expression:

$$\Delta v_{ov} = L_c . \frac{di_D}{dt} \tag{3}$$

where L_c is the sum of the parasitic inductances in the commutation path, which includes the parasitic inductances of M1 and M2, bus-parasitic inductance, and trace inductances. In the di_D/dt control region, di_D/dt is given by the following expression:

$$\frac{di_D}{dt} \approx -\frac{V_{\rm GS,TH} + i_D/2g_{fs}}{R_G C_{iss}/g_{fs} + L_\sigma}. \tag{4}$$

In (4), C_{iss} is the input capacitance of M1 and L_σ is the sum of parasitic inductances seen from the source of M1. Following (4), the di_D/dt is controlled by varying the resistance of the discharging path of the gate of M1. This resistance is adjusted by changing the optical intensity of OTPT2, as shown in Fig. 3. Current level (L_2) of the laser driver sets the optical intensity in the di_D/dt control region and L_2 is proportional to the external voltage control command V_2, as shown in Fig. 1.

Of course, while the control of $dv_{\rm DS}/dt$ and di_D/dt in their respective regions of operation is important, a seamless transition between the $dv_{\rm DS}/dt$ and di_D/dt control regions is equally

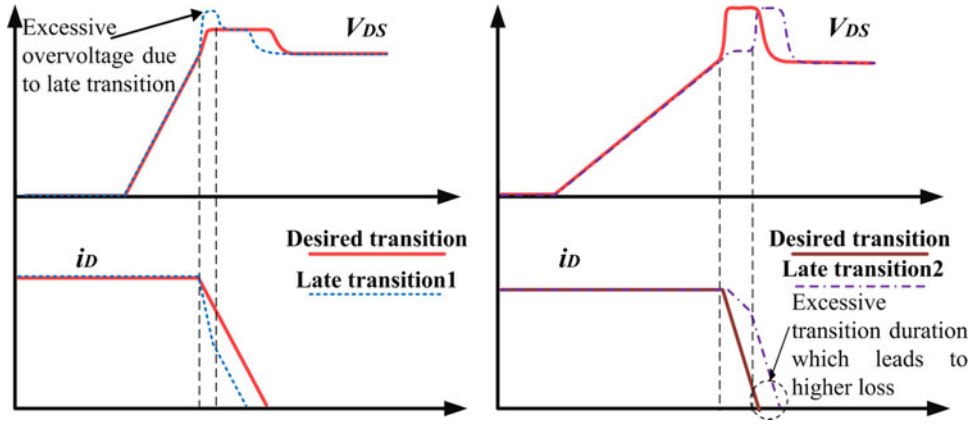

Fig. 6. Effect of late transition between the $dv_{\rm DS}/dt$ and di_D/dt control regions on device stress and switching loss.

important. In the following section, we derive this threshold condition for transition between the two control regions and outline its implementation.

A. *Threshold Condition for Transition Between the $dv_{\rm DS}/dt$ and the di_D/dt Control Regions*

The transition between L_1 and L_2, thereby transitioning from the $dv_{\rm DS}/dt$ to the di_D/dt control region, is initiated by the control circuit illustrated in Fig. 1. This transition guarantees the independent control of di_D/dt and $dv_{\rm DS}/dt$. Following, [7], [14], [16], an easy way to detect the onset of the di_D/dt control region is to detect the change in the di_D/dt from near zero to a significantly larger value. If this approach is adopted, the onset of transition is initiated later than the desired instant due to control-loop and OTPT-related delays. So, one may lose the control over di_D/dt in all or a part of this di_D/dt control region, which may lead to excessive device stress or switching loss as illustrated in Fig. 6. Another approach [8] for predicting the onset of the di_D/dt control region is based on detecting the saturation region of the voltage corresponding to $dv_{\rm DS}/dt$ control region in Fig. 2 and initiating the transition between the $dv_{\rm DS}/dt$ and the di_D/dt control regions after a fixed delay. However, the error in the prediction of onset of transition is significant in applications where the $dv_{\rm DS}/dt$ varies over a wide range.

Therefore, in the proposed scheme, to ensure the independent control of $dv_{\rm DS}/dt$ and di_D/dt, a simple control circuit is designed which predicts the onset of transition between the $dv_{\rm DS}/dt$ and di_D/dt control regions based on the actual $dv_{\rm DS}/dt$ and the scaled bus-voltage reference ($v_{\rm ref}$). The di_D/dt control region onsets at t_3, when $v_{\rm DS}$ reaches the bus voltage ($V_{\rm Bus}$) as shown in Figs. 2 and 7. However, considering a combined constant delay of Δt seconds due to the feedback and due to the delay in the actuation of OTPT2, the control circuit initiates the transition between $dv_{\rm DS}/dt$ and di_D/dt control regions at time $t_2(=t_3-\Delta t)$. An accurate onset of transition ensures the independent controllability of the $dv_{\rm DS}/dt$ and di_D/dt control regions.

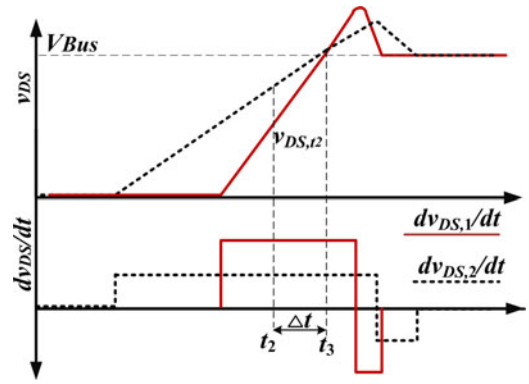

Fig. 7. Signals $v_{\rm DS}$ and $dv_{\rm DS}/dt$, at the desired time (t_2) of transition for two different $dv_{\rm DS}/dt$, considering the constant delay of Δt seconds in the feedback loop.

Now, using Fig. 7, one can show that for any given $dv_{\rm DS}/dt$ the following equality holds:

$$v_{{\rm DS},t2} + (dv_{{\rm DS},t2}/dt)\ .\ \Delta t = V_{\rm Bus}. \tag{5}$$

In (5), $v_{{\rm DS},t2}$ and $dv_{{\rm DS},t2}/dt$ represent, respectively, the values of $v_{\rm DS}$ and $dv_{\rm DS}/dt$ at time t_2. Assuming the scaling factors of α_1, α_2, and α_3 associated with sensing $V_{\rm Bus}$, $v_{\rm DS}$, and $dv_{\rm DS}/dt$, respectively, the following equations hold:

$$v_{\rm ref} = \alpha_1.V_{\rm Bus} \tag{6}$$

$$v'_{{\rm DS},t2} = \alpha_2.v_{{\rm DS},t2} \tag{7}$$

$$dv'_{{\rm DS},t2}/dt = \alpha_3.(dv_{{\rm DS},t2}/dt). \tag{8}$$

In (7), $v'_{{\rm DS},t2}$ represents the value of sensed $v_{\rm DS}$ at time t_2 with a scaling factor of α_2. In (8), $dv'_{{\rm DS},t2}/dt$ represents the value of sensed $dv_{\rm DS}/dt$ at t_2 with a scaling factor of α_3. Substituting (6)–(8) into (5) yields the following relation:

$$\frac{v'_{{\rm DS},t2}}{\alpha_2} + \frac{dv'_{{\rm DS},t2}/dt}{\alpha_3}.\Delta t = \frac{v_{\rm ref}}{\alpha_1}. \tag{9}$$

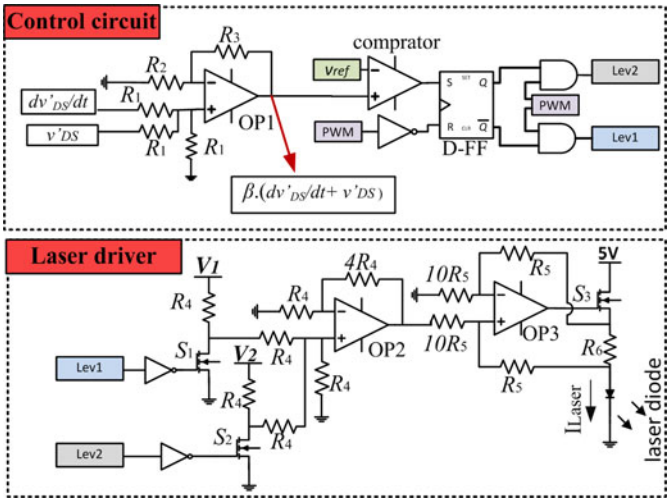

Fig. 8. Schematics of the control circuit and the laser driver.

TABLE I
TRUTH TABLE OF THE CONTROL CIRCUIT OF FIG. 8

Comparator	$\overline{\text{PWM}}$	Q	$\bar{\text{Q}}$	LEV1	LEV2
1	0	1	0	1	0
0	1	0	1	0	0
1	1	1	1	0	0
0	0	X	X	X	X

Because Δt is considered to be a constant, (8) can be rewritten as follows:

$$\beta_1.\acute{v}_{\text{DS},t2} + \beta_2.(d\acute{v}_{\text{DS},t2}/dt) = v_{\text{ref}}. \tag{10}$$

In (10), β_1 equals to (α_1/α_2) and β_2 equals to$(\alpha_1.\Delta t/\alpha_3)$. Using (10), the threshold condition for transition from the dv_{DS}/dt to di/dt control region is found to be

$$(\beta_1.\acute{v}_{\text{DS}} + \beta_2.(d\acute{v}_{\text{DS}}/dt)) - v_{\text{ref}} \geq \varepsilon. \tag{11}$$

In (11), $\acute{v}_{\text{DS}}$ and $d\acute{v}_{\text{DS}}/dt$ represent, respectively, the sensed values of v_{DS} and dv_{DS}/dt at any time with scaling factors of α_2 and α_3 whereas ε represents a very small positive value. Essentially, (11) indicates that there is a time t (ideally $t = t_2 = t_3 - \Delta t$) at which the difference between $\beta_1.\acute{v}_{\text{DS}} + \beta_2.(d\acute{v}_{\text{DS}}/dt)$ and v_{ref} is either zero or very close to zero. This concept is used to design a controller which compensates for the delay in the feedback loop and ensures a seamless transition between dv_{DS}/dt and di_D/dt control regions.

The control circuit and laser driver schematics are shown in Fig. 8. The coefficients β_1 and β_2 are considered to be equal to make the design of the control circuit easier. Therefore, the coefficients α_1 and α_2 have the following relation:

$$\beta_1 = \beta_2 = \beta \Rightarrow \frac{\alpha_1}{\alpha_2} = \frac{\alpha_1}{\alpha_3}\Delta t \Rightarrow \alpha_2 = \frac{\alpha_3}{\Delta t}. \tag{12}$$

The sensed v_{DS} and dv_{DS}/dt are scaled with the proper coefficient β and added using the OP1, as shown in Fig. 8, where $\beta = R_1/3.(1 + R_3/R_2)$. The output of OP1 is then compared with v_{ref} using a comparator to monitor if the threshold condition in (11) is met. If (11) is satisfied, the control circuit initiates the transition from dv_{DS}/dt to di_D/dt control region by setting Lev1 to logic state 0 and Lev2 to logic state 1 using the D-FF and AND operators of Fig. 8.

Because of the negative dv_{DS}/dt in the di_D/dt control region, the threshold condition might not be satisfied in the di_D/dt control region. Therefore, a D flip-flop is used to prevent undesirable fluctuations of the logic states of signals Lev1 and Lev2 in the di_D/dt control region. The truth table for the control circuit can be found in Table I. In Table I, X means no change in the state of the signal. Any negligible error in initiating the onset of transition (i.e., $\varepsilon \neq 0$ and instead $\varepsilon \approx 0$) is due to the nonidealities in the circuit elements, nonlinearities, and error in the estimation of the total delay of the feedback loop [18].

Subsequent to the change in the logic states of Lev1 and Lev2, the laser driver changes its output current (I_{Laser}) from L_1 to L_2 (which is proportional to V_1 and V_2) and is given by the following relation:

$$I_{\text{Laser}} = \begin{cases} \gamma.V_1 = L_1, & \text{when Lev1 signal is high} \\ \gamma.V_2 = L_2, & \text{when Lev2 signal is high} \\ 0, & \text{when PWM signal is low.} \end{cases} \tag{13}$$

In (13), γ is a circuit-dependent constant and it is equal to $\gamma = 0.1/R_6$. The outputs of the flip-flop Q and $\overline{\text{Q}}$, in Fig. 8, work complementarily. Furthermore, the Lev1 and Lev2 signals are derived using the AND operation of the PWM signal with $\bar{\text{Q}}$ and Q, respectively. Therefore, Lev1 and Lev2 signals in (12) are complement to each other in the duration when the PWM signal is high and they are both low when PWM signal is low, as illustrated in Fig. 2 and Table I. Following (1), (4), and (14), one can adjust dv_{DS}/dt and di_D/dt by respectively controlling V_1 and V_2, which in turn control the output current of the laser driver to magnitudes of L_1 and L_2. Modulating the optical intensity by the proposed laser driver, along with the implementation of the threshold condition (11), enables one to attain the unified dv_{DS}/dt and di_D/dt control.

B. Availability of Independent dv_{DS}/dt and di_D/dt Control

In Section II-A, the threshold condition for independent control of turn-off dv_{DS}/dt and di_D/dt was derived. Subsequently, the control circuit was designed based on the aforementioned threshold condition. However, the threshold condition was derived considering the following assumptions:

1) The Δt (total delay in the feedback loop and OTPT) is fixed.
2) The dv_{DS}/dt is fixed from the time at which the transition command initiates (t_2) up to the desired moment of transition at t_3. Essentially the dv_{DS}/dt is fixed during the delay time of OTPT.
3) Δt is less than the duration of dv_{DS}/dt control region ($\Delta t < (t_3 - t_1)$).

Based on the mathematical analysis and threshold condition in Section II-A, the control circuit can independently control the turn-off dv_{DS}/dt and di_D/dt as long as the aforementioned

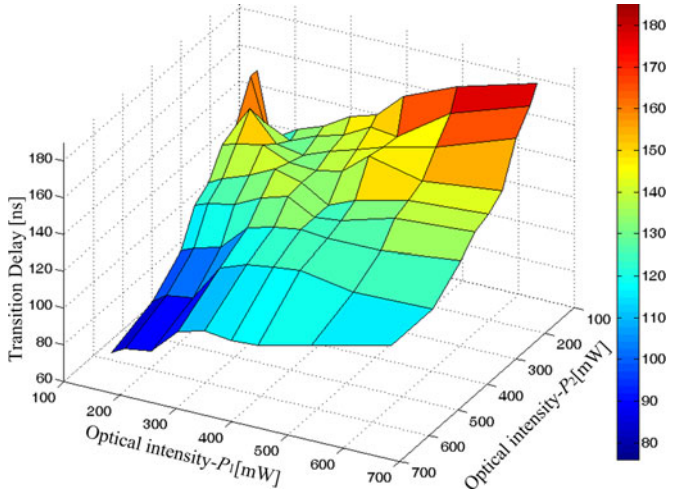

Fig. 9. Measured transition delay of resistance of the OTPT when the optical intensity changes from P_1 to P_2.

assumptions are valid. Therefore, the domain of validity of the aforementioned assumptions shall be analyzed to specify the boundaries for the availability of independent $dv_{\rm DS}/dt$ and di_D/dt control.

In Section II-A, it is assumed that the Δt is fixed. However, Δt varies proportionally to the difference between the optical intensities in the $dv_{\rm DS}/dt$ and the di_D/dt control regions. In this control scheme, the turn-on and turn-off delays of OTPT are not important. However, the important delay is defined as the total time that it takes for the resistance of OTPT to change from the value R1 (corresponding to the optical intensity P_1 and the laser current of $L1$) and reaches the final resistance value of R2 (corresponding to the optical intensity P_2 and the laser current of L_2). In order to derive the transition delay of the OTPT when it is subject to a step change in its receiving optical intensity, OTPT is tested using the resistive-load circuit of Fig. 3. In this setup, OTPT receives the optical intensity of P_1 through the laser and optical link which causes the voltage drop of V_{d1} across the OTPT. Subsequently, the optical intensity is varied from P_1 to P_2 which makes the voltage drop V_{d2} across the OTPT. The delay is measured between the time at which the optical intensity is changed to P_2 and the time at which the voltage drop across OTPT reaches 90% of its final value (V_{d2}). The measured delay time for different values of P_1 and P_2 is derived using the point to point method, and plotted in Fig. 9.

If optical intensities P_1 and P_2 are equal ($P_1 = P_2$), the transition delay is essentially zero. However, the value of transition delay in this case is selected such that the plot of Fig. 9 is smooth.

Now consider the case in which the optical intensity P_1 is applied to the OTPT in the $dv_{\rm DS}/dt$ control region, to control the turn-off $dv_{\rm DS}/dt$. Similarly, the optical intensity P_2 is applied in the di_D/dt control region to control the turn-off di_D/dt. Therefore, the transition delay for the resistance of OTPT2 to change from R1 (corresponding to the optical intensity P_1) and reaches the value of R2 (corresponding to the optical intensity P_2) is Δt_1, based on Fig. 9. Considering the implemented transition delay in the control circuit is equal to Δt, the transition error because of the variable transition delay of OTPT2, (E_{r1}), is defined by the following expression:

$$E_{r1} = \Delta t_1 + \Delta t_c - \Delta t. \tag{14}$$

In (14), Δt_c is the delay of the control circuit. If $E_{r1} > 0$, it affects the controllability over the di_D/dt in the di_D/dt control region, and if $E_{r1} < 0$, it affects the controllability over the $dv_{\rm DS}/dt$ in the $dv_{\rm DS}/dt$ control region. Therefore, the proportional error due to the variable transition delay of OTPT2, $(E_{r1}\%)$, is defined as

$$E_{r1}\% = \frac{E_{r1}}{t_{\rm rise}} = \frac{E_{r1}}{i_D}.di_D/dt \times 100\%, \text{ if } E_{r1} > 0$$
$$E_{r1}\% = \frac{E_{r1}}{t_{\rm fall}} = \frac{E_{r1}.dv_{\rm DS}/dt}{V_{\rm Bus} - v_{\rm DS1}} \times 100\%, \text{ if } E_{r1} < 0. \tag{15}$$

In (15), $t_{\rm rise}$ is the rise time of the drain-to-source voltage of M1, and $t_{\rm fall}$ is the fall time of the drain current of M1. In this study, the independent transition control of turn-off $dv_{\rm DS}/dt$ and turn-off di_D/dt is valid, if $E_{r1}\% \leq 10\%$.

The control circuit in Section II-A is designed using the threshold condition and considering a fixed $dv_{\rm DS}/dt$ in the $dv_{\rm DS}/dt$ control region. However, because of nonlinear behavior of $C_{\rm GD}$ the actual $dv_{\rm DS}/dt$ in the $dv_{\rm DS}/dt$ control region is not fixed. Therefore, the actual $dv_{\rm DS}/dt$ has some deviation from the average $dv_{\rm DS}/dt$ which is defined by $C_{\rm GD,avg2}$. This deviation might results in a transition error, especially in the case of a high $dv_{\rm DS}/dt$ in which the value of $v_{\rm DS}$ at t_2 $(v_{{\rm DS},t2})$ is close to $v_{\rm DS1}$. t_2 is the time at which the transition from the $dv_{\rm DS}/dt$ to the di_D/dt control region is initiated by the control circuit, as shown in Fig. 2.

Following (2) and Fig. 4, the average $C_{\rm GD}$ in the $dv_{\rm DS}/dt$ control region is equal to $C_{\rm GD,avg2}$. Therefore, the average $dv_{\rm DS}/dt$ which is defined by $C_{\rm GD,avg2}$, is equal to $dv_{\rm DS,avg}/dt$. Hence, the drain-to-source voltage of M1 at which the threshold condition is satisfied and transition is initiated is derived by the following expression, using (5):

$$v_{\rm DS2} = V_{\rm Bus} - (dv_{\rm DS,avg}/dt).\Delta t. \tag{16}$$

However, if $v_{\rm DS2}$ is close to $v_{\rm DS1}$, the value of $C_{\rm GD}$ at $v_{\rm DS2}(C_{\rm GD2})$ is higher than the value of $C_{\rm GD,avg2}$, as shown in Fig. 4. Because $C_{\rm GD2}$ is higher than $C_{\rm GD,avg2}$, the slope of the drain-to-source voltage of M1 at $v_{\rm DS2}$ is lower than the $dv_{\rm DS,avg}/dt$, according to (2). Therefore, the value of $dv_{\rm DS}/dt$ at $v_{\rm DS2}$ is not high enough to satisfy the threshold condition. As a result, the threshold condition is satisfied and transition is initiated, after some delay, at $v_{\rm DS3}(v_{\rm DS3} > v_{\rm DS2})$. $v_{\rm DS3}$ is derived using the following expression:

$$v_{\rm DS3} = V_{\rm Bus} - (dv_{\rm DS3}/dt).\Delta t. \tag{17}$$

In (17), $dv_{\rm DS3}/dt$ is the $dv_{\rm DS}/dt$ at voltage $v_{\rm DS3}$ corresponding to $C_{\rm GD3}$ in Fig. 4. The transition is initiated Δt seconds after $v_{\rm DS}$ reaches $v_{\rm DS3}$. However, the actual time that it takes for $v_{\rm DS}$ to reach $V_{\rm Bus}$, (Δt_2), (beginning of the di_D/dt control region) is derived using the following equation:

$$\Delta t_2 = \frac{dv_{\rm DS3}/dt}{dv_{\rm DS,avg}/dt}.\Delta t. \tag{18}$$

In (18), it is assumed that the average $dv_{\rm DS}/dt$ from $v_{\rm DS3}$ to $V_{\rm Bus}$ is equal to $dv_{\rm DS,avg}/dt$. Therefore, the transition error due to variable $dv_{\rm DS}/dt$ in the $dv_{\rm DS}/dt$ control region, (Er_2), is equal to:

$$\begin{aligned} Er_2 &= \Delta t - \Delta t_2 = \left(1 - \frac{dv_{\rm DS3}/dt}{dv_{\rm DS,avg}/dt}\right).\Delta t \\ Er_2 &= \left(1 - \frac{C_{\rm GD,avg2}}{C_{\rm GD3}}\right).\Delta t. \end{aligned} \tag{19}$$

Because $C_{\rm GD3}$ is always greater than $C_{\rm GD,avg2}$ in high $dv_{\rm DS,avg}/dts$, Er_2 is positive. Positive Er_2 means that, the transition error does not affect the controllability over the $dv_{\rm DS}/dt$ in the $dv_{\rm DS}/dt$ control region, but it affects the controllability over the di_D/dt in the di_D/dt control region. If the amount of the transition error (Er_2) is considerable comparing to $t_{\rm fall}$ of M1, the independent controllability of $dv_{\rm DS}/dt$ and di_D/dt is not granted. Therefore, the proportional error due to variable $dv_{\rm DS}/dt$ in the $dv_{\rm DS}/dt$ control region, $(Er_2\%)$, is defined as follows:

$$Er_2\% = \frac{Er_2}{t_{\rm fall}} \times 100\% = Er_2 \times \frac{di_D/dt}{i_D} \times 100\%. \tag{20}$$

In this study, $Er_2\% \leq 10\%$ is considered as an acceptable error for independent controllability of $dv_{\rm DS}/dt$ and di_D/dt.

Following, the procedure of calculating the quantitative boundaries of $dv_{\rm DS}/dt$ and di_D/dt for having the independent controllability of $dv_{\rm DS}/dt$ and di_D/dt is described. Initially, the maximum applicable di_D/dt, $(di_{D,\max}/dt)$, is derived for a given load current and bus voltage, using (3) and considering the maximum allowable overvoltage. Then, the minimum fall time of the drain current of M1, $(t_{\rm fall,min})$, is calculated using the following expression:

$$t_{\rm fall,min} = \frac{i_D}{di_{D,\max}/dt}. \tag{21}$$

Subsequently, P_2 is calculated using (4) and Fig. 5. Knowing P_2, Δt is selected using Fig. 9, such that the conditions in (14) is satisfied. Afterward, Er_2 is calculated knowing the maximum admissible $Er_2\%$ for $t_{\rm fall,min}$, using (20). Then, the value of $C_{\rm GD3}$ is derived, using (19), and the corresponding voltage for $C_{\rm GD3}$ $(v_{\rm DS3})$ is derived, using Fig. 4. Therefore, the maximum allowable $dv_{\rm DS}/dt$ is equal to

$$dv_{\rm DS,max}/dt = \frac{V_{\rm Bus} - v_{\rm DS3}}{(1 - Er_2\%/100).\Delta t}. \tag{22}$$

If $dv_{\rm DS,max}$ is selected properly, one will not face the condition in which Δt is less than the duration of $dv_{\rm DS}/dt$ control region $(\Delta t < (t_3 - t_1)$. However, if this condition happens the independent controllability of turn-off $dv_{\rm DS}/dt$ and di_D/dt is not granted. The flowchart of the procedure of calculating the quantitative boundaries of $dv_{\rm DS}/dt$ and di_D/dt is shown in Fig. 10.

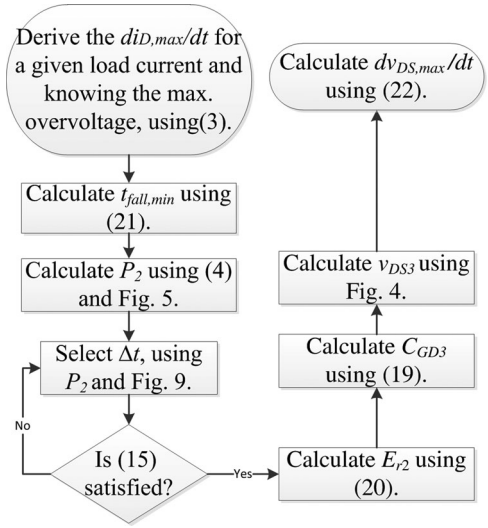

Fig. 10. Flowchart of the procedure of calculating the quantitative boundaries of $dv_{\rm DS}/dt$ and di_D/dt for independent control of turn-off $dv_{\rm DS}/dt$ and di_D/dt.

III. Experimental Results

The standard clamped-inductive test circuit of Fig. 1 along with the proposed control circuit are designed and fabricated as shown in Fig. 11. The fabricated set up includes the power circuit, the hybrid device package, power-supply circuits and the laser on the top side of the board and the control circuit, laser driver and sensing circuits on the bottom side of the board. The implemented SiC power MOSFET is CMF10120D with break-down voltage (BV) of 1200 V, current rating of 24 A, $C_{\rm GD} = 7$ pF, *Ciss* $= 928$ pF and *Coss* $= 68$ pF. A 2 W, 808 nm fiber-coupled laser is used to trigger the OTPT2, as shown in Fig. 11. The threshold current of the laser is 0.4 A, and its output optical power as a function of input current is shown in Fig. 12. An additional inductor is used in the commutation path to simulate the effect of the leakage inductance in the isolated dc/dc converters such as cuk, flyback, and forward. Voltage sensing circuit has a band-width (BW) of 200 MHz and delay of 5 ns. The experimental waveforms are measured using Tektronix DPO7104, which has the BW of 1 GHz. A 25 MHz differential voltage-probe along with a 50 MHz current sensors are used to provide the signals for the oscilloscope. Subsequently, the measured data are plotted using MATLAB software.

Experimental results for the independent optical control of the di_D/dt of M1 with fixed $dv_{\rm DS}/dt$ are shown in Fig. 13. The output current of the laser-driver $(I_{\rm Laser})$ remains the same in the $dv_{\rm DS}/dt$ control region. This leads to the same resistance for OTPT2, which is placed in the discharging path of the gate of M1, for all the cases. As the result, the current through OTPT2 and the turn-off $dv_{\rm DS}/dt$ in the $dv_{\rm DS}/dt$ control region is kept similar for all of the cases following (1). A step change in the output current of the laser driver initiates the onset of transition from the $dv_{\rm DS}/dt$ to the di_D/dt control region. The proper time of transition ensures independent controllability in the $dv_{\rm DS}/dt$ and di_D/dt control regions. Therefore, one is able to control the slope of the drain current in the di_D/dt control region without affecting the controllability over slope of the drain-to-source voltage in the $dv_{\rm DS}/dt$ control region. This is illustrated in Fig. 13. As current level (L_2) of the laser driver in the di_D/dt control region decreases the turn-off di_D/dt, the

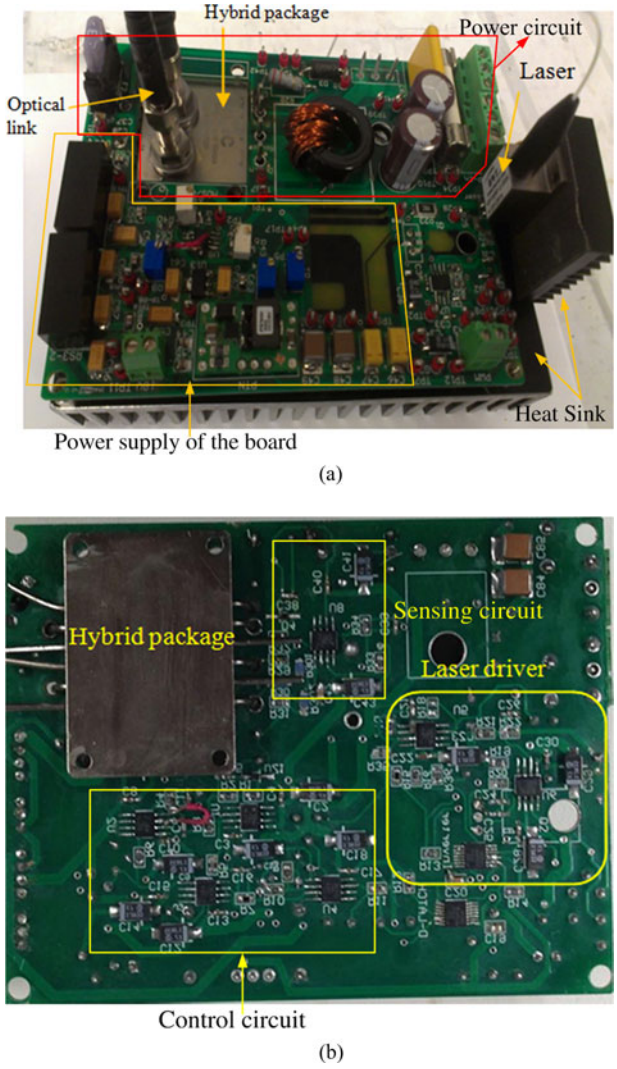

Fig. 11. Fabricated test set up: (a) top side of the board which includes the power circuit, laser and power-supply circuits; and (b) bottom side of the board which includes the control circuit, sensing circuits, and laser driver.

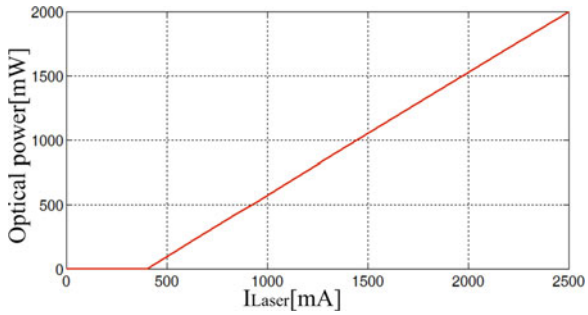

Fig. 12. Output optical power of the laser at the end of the fiber-optic cable as a function of laser current (I_{Laser}).

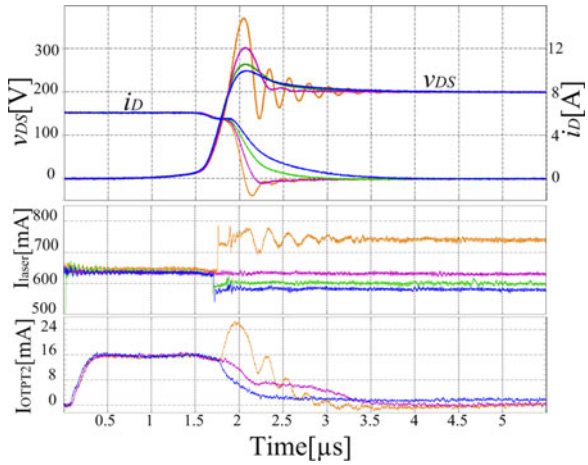

Fig. 13. Measured turn-off waveform of v_{DS}, i_D, I_{laser}, and I_{OTPT2} with varied di_D/dt (of 30, 20, 10, and 5 A/μs) and the fixed dv_{DS}/dt (of 600 V/μs).

voltage overshoot and oscillation reduce as well. Fig. 13 validates that, the di_D/dt of M1 is dynamically controlled by controlling the current flowing through OTPT2 (i.e., I_{OTPT2}). The latter is dependent on the optical intensity of OTPT2, which in turn, is dependent on the output-current level of the laser driver.

The gate-to-drain and input capacitances of the SiC power MOSFETs are dramatically lower than their Si counterparts with the same rating (i.e., compare the $C_{\mathrm{GD}} = 77\,\mathrm{pF}$ and $C_{iss} = 21\,nF$ of IXFL32N120P, to C_{GD} and C_{iss} of M1). Therefore, a higher gate resistance (which can be 10 to 20 times higher) is needed for a SiC MOSFET to ensure that it has the same dv_{DS}/dt as compared to its Si counterpart, following (3). A higher gate resistance in the case of having the same dv_{DS}/dt, results in a dramatically lower gate current. Furthermore, during the discharging time of the C_{iss} of M1, OTPT acts like a constant current-source and prevents the current spike of the gate current which is a common phenomenon in the conventional gate drive circuits, as shown in Fig. 13. This behavior also results in a longer turn-off delay for M1. If the traditional gate drive with the fixed gate resistance is used, the gate voltage exponentially decreases by the following equation until it reaches the Miller voltage (V_{Miller}):

$$v_{\mathrm{GS}} = V_{CC}.e^{-t/R_G C_{iss}}. \tag{23}$$

In (23), V_{CC} is the gate bias voltage. Therefore, the delay time for this case is derived by the following equation:

$$t_{d-R} = R_G C_{iss}.\ln\left(V_{CC}/V_{\mathrm{Miller}}\right). \tag{24}$$

In (24), t_{d-R} is the turn-off delay time of M1 with the conventional fixed-gate-resistance method. On the other hand, if the OTPT is used in the gate circuit of M1, the gate current (i_G) is derived using following relation:

$$i_G = \frac{V_{CC} - V_{\mathrm{Miller}}}{t_{d-O}}.C_{iss} = \frac{V_{\mathrm{Miller}}}{R_G}. \tag{25}$$

In (25), t_{d-O} is the turn-off delay time of M1 in the case of using the proposed optical approach. Therefore, t_{d-O} is derived using the following equation:

$$t_{d-O} = R_G C_{iss}.\frac{V_{CC} - V_{\mathrm{Miller}}}{V_{\mathrm{Miller}}}. \tag{26}$$

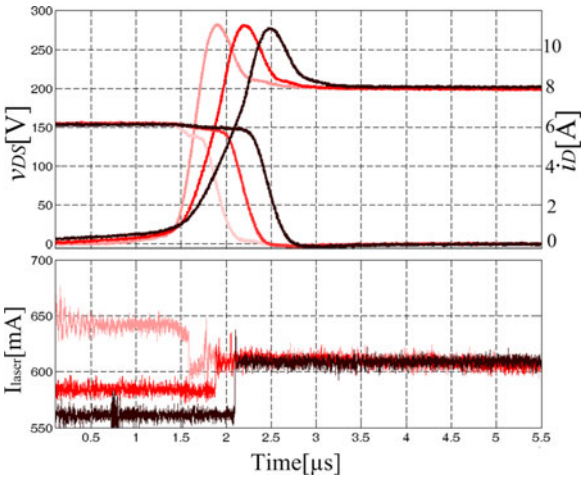

Fig. 14. Measured turn-off waveforms of $v_{\rm DS}$, i_D, and $I_{\rm laser}$ with varied $dv_{\rm DS}/dt$ (of 530, 330, and 225 V/μs) and a fixed di_D/dt (of 17 A/μs).

Consequently, the ratio of the turn-off delay times for the two cases is:

$$\frac{t_{d-O}}{t_{d-R}} = \frac{(V_{CC}/V_{\rm Miller}-1)}{\ln(V_{CC}/V_{\rm Miller})}. \tag{27}$$

Following (27) and depending on the load current of M1, one can conclude that using the proposed approach the turn-off delay of M1 is 1.3–2.5 times longer as compared to the conventional fixed-resistance method, in the case of having the same $dv_{\rm DS}/dt$.

The experimental results for the independent optical control of the $dv_{\rm DS}/dt$ of M1 with the fixed i_D/dt, are shown in Fig. 14. The turn-off $dv_{\rm DS}/dt$ increases by increasing the current level of the laser driver in this region. The onset of transition from $dv_{\rm DS}/dt$ to di/dt control region is set properly by control circuit for different values of $dv_{\rm DS}/dt$. This ensures the independent $dv_{\rm DS}/dt$ and di_D/dt controls. Therefore, one is able to control the drain-to-source voltage slope in the $dv_{\rm DS}/dt$ control region without affecting the controllability of slope of the drain current in the di_D/dt control region, as shown in Fig. 14. The output-current levels of the laser driver remain the same in the di_D/dt control region which lead to the same resistance for OTPT2. Therefore, di_D/dt and overvoltage for all the cases are same according to (3) and (4). di_D/dt can be adjusted regardless of the value of $dv_{\rm DS}/dt$ in the $dv_{\rm DS}/dt$ control region by varying the current level of the laser driver.

The test circuit and control block diagram for the high-side-drive case is shown in Fig. 15. Experimental results for the independent optical control of the di_D/dt of M1 with the fixed $dv_{\rm DS}/dt$, as well as, the independent optical control of the $dv_{\rm DS}/dt$ of M1 with the fixed di_D/dt for the case of high-side drive are shown respectively in Fig. 16 and Fig. 17. The results are similar to the results of the case of low-side drive, which validates the feasibility of the proposed control for high-side drive cases, as long as an isolated voltage for the gate bias of M1 is provided.

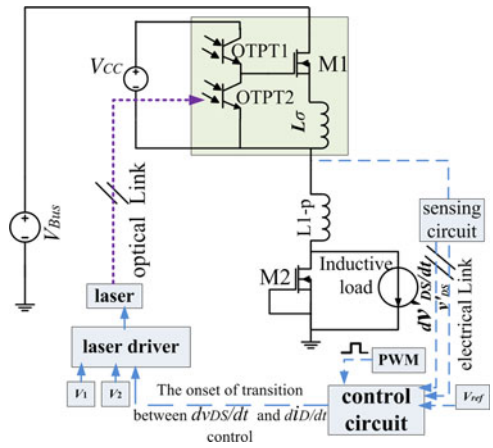

Fig. 15. Test circuit and control block diagram for the high-side drive case.

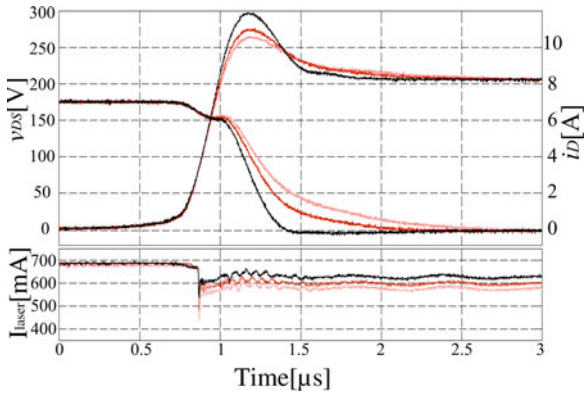

Fig. 16. Measured turn-off waveform of $v_{\rm DS}$, i_D, $I_{\rm laser}$, and $I_{\rm OTPT2}$ with varied di_D/dt (of 16, 11.5, and 9.5 A/μs) and the fixed $dv_{\rm DS}/dt$ (of 770 V/μs) for the high-side drive case.

To verify the control circuit adaptability in different operating conditions, the $v_{\rm DS}$, i_D, and $I_{\rm Laser}$ are measured for variation of the bus voltage and load current as depicted in Figs. 18 and 19, respectively. The control circuit naturally initiates the transition from the $dv_{\rm DS}/dt$ to the di_D/dt control region by changing the current levels of the laser driver at the desired points, taking into account the loop delay as discussed earlier. According to (1) and (4), and considering the same load and thermal conditions, the output-current level of the laser driver remains approximately constant in each of the regions of control for different bus voltages to attain the same $dv_{\rm DS}/dt$ and di_D/dt, as shown in Fig. 18. Similarly, to attain the same $dv_{\rm DS}/dt$ and di_D/dt for different load currents, $I_{\rm Laser}$ decreases in each region of control as the load current increases, which is depicted in Fig. 19.

The measured turn-off switching losses and energy obtained using a conventional approach to drive the gate and that obtained using the proposed optically switched transition controller are shown in Figs. 20 and 21, respectively. The intensity of the optical beam for OTPT2 is kept constant in the two regions of control for the conventional approach, similar to the proposed approach in [22]. This emulates the discharge of the gate of

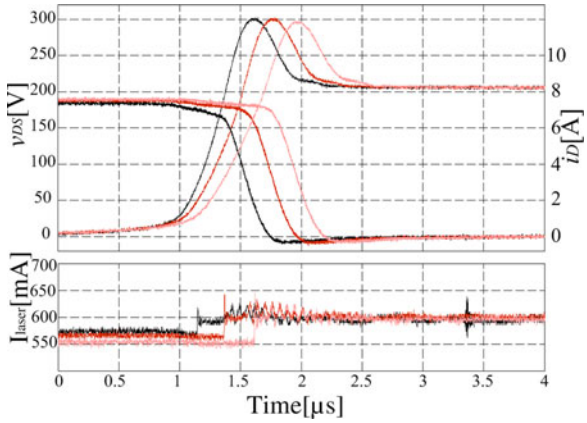

Fig. 17. Measured turn-off waveforms of $v_{\rm DS}$, i_D, and $I_{\rm laser}$ with varied $dv_{\rm DS}/dt$ (of 430, 350, and 300 V/μs) and a fixed di_D/dt (of 20 A/μs) for the high-side drive case.

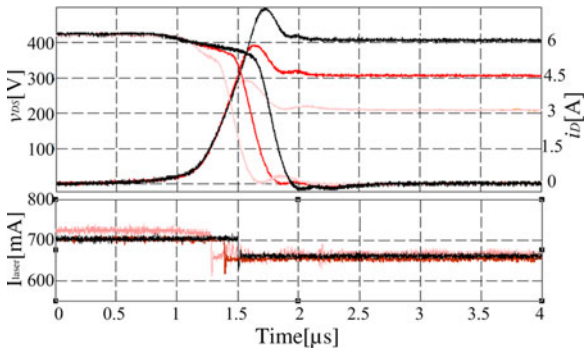

Fig. 18. Measured turn-off waveform of $v_{\rm DS}$, i_D, and $I_{\rm laser}$ for different bus voltages with the fixed $dv_{\rm DS}/dt$ of 525 V/μs and the fixed di_D/dt of 20 A/μs.

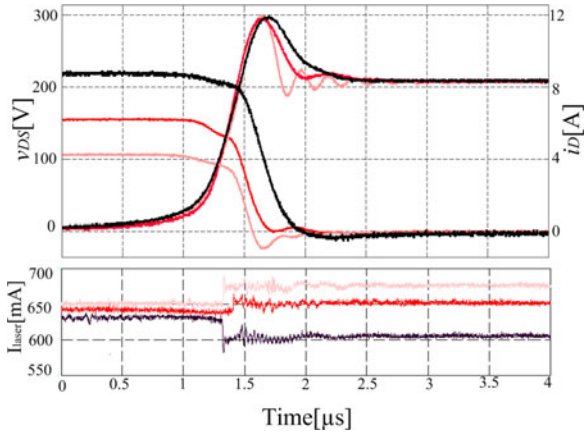

Fig. 19. Measured turn-off waveforms of $v_{\rm DS}$, i_D, and $I_{\rm Laser}$ for different load currents with the fixed $dv_{\rm DS}/dt$ of 340 V/μs and the fixed di_D/dt of 20 A/μs.

M1 under condition of fixed gate resistance for $dv_{\rm DS}/dt$ and di_D/dt regions of control. In contrast, for the proposed controller, the $dv_{\rm DS}/dt$ and di_D/dt are so adjusted such that not only the peak-power loss and switching energy are reduced but the peak overvoltage stress is decreased as well, compared to

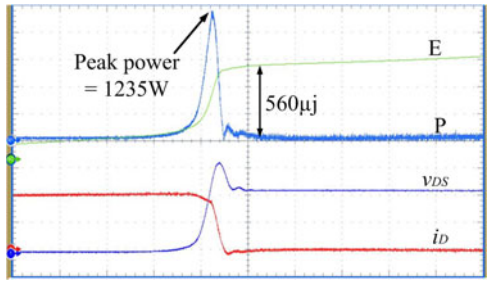

Fig. 20. Measured switching loss and energy for conventional approach [24] to drive the gate. In this approach, the intensity of the optical beam for OTPT2 is kept constant in the $dv_{\rm DS}/dt$ and di_D/dt regions of control. E = switching energy (200 μj/div), P = switching power loss (258 W/div), $v_{\rm DS}$ is 90 V/div, i_D is 3 A/div and time division is 800 ns/div.

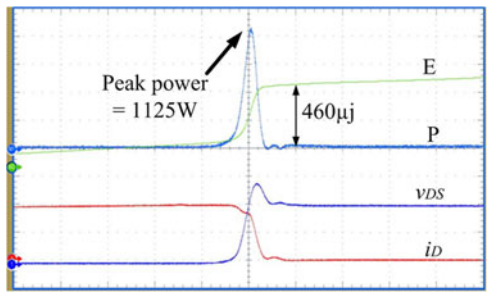

Fig. 21. Measured switching loss and energy for the proposed optical-transition controller. The peak-power reduction of 110 W along with the switching-energy reduction of 100 μJ and 17% reduction of overvoltage stress are achieved using the optical-transition controller as compared to the conventional gate drive. E = switching energy (200 μj/div), P = switching power loss (258 W/div), $v_{\rm DS}$ is 100 V/div, i_D is 3 A/div and time division is 800 ns/div.

the results obtained using the conventional approach. Using the new controller, the peak-power reduction of 110 W along with the switching-energy reduction of 100 μJ and 15 V reduction of overvoltage stress are achieved. This is achieved in part by increasing the $dv_{\rm DS}/dt$. Furthermore, the di_D/dt is slightly decreased to reduce the peak voltage stress and minimize the adverse effect of the reduction of di_D/dt on the switching loss.

In the case of maximum di_D/dt of 43A/μs in 6 A load current and using the flowchart of Fig. 10, the Δt is selected to be 150 ns and implemented in the control circuit. Therefore, the $dv_{\rm DSmax}/dt$ is calculated to be equal to 1030 V/μs in 200 V, based on the explained procedure in Section II-A and using (21). The minimum $dv_{\rm DSmax}/dt$ for the case of maximum di_D/dt is around 200 V/μs, and the minimum di_D/dt for the case of maximum $dv_{\rm DSmax}/dt$ is around 4.7 A/μs, based on Figs. 9, 5, and using (1), (4), and (15).

IV. Conclusion

A novel unified independent dv/dt and di/dt control of an optically triggered (OT) hybrid PSD, which contains a SiC MOSFET as the main PSD and two GaAs-based OTPTs as the gate driver, has been outlined. It has been shown that the unified control of turn-off $dv_{\rm DS}/dt$ and di_D/dt is achieved by modulating the optical intensity of the OTPT2 using a single

circuit. Independent control of $dv_{\rm DS}/dt$ and di_D/dt is achieved by predicting the onset of transition between the corresponding control regions using the unified control circuit. The control circuit performance has been verified through experimental results over different operating conditions including variation of $dv_{\rm DS}/dt$, di_D/dt, load current, and bus voltage. It has been shown that, the proposed optical controller is able to attain the desired switching-transition behavior using independent control of $dv_{\rm DS}/dt$ and di_D/dt, which is not possible in the conventional gate drivers. Although the new optical controller is designed for an OT PSD, the control concept is also applicable for ET PSDs where the delay of the event feedback-loop is significant compared to the total duration of the switching transition.

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