On-Chip Compensated Wide Output Range Boost Converter with Fixed-Frequency Adaptive Off-Time Control for LED Driver Applications

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***Abstract*—An on-chip compensated wide output range boost converter with fixed-frequency adaptive off-time current-mode control is presented. The small signal characteristic of the boost converter with current-mode control is reviewed, and an adaptive current sensing technique is proposed to reduce the variation of phase margin at different output voltages. On-chip compensation is achieved with a Type II compensator. Adaptive off-time control is adopted for its fast response and no need for slope compensation, while its disadvantage of varying switching frequency is eliminated by the proposed off-time generator. The IC controller was fabricated in a 0.5 μm 2P3M BCD 40 V process. Measurement results confirm that an output range of 5.5 V $\sim$ 36 V with an input voltage of 5 V is achieved. The switching frequency is fixed at 1 MHz with a variation of $\pm$1%. The measured peak efficiency and maximum output power are 92.9% and 8.6 W, respectively. For a load step of 200 mA using a 3.3-μH inductor and a 20-μF output capacitor, overshoot and undershoot of the load transient responses are smaller than 1% of the output voltage.**

***Index Terms*—Adaptive current sensing (ACS), adaptive off-time control, boost converter, current-mode control, fixed switching frequency, frequency locking, on-chip compensation, small signal analysis, wide output range.**

I. Introduction

PORTABLE electronic systems, such as cellular phones, digital cameras, and notebooks widely use light emitting diodes (LEDs) for display, backlight, or other illumination purposes. Series connection of the LEDs can provide identical LED currents for uniform brightness without the need for ballast resistors and expensive factory calibration [1], [2]. For these applications, boost converters are used to step up the battery voltage to drive LEDs with high power efficiency. As the forward voltage of each LED is usually around 3 V, a boost converter with a wide output range is needed to meet different illumination requirements with different numbers of LED connected in series [2], [3]. However, due to the more complicated characteristics of the power stage, boost converters are more difficult to design than buck converters, especially for a wide output range. A variety of control methods have been explored, such as pulse-width modulation (PWM) control [4]–[9], hysteretic control [10], [11], and constant on/off time control [12]–[19].

PWM boost converters can be designed to work in either the voltage-mode or the current-mode, and be stabilized by appropriate loop compensation. For voltage-mode control, there are two conjugate poles and one right half plane (RHP) zero in the duty-cycle to the output voltage transfer function [20], [21], and a complicated Type III compensation network is needed. The locations of the conjugate poles and the zero vary with the duty-cycle that depends on both the input and the output voltages, and it is very challenging to stabilize the converter over a wide range of output voltage by using an on-chip compensator that can only give fixed locations of poles and zeroes. In [4], leading edge modulation is employed to turn the RHP zero to be a left-half-plane (LHP) zero, but a large equivalent series resistance of the output capacitor is required that increases the output voltage ripple. In [5], a tri-state boost converter is proposed to eliminate the RHP zero, but it is only effective for a particular duty-cycle, and operating with a long freewheel period also degrades the power efficiency.

With PWM current-mode control, the RHP zero stays unchanged but the conjugate poles are spilt into a low-frequency pole and a high-frequency pole [21]–[23], making loop compensation simpler. However, the locations of the low-frequency pole and the RHP zero still vary with the input and the output voltages. It is not uncommon that boost converters are compensated with off-chip components [6], [7]. The values of those components could be adjusted according to the input and output voltages to ensure loop stability and to improve transient responses. However, off-chip components increase the area of PCB and the cost as well as design complexity for the users. In [8], an adaptive compensation concept is proposed to achieve on-chip compensation for a wide duty-cycle range, but the values of the inductor and the output capacitor have to be different for different duty-cycles. In [9], an adaptive P compensator is proposed to simplify loop compensation, but the load and line

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regulations are quite large that limit its applications. Moreover, for PWM current-mode control with duty-cycle larger than 0.5, a compensation ramp has to be added to suppress subharmonic oscillation [24]–[26]. However, the compensation ramp has to be large enough to handle the worst case, which makes the system act more like voltage-mode control and degrades the transient responses [25], especially for applications that need a wide output range.

Hysteretic voltage-mode control is widely used in buck converters for its fast transient response and no need for loop compensation [27], [28]; however, it is proved in [29] that there is no feasible operating region for a hysteretic voltage-mode boost converter. As a result, only hysteretic current-mode control [10], [11] can be implemented; but a freewheeling period is needed in [10] that degrades the power efficiency, and an auxiliary winding of inductor is required in [11] that increases the cost.

Recently, constant on/off-time current-mode control [30] is getting more attention in designing boost converters [12]–[19] for its fast transient response and no need for a compensation ramp. However, a conventional constant on/off-time control results in a varying switching frequency that causes electromagnetic interference (EMI) noise problem. Adaptive on/off-time methods [12]–[15] and frequency locking methods [17], [19], [28], [31]–[33] are two main techniques to solve this problem. A detailed review on these techniques can be found in [19]. The first technique is to make the on/off-time dependent on certain related system parameters to reduce the variation of switching frequency, but the result is still not as good as PWM control, especially when the converter has to work in both the continuous conduction mode (CCM) and the discontinuous conduction mode (DCM). The second technique achieves a fixed switching frequency at the expense of a complicated circuit structure. Besides the issue of a varying switching frequency, the constant on/off-time control has to deal with the difficulty of loop compensation similar to the PWM current-mode control.

Compared to constant on-time control, constant off-time control is adopted here as it is more convenient for boost converters to sense the inductor current when the power switch is on [30]. An adaptive current sensing (ACS) technique is proposed [18] to achieve a wide output range operation with on-chip compensation. According to the proposed ACS technique, the inductor current sensing gain is designed to be inversely proportional to the output voltage, and the phase margin is kept nearly constant when the output voltage changes. To avoid the EMI problem in constant off-time control, a novel off-time generator (OTG) that integrates the adaptive off-time method and the frequency locking method together is also proposed that could make the switching frequency constant under all conditions.

This paper is organized as follows. In Section II, the small signal characteristic of the boost converter with constant off-time current-mode control is reviewed, and the proposed ACS technique is introduced. The issue of varying switching frequency will also be discussed. In Section III, the system architecture of the proposed boost converter and the implementation of key circuit blocks are discussed. In Section IV, measurement results are presented to verify the proposed techniques; and conclusions are drawn in Section V.

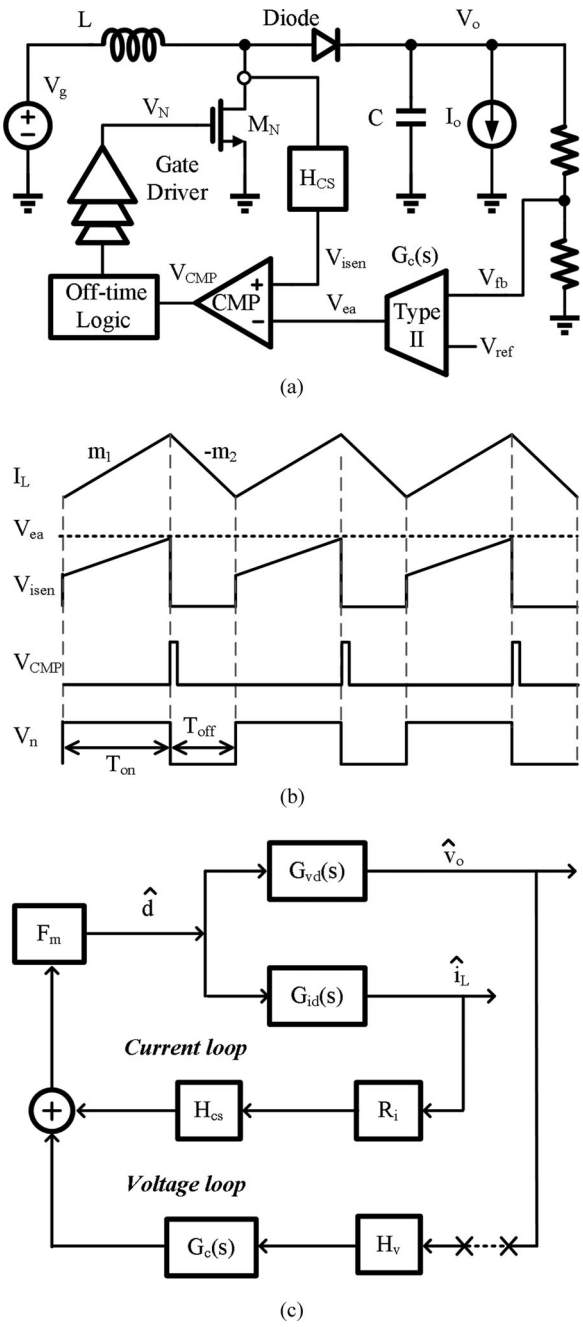


Fig. 1. Constant off-time current-mode controlled boost converter: (a) block diagram; (b) timing diagram; (c) small signal model.

II. System Considerations of Wide Output Range Boost Converter

A. Small Signal Analysis of Constant Off-Time Current-Mode Controlled Boost Converter

Fig. 1(a) shows the architecture of a constant off-time current-mode controlled boost converter. Its timing diagram is shown in Fig. 1(b). The trigger signal of the off-time is generated by comparing the sensed inductor current signal $V_{\rm isen}$ and the output signal of the compensator V_{ea}. With constant off-time control, the duration of the off-time is predefined as a fixed

value, while the on-time is modulated by the feedback loop to regulate the output voltage V_o. Fig. 1(c) shows the small-signal model of the constant off-time current mode control in CCM, which is similar to that of the conventional PWM current-mode control [30]. The transfer functions of the voltage loop and the current loop are given by [20], [22]

$$T_v(s) = H_v F_m G_c(s) G_{vd}(s) \quad (1)$$

$$T_i(s) = R_i H_{cs} F_m G_{id}(s) \quad (2)$$

where $G_{vd}(s)$ and $G_{id}(s)$ are the transfer functions of the duty-cycle to the output voltage and the duty-cycle to the inductor current, respectively, as shown in [20]. The feedback ratio H_v is to set the desired output voltage, which is equal to $V_{\rm ref}/V_o$ ($V_{\rm ref}$ is the reference voltage). The transfer function of the compensator is $G_c(s)$. For current-mode control, Type II compensator is usually adopted [16], [19], and it consists of a low-frequency pole $-p_c$ and a higher frequency zero $-z_c$ with dc gain A_c, as is given by

$$G_c(s) = A_c \frac{1+\frac{s}{z_c}}{1+\frac{s}{p_c}}. \quad (3)$$

The inductor current (I_L) is sensed and converted to a voltage signal by the sensing resistor R_i, and further be processed to achieve a gain of H_{cs}. The modulator gain is F_m as derived in [30]. With the current loop closed, the loop gain transfer function can be derived as [22], [23]

$$T_{\rm loop}(s) = \frac{T_v(s)}{1+T_i(s)} = \frac{H_v F_m G_c(s) G_{vd}(s)}{1+R_i H_{cs} F_m G_{id}(s)}. \quad (4)$$

With current-mode control, the inductor can be regarded as a voltage controlled current source, and the complex pole-pair (with resonance frequency $\omega_o = 1\sqrt{LC}$) of the power stage is spilt into two real poles ($-p_1$ and $-p_2$) [23]. The high frequency pole $-p_2$ is around the switching frequency f_{sw}, which can be neglected in the analysis for simplicity [8], [16]. Hence, the power stage can be approximated as a first-order system with the dominant pole $-p_1$ and the RHP zero $+ z_{\rm rhp}$. Then, (4) can be simplified as [21], [25]

$$T_{\rm loop}(s) = G_c(s) \times T_u(s) = \frac{A_c\left(1+\frac{s}{z_c}\right)}{1+\frac{s}{p_c}} \times \frac{A_{\rm pwr}\left(1-\frac{s}{z_{\rm rhp}}\right)}{\left(1+\frac{s}{p_1}\right)} \quad (5)$$

where $T_u(s)$ is defined as the uncompensated loop gain, and

$$p_1 = \frac{2}{RC} = \frac{2I_o}{V_o C} \quad (6)$$

$$z_{\rm rhp} = \frac{D'^2 R}{L} = \frac{V_g^2}{V_o I_o L}. \quad (7)$$

From (6) and (7), it is observed that the locations of $-p_1$ and $+ z_{\rm rhp}$ vary with the output voltage V_o and the load current I_o. It is still challenging to operate the converter over a wide operation range with a fixed on-chip compensator [6]–[9].

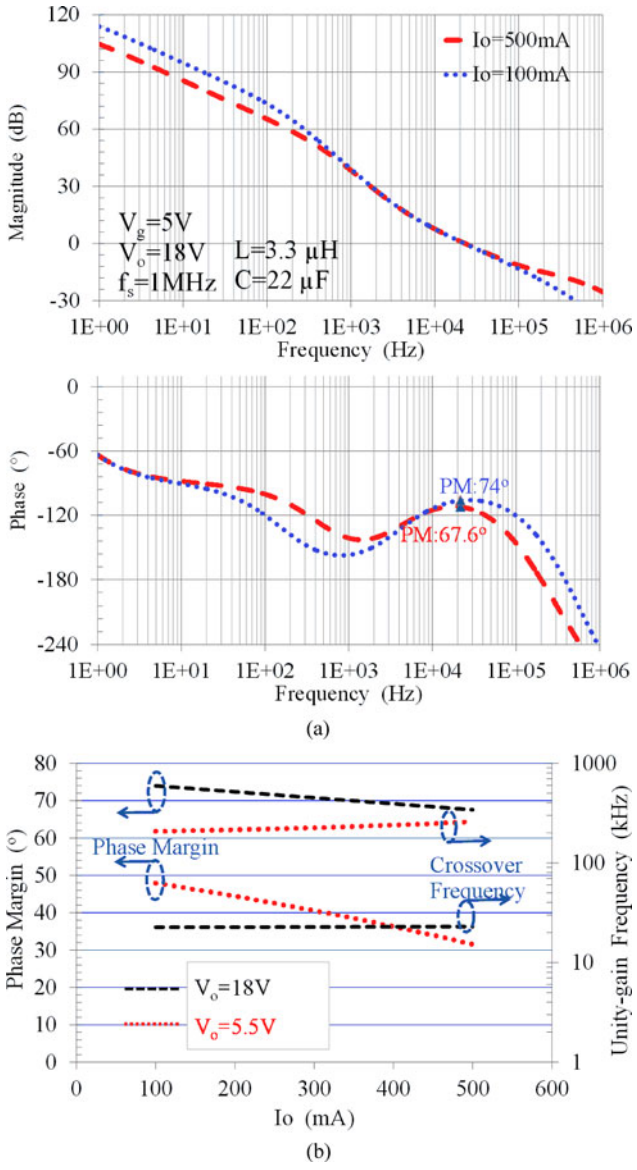


Fig. 2. (a) Bode plots of the converter with different I_o; (b) variations of the phase margin and the crossover frequency that against I_o.

From (4), the dc loop gain can be computed as

$$T_0 \approx \frac{G_{vd0} H_v A_c F_m}{G_{id0} H_{cs} F_m} = \frac{A_c V_g V_{\rm ref}}{I_o H_{cs} V_o}. \quad (8)$$

It can be observed that the dc gain of the system is inversely proportional to I_o, while the location of $-p_1$ is proportional to I_o. As a result, their product is nearly constant, and the phase margin is mainly influenced by $+z_{\rm rhp}$ when I_o changes. A larger I_o results in a lower frequency $+z_{\rm rhp}$, and thus a smaller phase margin. Fortunately, the maximum load current is around 350 mA for LED driver applications [2], [34]. By properly designing the compensation network, it is not difficult to cover such a load range. Fig. 2(a) shows the Bode plots of (4) at different load currents (100 and 500 mA) if the compensator

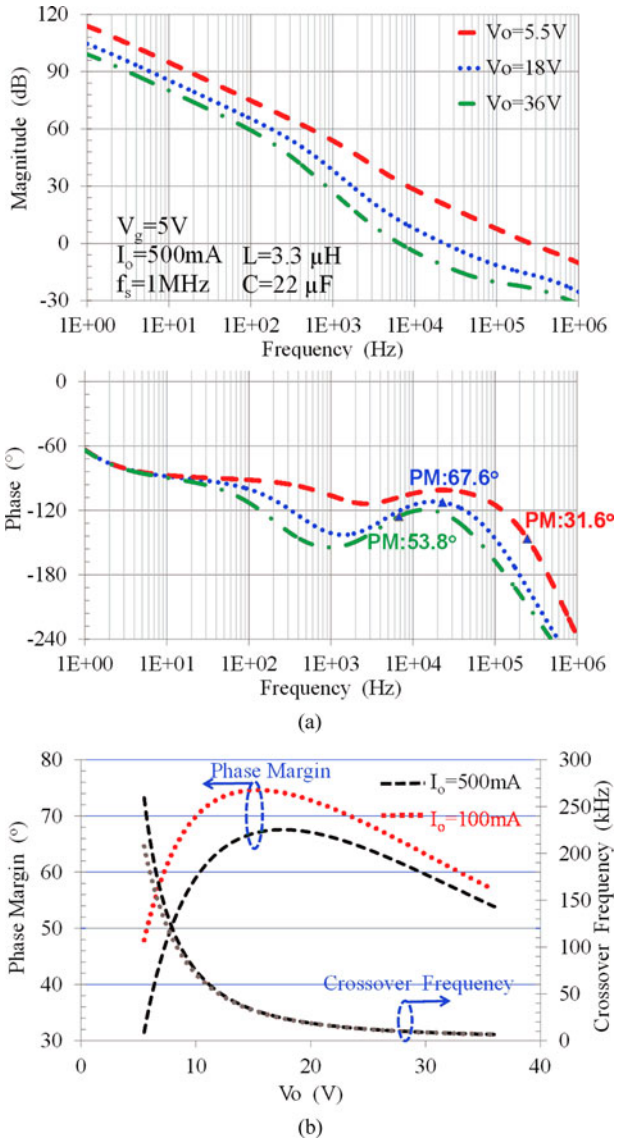


Fig. 3. (a) Bode plots of the converter with different V_o; (b) variations of the phase margin and the crossover frequency that against V_o.

is designed for $V_o = 15$ V, and the phase margins are good. Fig. 2(b) further shows that the variations of the phase margin and the unity-gain frequency $\omega_{\rm UGF}$ against I_o are quite small. However, the output voltage has to change from about 6 (two LEDs in series) to 35 V (ten LEDs in series). It is difficult to obtain good phase margin over such a wide output range with a fixed on-chip compensator. As shown in Fig. 3, the variation of phase margin is about 40° and special techniques are needed to solve this problem.

B. ACS Technique

From (6) and (7), we learn that p_1 and $z_{\rm rhp}$ vary with V_o, but their ratio does not

$$\frac{p_1}{z_{\rm rhp}} = \frac{2I_o/V_oC}{V_g^2/V_oI_oL} = \frac{2I_o^2L}{V_g^2C}. \tag{9}$$

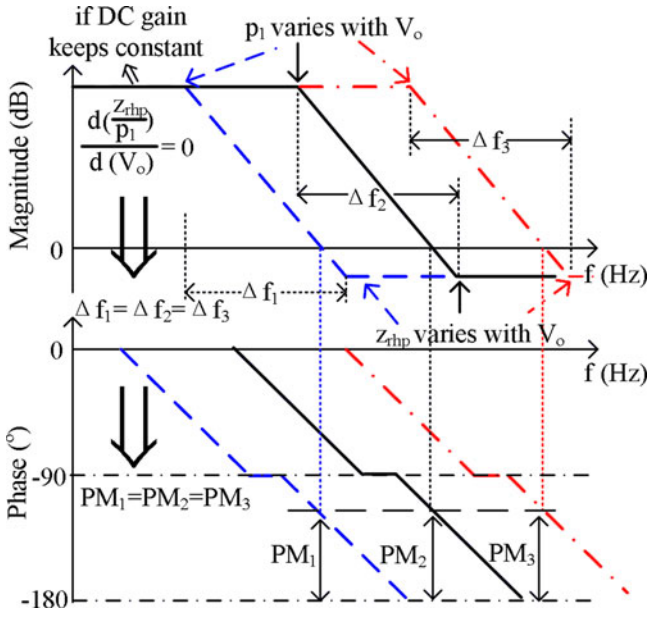


Fig. 4. Bode plots of the system with a pole and a RHP zero.

As shown in Fig. 4, consider the uncompensated loop gain $T_u(s)$ with p_1 and $z_{\rm rhp}$, and $p_1/z_{\rm rhp}$ is kept constant. If the dc gain is also kept constant, the phase margin will be kept constant, and only the unity-gain frequency is changed when V_o changes. Then, the design strategy of the compensator is to place the pole p_1 and the zero z_c such that $p_c < p_1 < z_c < \omega_{\rm UGF} < z_{\rm rhp}$. The LHP zero z_c should be sufficiently low with respect to the unity-gain frequency ω_{UGF}, and ω_{UGF} be sufficiently low with respect to the RHP zero $z_{\rm rhp}$ to achieve a relatively large phase margin. Then, the phase shift introduced by p_c will be cancelled out by z_c, and the effect of the compensator will be the same at different V_o. Finally, the dc loop gain T_o should be kept constant to reduce the change in phase margin for different V_o. According to (8), H_{cs} is designed to be inversely proportional to V_o, and we label this as the ACS technique. Fig. 5 shows the Bode plots of (4) with different V_o by using ACS. Compared to Fig. 3, the change in the dc gain is reduced and the phase margin is kept approximately constant for different V_o. Hence, a wide output range boost converter with an on-chip compensator is realized.

Next, consider DCM operation with the inductor current returns to zero every cycle, and the loop gain transfer function is given by [19], [33]

$$T_{\rm loopDCM} = \frac{H_v A(s) F_m \left(\frac{2V_o}{2M-1}\sqrt{\frac{M-1}{\rm KM}}\right)}{1 + sRC\frac{M-1}{2M-1}} \tag{10}$$

where $M = V_o/V_g$ and $K = 2L/RT_s$. The power stage working in DCM is reduced to a first-order system with no RHP zero. The system is in fact easier to be stabilized than when operating in CCM, and Type II compensation can still be used. Fig. 6 shows the Bode plots of (10) when the converter is working in DCM with a load current of 10 mA. The converter still has good stability over a wide output range.

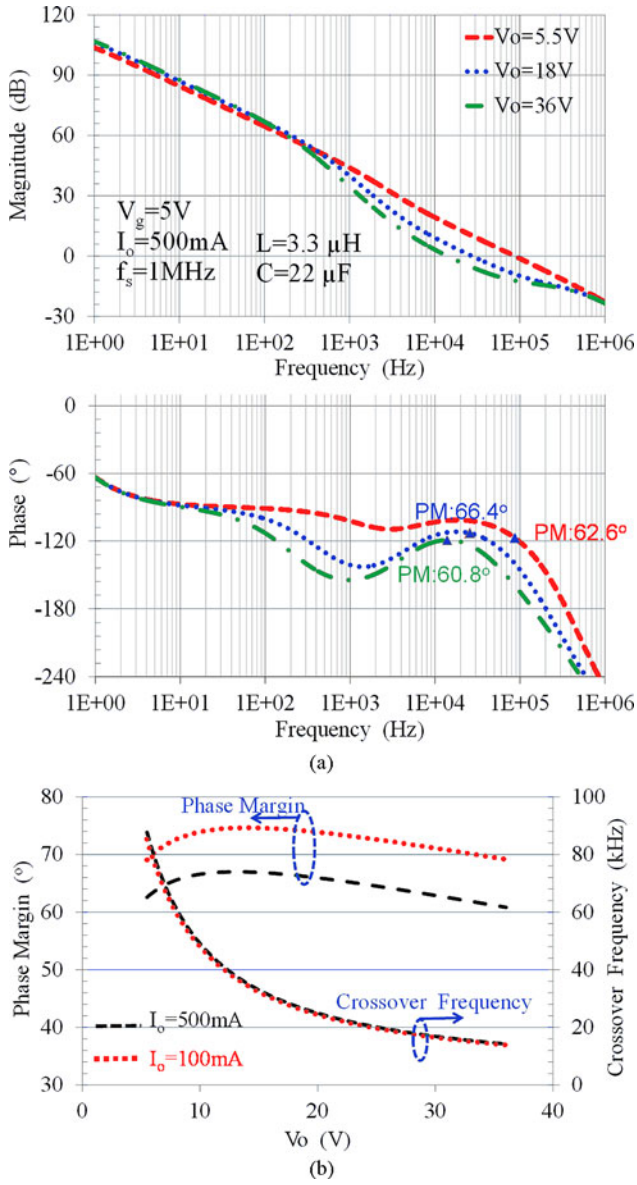


Fig. 5. (a) Bode plots of the converter with different output voltages with ACS; (b) variations of the phase margin and the crossover frequency that against V_o.

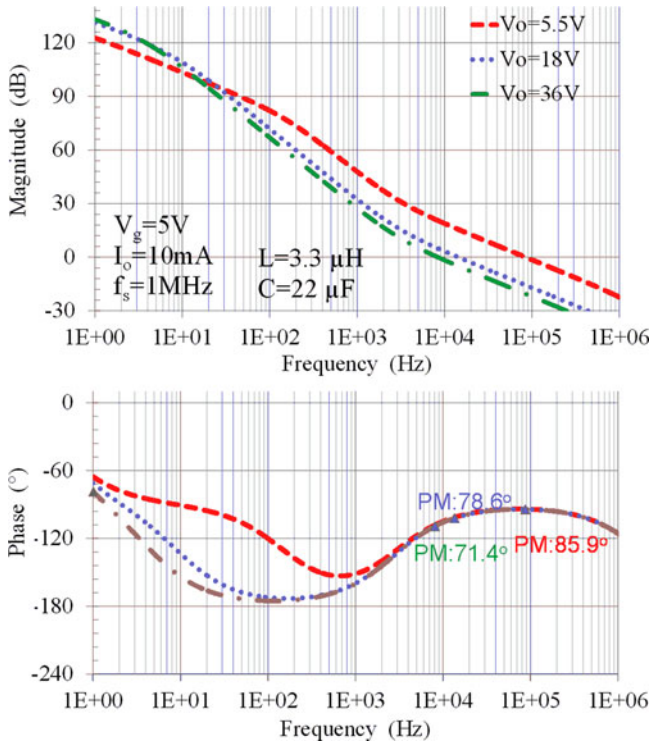


Fig. 6. Bode plots of the converter under V_o when operating in DCM.

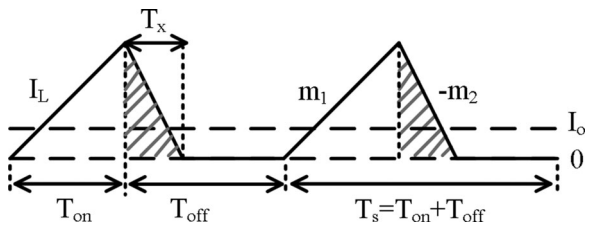


Fig. 7. Inductor current waveform in DCM.

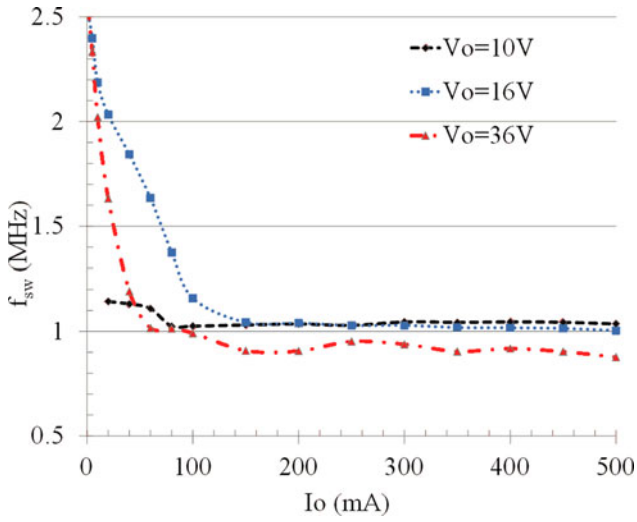


Fig. 8. Simulated switching frequency with different V_o and I_o.

C. Frequency Variation Issue in Off-Time Control

Compared to PWM control, the main disadvantage of constant off-time control is that the switching frequency varies with the working conditions, especially when the converter is required to work in both CCM and DCM. In CCM, the relationship between the switching period T_s and the off-time period $T_{\rm off}$ in the ideal case is given by

$$T_s = T_{\rm off} \times \frac{V_o}{V_g}. \tag{11}$$

The idea of adaptive off-time can be explained by (11). If $T_{\rm off}$ is designed to be proportional to V_g and be inversely proportional to V_o, T_s will be a constant. However, due to the parasitic resistors of the power transistor, the inductor and layout routing,

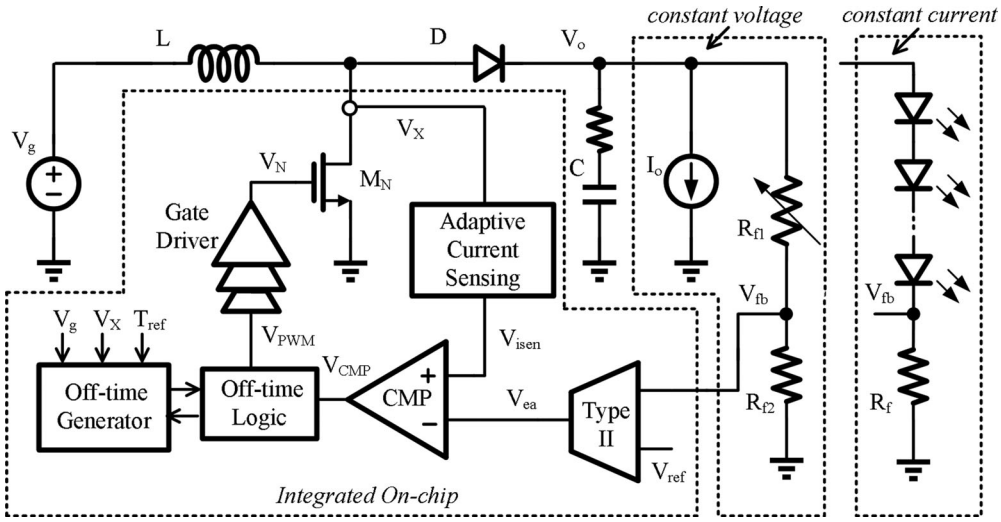


Fig. 9. System architecture of the wide output range boost converter.

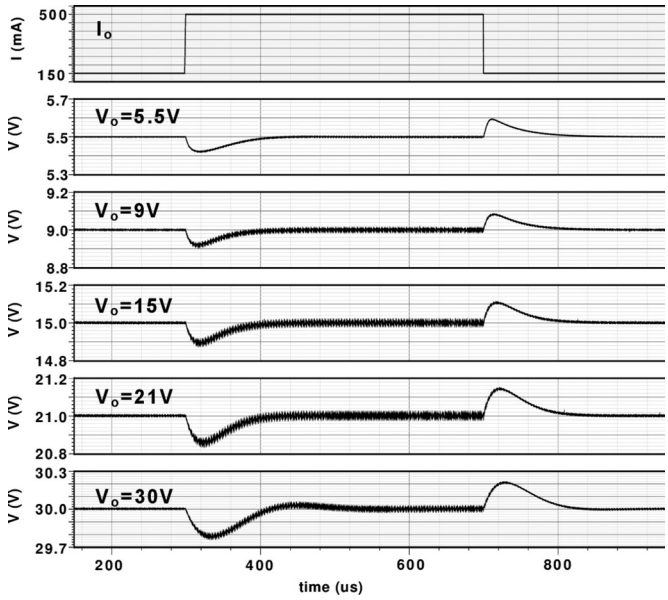


Fig. 10. Simulated transient response with ACS technique.

the switching frequency cannot be truly constant. The situation gets worse when the converter operates in DCM, as shown in Fig. 7. Using charge balance analysis [29], we have

$$I_o \times T_s = \frac{1}{2} \times T_x \times m_2 T_x. \tag{12}$$

Meanwhile

$$T_s = T_x \times \frac{V_o}{V_g} + (T_{\text{off}} - T_x). \tag{13}$$

$$T_s = [I_o L (V_O - V_g) + V_g^2 T_{\text{off}} + \sqrt{I_o^2 L^2 (V_o - V_g)^2 + I_o L (V_o - V_g) V_g^2 T_{\text{off}}}]/V_g^2. \tag{14}$$

With (12) and (13), the relationship between T_s and T_{off} at DCM is derived as (14). It shows that T_s depends on V_g and V_o as well as I_o and L. Moreover, T_s decreases with I_o, which means that the converter will operate at a higher frequency when the load current is lower, worsening the power efficiency at light load.

Fig. 8 shows the transistor-level Cadence simulation results of f_{sw} with different V_o and I_o by using adaptive off-time control. The target switching frequency is 1 MHz and the off-time is designed according to (11). The switching frequency is well controlled when the system is working in CCM; however, it varies a lot in DCM, as predicted by (14). Therefore, the technique of frequency locking is preferred as the bandwidth of the locking loop is quite low that does not affect the stability of the main loop [19], [33]. However, the switching frequency when unlocked can vary by one order even in CCM only according to (11), and thus, the frequency locking circuit should have a large locking range. Luckily, by employing an adaptive off-time method the frequency variation could be reduced. Hence, in this design, a new OTG that combines the adaptive off-time method and the frequency locking method is proposed to fix the switching frequency for the whole output and load range. The circuit implementation of the proposed OTG will be discussed next.

III. Proposed System Architecture and Circuit Implementation

A. System Architecture

Fig. 9 shows the simplified system architecture of a wide output range boost converter with adaptive off-time current-mode control. The Type II compensator proposed in [18] is fabricated on-chip to achieve a tight regulation and stabilize the converter. With the proposed OTG, the switching frequency is fixed for the whole operation range to avoid EMI problem and efficiency degradation. The boost converter can also be used to drive several LEDs in series with a constant current by using a sensing resistor [2]. As shown in Fig. 9, the voltage drop on the

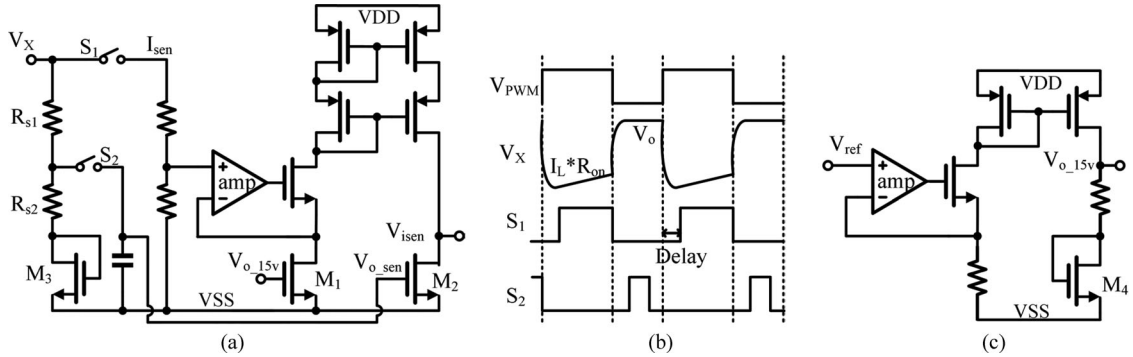


Fig. 11. (a) ACS circuit; (b) timing diagram; and (c) generation circuit of $V_{o_{15V}}$.

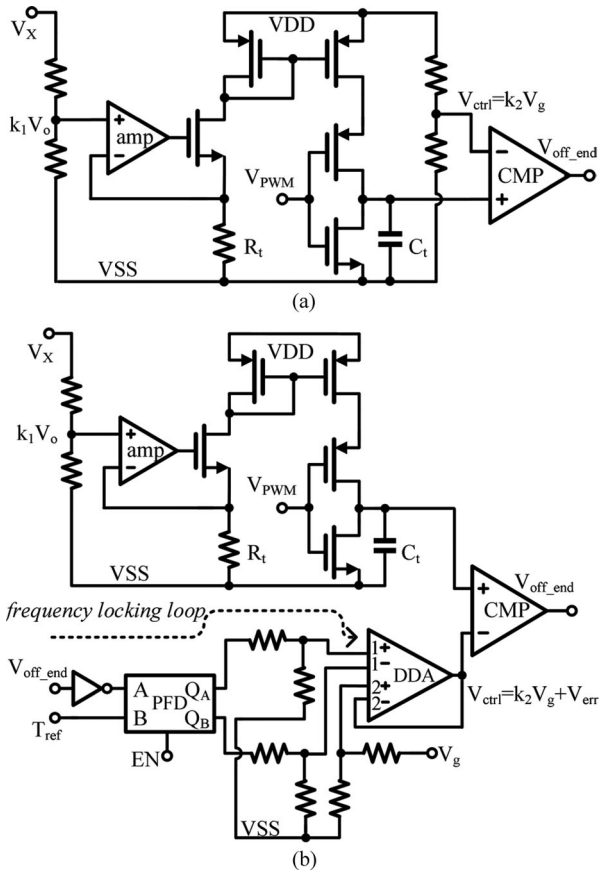


Fig. 12. (a) Conventional adaptive OTG; (b) proposed OTG.

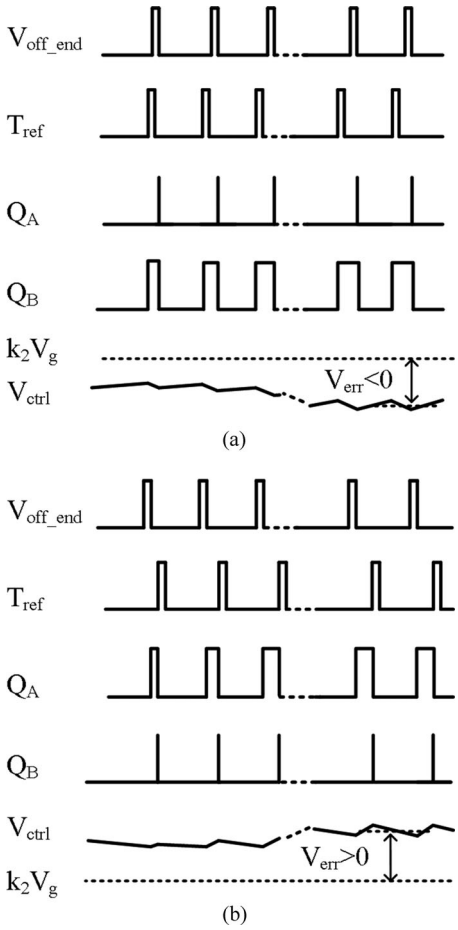


Fig. 13. Operation principle of proposed OTG: (a) when $T_s > T_{\rm ref}$; (b) when $T_s < T_{\rm ref}$.

sensing resistor R_f is regulated by the feedback loop, and so does the current that flows in LEDs and R_f. A more advanced design of LED driver with dimming control using the proposed techniques can be found in [35].

B. ACS Circuit

Fig. 10 shows the schematic of the ACS circuit and its operation principle. The PWM signal is processed to generate two sampled signals: S_1 and S_2. S_1 is used to sense the inductor current when the power transistor M_N is ON, and S_2 is used to sample and hold the voltage of the node V_X when M_N is OFF; with $V_x \approx V_o$ in this phase, sensing V_x to obtain V_o saves one pad. Delay is added between the PWM signal and S_1 to block the switching noise when M_N switches from OFF to ON.

Transistors $M_1 \sim M_3$ have the same aspect ratio and are matched in the layout so that they have the same threshold voltage V_{tn}. M_1 and M_2 work in the deep linear region and serve as resistors with values that are approximately inversely proportional to their respective overdrive voltages. M_3 is

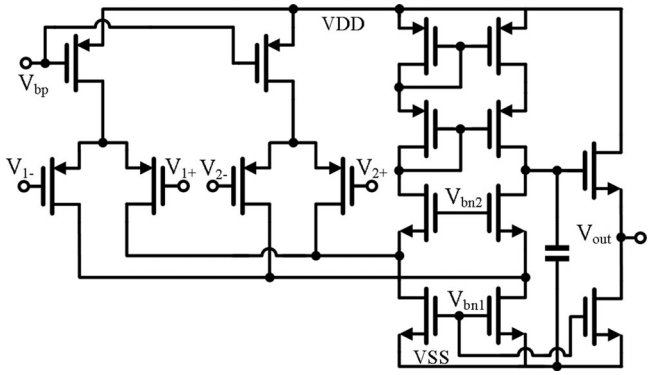


Fig. 14. Schematic of DDA.

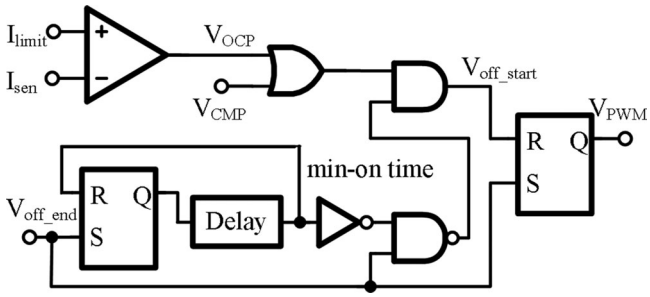


Fig. 15. Constant off-time logic circuit.

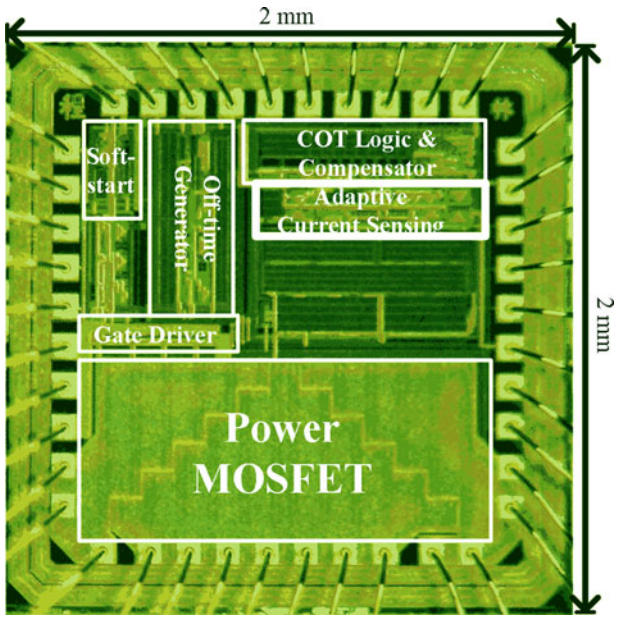


Fig. 16. Chip micrograph.

diode-connected and sinks a very low current such that its overdrive voltage is negligible and $V_{gs3} \approx V_{tn}$. The voltage $V_X - V_{tn}$ is scaled down by a resistor divider consists of R_{s1} and R_{s2}. As $V_o \gg V_{tn}$, the sensed output voltage $V_{\text{o\_sen}}$ can be expressed as

$$V_{o\_\text{sen}} = \frac{1}{k}\left(V_o - V_{gs3}\right) + V_{gs3} \approx \frac{1}{k}V_o + V_{\text{th}} \qquad (15)$$

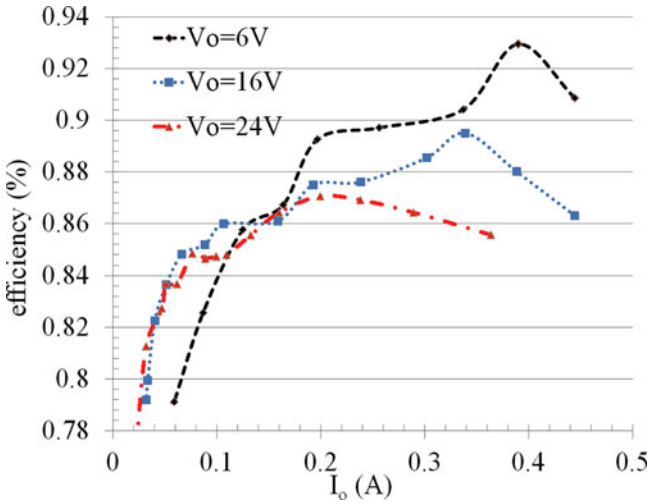


Fig. 17. Measured power efficiency.

where $k = R_{s2}/(R_{s1} + R_{s2})$. The on-resistance of M_2 in the deep linear region is then given by

$$R_{\text{on2}} = \frac{1}{k_n\left(V_{o\_\text{sen}} - V_{\text{th}}\right)} = \frac{k}{k_n}\frac{1}{V_o} \propto \frac{1}{V_o}. \qquad (16)$$

The bias voltage of M_1 ($V_{\text{o\_15V}}$) is generated by the circuit in Fig. 10(c). The reference voltage V_{ref} or any other dc voltage that is available in the system can be used to generate a voltage level according to (15) by setting $V_o = 15$ V, so that the on-resistance of M_1 is

$$R_{\text{on1}} = \frac{1}{k_n\left(\frac{1}{k}V_{o\_15\text{v}} + V_{\text{th}} - V_{\text{th}}\right)} \propto \frac{1}{V_{o\_15\text{v}}}. \qquad (17)$$

Therefore, the current sensing gain H_{cs} is obtained to be inversely proportional to V_o as required by (8)

$$H_{\text{cs}} \propto \frac{R_{\text{on2}}}{R_{\text{on1}}} = \frac{V_{o\_15\text{V}}}{V_o}. \qquad (18)$$

Next, the converter is designed for $V_o = 15$ V using the analysis in the previous section, and the system will keep a good phase margin in a wide output range as shown in Fig. 5. Fig. 11 shows the simulated transient response when I_o changes between 150 and 500 mA. It can be observed that the converter has consistent responses and good stability in different V_o.

C. OTG and Logic Circuit

Fig. 12 shows the schematic of both the conventional adaptive OTG and the proposed OTG. The main difference between the proposed frequency locking circuit and those reported in [26]–[29] is in integrating the adaptive off-time method to reduce the locking range that simplifies the design of the locking circuit. The integration of adaptive off-time into the OTG is achieved by using a differential difference amplifier (DDA) [36]. It works

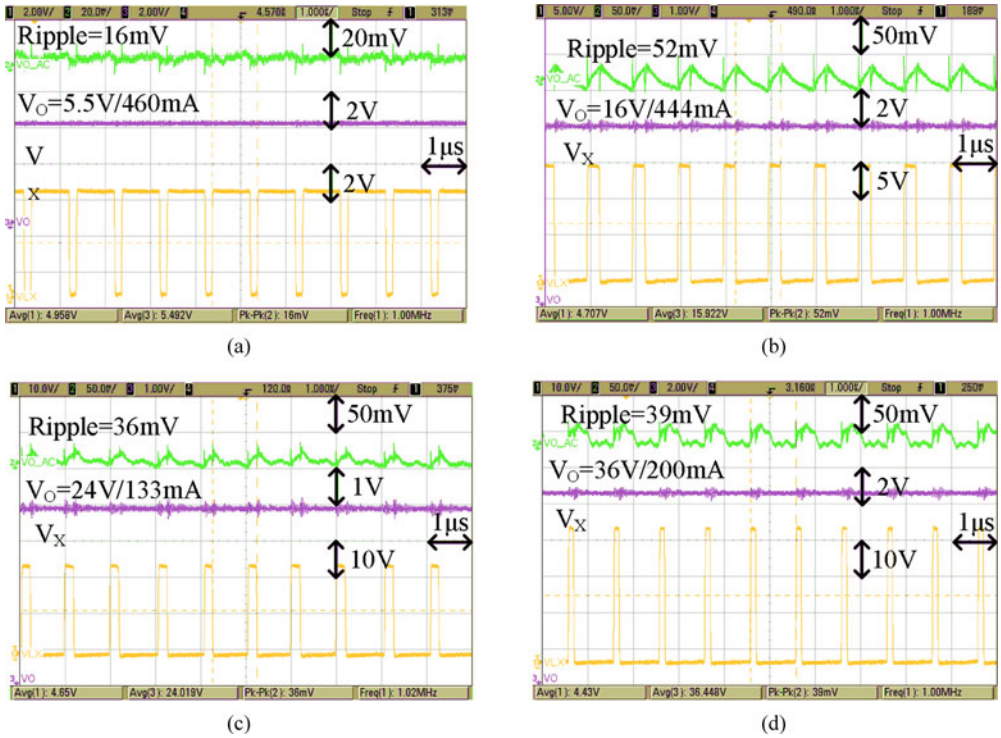


Fig. 18. Measured steady-state waveforms under different V_o: (a) $V_o = 5.5$ V; (b) $V_o = 16$ V; (c) $V_o = 24$ V; (d) $V_o = 36$ V.

as a charge pump and a low-pass filter for the frequency locking loop, and converts the error signal to be the control signal for adjusting the off-time and also ensures the stability of the locking loop. With different input and output voltages, the off-time is adjusted accordingly to reduce the switching frequency variation and to relieve the workload of the frequency locking loop. The schematic of the DDA is shown in Fig. 14. It is a folded-cascode amplifier with two input pairs. Due to negative feedback, we have [36]

$$v_{1+} - v_{1-} = -\left(v_{2+} - v_{2-}\right). \tag{19}$$

In the proposed OTG, the duration of the off-time is controlled by the voltage level of the node $V_{\rm ctrl}$, which is consisted by two parts: $k_2 V_g$ and $V_{\rm err}$. The part of $k_2 V_g$ is used to make the off-time to be proportional to V_g, and to relieve the locking range of the frequency locking loop. The part of $V_{\rm err}$ is an error correction voltage generated from the frequency locking loop. Without the frequency locking loop, $V_{\rm ctrl} = k_2 V_g$ and the switching frequency f_{sw} still varies with working conditions. With the frequency locking loop, the frequency error between the reference frequency $1/T_{\rm ref}$ and f_{sw} is detected by the phase frequency detector and then it is converted to $V_{\rm err}$ by DDA. As shown in Fig. 13, if $T_s (= 1/f_{sw}) > T_{\rm ref}$, it means that the current off-time is too long, the pulse width of Q_B will be increased and then $V_{\rm ctrl}$ will fall to shorten the off-time until $T_s = T_{\rm ref}$. Similarly, if $T_s < T_{\rm ref}$, the pulse width of Q_A will be increased and $V_{\rm ctrl}$ will rise to lengthen the off-time. Thus, f_{sw} is regulated to be $1/T_{\rm ref}$, and the off-time can be expressed as

$$T_{\rm off} = \frac{\left(k_2 V_g + V_{\rm err}\right) C_t}{k_1 V_o / R_t}. \tag{20}$$

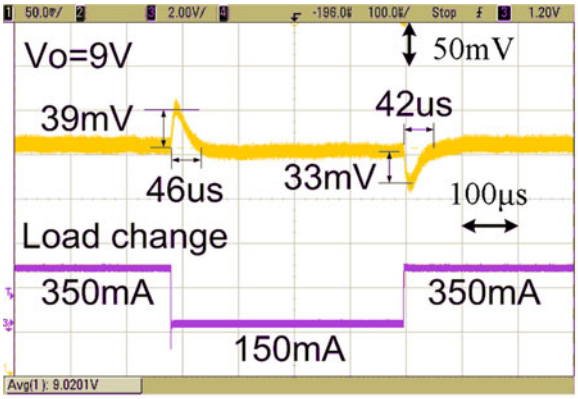
Fig. 15 shows the logic circuit of the off-time control. Overcurrent protection is also easily implemented in this design. A minimum on-time of around 100 ns generated by the delay cell is inserted into the logic to enhance noise immunity and avoid wrong switching actions.

IV. Measurement Results

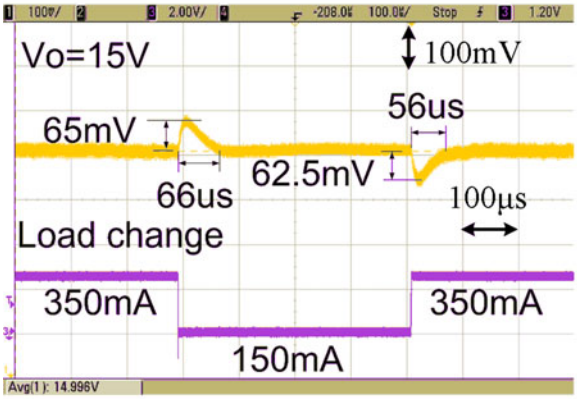
The proposed adaptive off-time current-mode controlled boost converter was fabricated in a 0.5 μm 2P3M BCD 40 V process. The chip micrograph is shown in Fig. 16. The chip area is 2 mm $\times$ 2 mm including the testing pads. All of the following results are measured at $V_g = 5$ V with a 3.3-μH inductor and a 20-μF output capacitor.

Fig. 17 shows the measured power efficiency when V_o is set to be 6 V, 16 V, and 24 V, respectively. A peak power efficiency of 92.94% is obtained when V_o is 6 V with a load current of 390 mA. As the switching loss of the node V_X and the conduction loss are both increased with V_o [37], a higher V_o results in a lower power efficiency, especially at heavy load. The measured maximum output power is 8.6 W when V_o is 24 V with a load current of 360 mA. Fig. 18 shows the measured steady-state waveforms of V_X and V_o that ranged from 5.5 to 36 V. The converter can work stably with small output ripples and fixed switching frequency of 1 MHz.

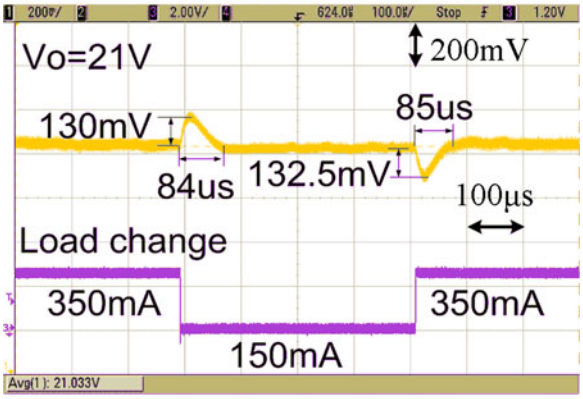
Fig. 19 shows the measured transient response with a load current step of 200 mA. It is observed that the converter



(a)



(b)



(c)

Fig. 19. Measured load transient response when under different V_o: (a) $V_o = 9$ V; (b) $V_o = 15$ V; (c) $V_o = 21$ V.

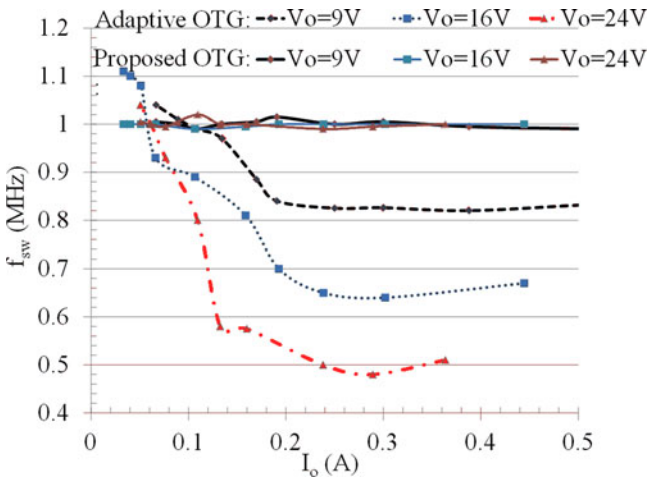


Fig. 20. Measured switching frequency with different output voltages and load currents.

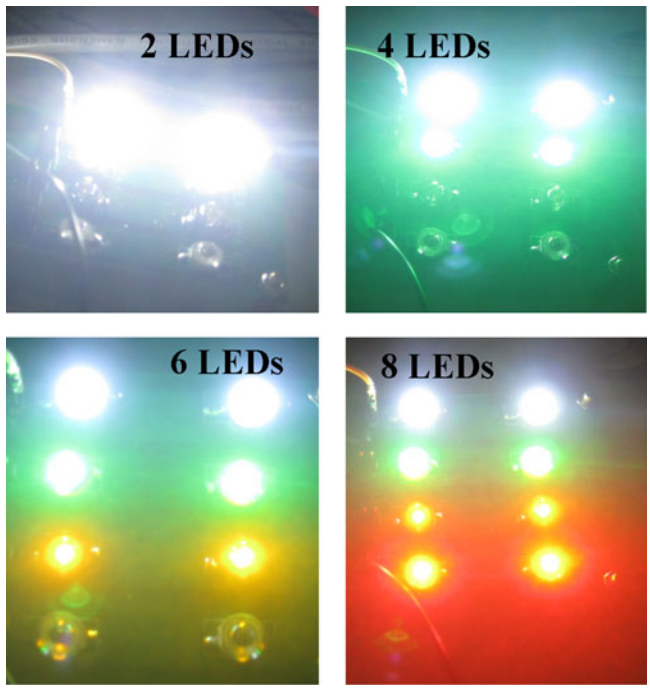


Fig. 21. LED driver test.

achieved consistent responses and good stability with different output voltages, which indicates that the phase margins were nearly constant over a wide output range. The measured overshoots/undershoots were smaller than 1% of the output voltage. A tight regulation can also be observed from Fig. 19.

Fig. 20 shows the comparison of the switching frequency due to the proposed OTG and the conventional adaptive OTG at different load currents. For the proposed OTG, the switching frequency is well controlled at the target frequency in both CCM and DCM. The range is from 990 to 1010 kHz, which translates into a $\pm 1\%$ error only. However, it varied with the load current significantly when using the conventional adaptive-off time control, especially when the converter was working in DCM.

The designed boost converter was also measured to drive LEDs with constant current as shown in Fig. 9. Fig. 21 shows that the converter successfully drove two to eight LEDs in series at a load current of 300 mA.

V. Conclusion

This paper presents an adaptive off-time current-mode controlled boost converter. An adaptive current-sensing technique is proposed to achieve wide output range with on-chip compensation. An OTG is proposed to fix the switching frequency in the whole operation range. Measurement results from fabricated chips verified the effectiveness of the proposed design. This boost converter is suitable for LED driver applications.

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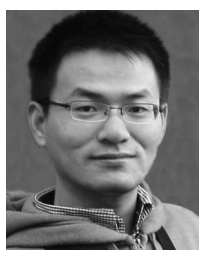

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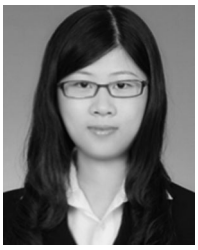

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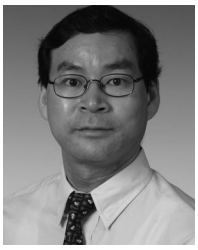

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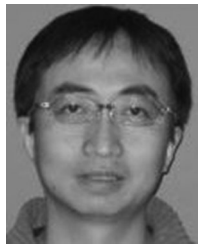

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