Modeling and Triple-Loop Control of ZVS Grid-Connected DC/AC Converters for Three-Phase Balanced Microinverter Application

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***Abstract*—This paper presents modeling and triple-loop control for a high-efficiency three-phase balanced inverter for using in grid-connected two-stage microinverter applications. An average signal model based on a synchronous rotation frame for a three-phase four-wire inverter has been developed. The inner current loop consists of a variable frequency bidirectional current mode (VFBCM) controller which regulates output filter inductor current thereby achieving ZVS, improved system response, and reduced grid current THD. Active damping of the *LCL* output filter using filter inductor current feedback is discussed along with small signal modeling of the proposed control method. Since the dc-link capacitor plays a critical role in two-stage microinverter applications, a dc-link controller is implemented outside of the two current control loops to keep the bus voltage constant. Finally, based on a two-stage 400-W prototype, simulation and experimental results are presented to verify the validity of the theoretical analysis, the effectiveness and feasibility of the proposed VFBCM control strategy.**

***Index Terms*—*LCL* filter, microinverter, three-phase four-wire inverter, total harmonic distortion (THD), two-stage, variable frequency bidirectional current mode control (VFBCMC), zero-voltage switching (ZVS).**

NOMENCLATURE

$U_{\rm pv}$	Output voltage of PV panel.
$I_{\rm pv}$	Output current of PV panel.
$U^*_{\rm bus}$	Bus voltage reference.
$U_{\rm bus}$	Bus voltage.
f_s	Switching frequency.
I^*_x	Inverter-side inductor current reference of phase $\rm x = a, b, c$.
i_{1x}	Inverter-side current of phase $\rm x = a, b, c$.
i_{2x}	Grid-side current of phase $\rm x = a, b, c$.
$U_{\rm gx}$	Grid voltage of phase $\rm x = a, b, c$.
L_1	Inverter-side inductor.
L_2	Grid-side inductor.
C_f	Output capacitor of the inverter stage.
U	Normalized inverter output voltage.
δ	Normalized grid voltage.
X	Normalized state vector $\hat{I}_{\rm 1d}\ \hat{I}_{\rm 1q}\ \hat{I}_{\rm 2d}\ \hat{I}_{\rm 2q}\ \hat{U}_{\rm cfd}\ \hat{U}_{\rm cfq}$.
Y	Normalized grid current $\hat{I}_{\rm 2d}\ \hat{I}_{\rm 2q}$.
$t_{\rm on}$	Turn-on time of inverter stage.
$t_{\rm off}$	Turn-off time of inverter stage.
$i_{\rm ref}$	Reference of the injected grid current.
$i_{\rm lower}$	Lower limit value of the comparator.
I_m	Output rms current of the three-phase inverter.
B_0	Comparator value at lower limit or upper limit U_m the sinusoidal voltage across C_f.
$i_{\rm dc}$	Bus current.
D	Duty cycle of the inverter stage.
T_s	Switching period of the inverter stage.
R_i	Current sensing coefficient.

Manuscript received December 6, 2013; revised February 25, 2014 and April 10, 2014; accepted May 26, 2014. Date of publication June 12, 2014; date of current version November 3, 2014. This work was supported by DoE Award No. EE0003176, and NSF Award No. 1156633, and FESC project. Recommended for publication by Associate Editor M. Liserre.

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Digital Object Identifier 10.1109/TPEL.2014.2329278

I. INTRODUCTION

WITH ever dwindling natural resources and increasing demands for power, the need to seek out viable alternative sources of the renewable energy is urgent. Solar energy offers extraordinary merits including environmental neutrality, unlimited availability, and low cost capable of competing with conventional sources due to technology advances and mass production. Over the last 10 years, the photovoltaic industry has averaged an annual growth rate of over 25% [1]. The microinverter has witnessed recent market success due to unique features such as improved energy harvesting, improved system efficiency, lower installation costs, plug-N-play operation, and enhanced flexibility and modularity. The microinverter sector has grown from a niche market to mainstream especially in the U.S.

Microinverters with high-frequency transformers can be grouped into three architectures based on the dc-link configurations: dc-link, pseudo-dc-link and high-frequency ac [2]–[5]. Due its high efficiency, power density, reliability, and excellent grid connection functionality, the two-stage microinverter consisting of an isolated dc–dc converter stage and an inverter stage with a dc link as shown in Fig. 1 is getting increased attention from academia and industry. The first stage tracks the maximum power point of the PV panel and the second stage is used to generate a synchronized sinusoid current with a unity power factor for injection into the grid. Since a large value dc link capacitor is required to balance the reactive power in single-phase microinverters, electrolytic capacitors are widely used. Unfortunately, electrolytic capacitors typically have a

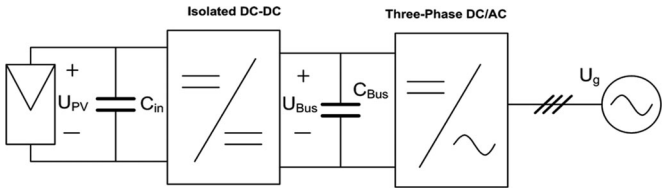

Fig. 1. Two-stage grid-connected PV inverter.

limited lifetime of 1000–12 000 h at 105 °C operating temperature which negatively impacts system reliability [6], [7]. Although some researchers have developed techniques to reduce the required capacitance in order to allow the use of longer lifespan film capacitors [8]–[13], these approaches have the drawbacks of either complicating the inverter topology and control or reducing the overall efficiency. Assuming further expansion of the microinverter market from low power to high power, a three-phase microinverter using film capacitors in the dc link will be discussed in this paper.

The topology used in most three-phase three-wire grid-connected microinverters is the pulse width-modulated voltage-source inverter in which switching losses are a dominant factor. Some sort of soft switching technique is often proposed in order to reduce these losses and a number of papers [14]–[21] have been published over the last 30 years describing various methods of achieving this. Unfortunately, most approaches are not widely used in industry due to complexity, reliability, and cost issues. In a three-phase four-wire inverter, the three phases are symmetrical with respect to the neutral wire and analysis can be performed on a single phase. If the inverter-side inductor current is bidirectional, ZVS can be achieved and switching losses can be dramatically reduced. The detailed operating modes of the three-phase four-wire inverter which we presented in [22] and [23] are beyond the scope of this paper.

Recently, the *LCL* filter has received a lot of attention due to its superior high-frequency attenuation compared to single inductor or *LC* filters. In this paper, a *LCL* filter is used between the grid and the inverter output stage. Filter resonance is an important issue to be considered in the design of the current controller for grid-connected inverters employing *LCL* output filters. There have been many solutions to the *LCL* resonance problem proposed in the literature [24]–[29]. These approaches can be either passive or active. One passive method of damping the *LCL* filter resonance is to insert a resistor in series with the filter capacitor. This method is relatively simple and highly reliable but it results in power loss and decreased high frequency performance. Active damping provides virtual resistance in the filter network via a control algorithm in order to suppress the resonance of the *LCL* filter. Compared to passive damping, active damping is more effective and efficient. Among various methods, active damping with capacitor current feedback has been broadly used due to its simple implementation [25], [26], [28]. Referring to paper [22], inverter-side inductor current sensing is required in order to achieve ZVS by controlling its bidirectional current. Active damping of the inverter-side inductor using a current feedback controller is described in this paper.

In order to achieve high efficiency and low injected grid current THD in the inverter, a VFBCMC is employed to determine switch ON/OFF. Although the state space averaging technique is widely used in inverter modeling, there have been some limits in its application due to the nonlinear characteristics of the duty cycle in variable switching frequency inverters [33], [34]. A small signal model of an inverter stage with a VFBCMC in the inner current control loop is derived from the PWM switch model [30]–[34]. A PI controller design based on the rotating synchronized frame [35] for the injected grid current control is extensively applied in three-phase three-wire inverters to reach a zero steady-state error. Modeling and control of a three-phase inverter with *L* or *LCL* filter is presented in [36]. In order to use PI controller for the injected grid current closely tracking its reference, the small signal model for the three-phase four wire inverter is built into the rotating synchronized frame. The step–by-step design of a triple-loop controller for inverter output filter inductor current, injected grid current, and dc link voltage based on small signal modeling is presented.

The remainder of this paper is organized as follows. System description of three-phase dual-stage microinverter is illustrated in Section II. Small signal modeling of three-phase four-wire inverter is presented in Section III. Section IV will discuss a triple-loop control design based on the equivalent circuit and average modeling of the second stage. Simulation and experimental results are given to verify the modeling and triple-loop controller design in Section V. Conclusion is given in Section VI.

II. Three-Phase Grid-Tie Inverter System

A. Description of Dual-Stage Architecture

In order to provide galvanic isolation, various isolated dc–dc converters for high step up applications have been proposed. Recently, the *LLC* resonant topology has become attractive due to its desirable characteristics such as high efficiency and natural ZVS/ZCS commutation. Therefore, a full-bridge *LLC* resonant converter is employed in the first stage to achieve high efficiency and track the maximum power point of each PV panel. The proposed soft switching technique [22] shown in Fig. 2 simplifies the inverter topology and reduces the cost since it does not require any auxiliary components. The body capacitors of the main MOSFETs and the converter-side inductor L_1 are combined to form a resonant circuit. The inverter-side inductor current is intentionally bidirectional within a switching cycle to generate ZVS conditions during commutation. Meanwhile, the average inductor current is controlled to produce a sinusoidal current in L_1. The proposed soft switching technique is suitable for microinverter applications where the switching losses are usually dominant. Based on the above, Fig. 2 shows the proposed high-efficiency microinverter architecture with both-stage zero voltage switching consisting of a full-bridge *LLC* resonant dc–dc step up converter and three-phase four-wire soft switching inverter.

B. System Control Description

An overall control diagram for two-stage three-phase four-wire microinverter PV system is shown in Fig. 3. The voltage

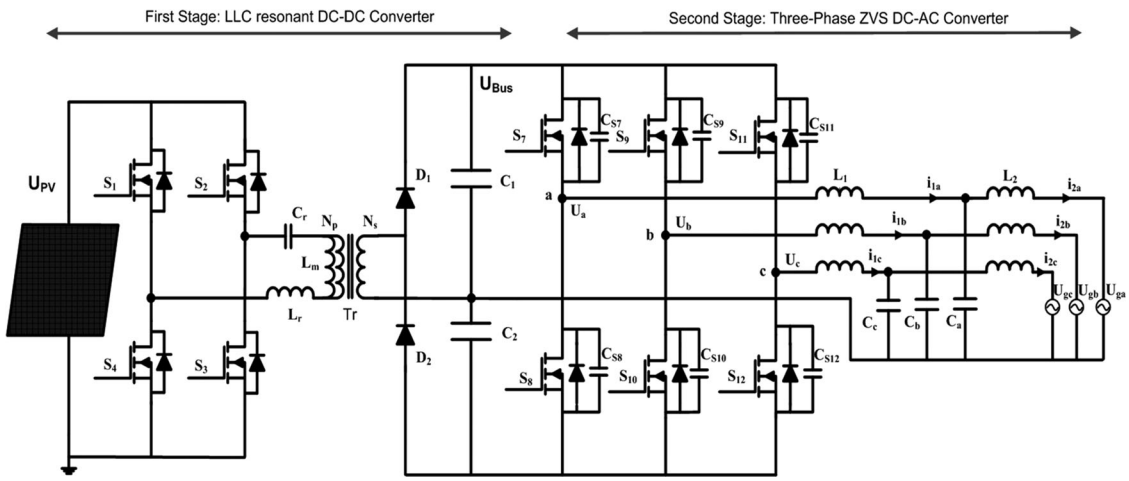

Fig. 2. Two-stage three-phase four-wire grid-tie inverter PV system.

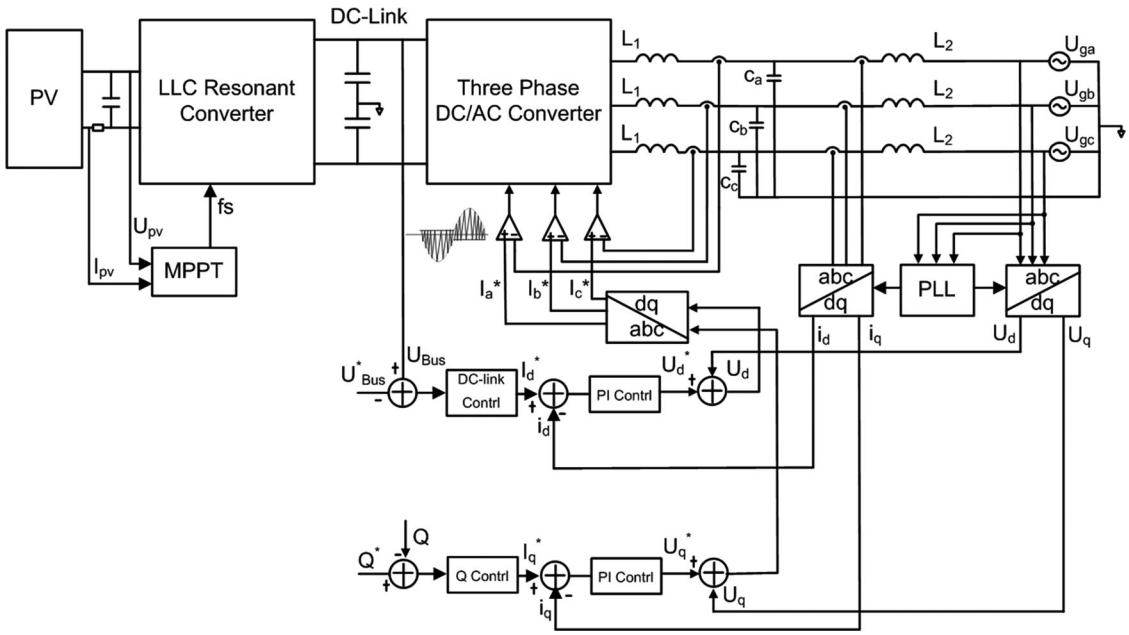

Fig. 3. Overall control diagram of a two-stage three-phase grid-tie inverter system.

($U_{\rm pv}$) and current ($I_{\rm pv}$) of the PV panel are both sensed continuously to calculate the instantaneous power. The MPPT algorithm is based on the variation of the instantaneous power of PV panel that changes the switching frequency of the *LLC* resonant dc–dc converter to track the maximum power output. In order to keep power balanced between the generator (PV panel) and the grid for two-stage microinverter system, a bus voltage regulator is used to keep the voltage constant. The bus voltage is regulated by controlling the amount of current injected into the grid. For example, if the irradiance is increasing, the bus voltage increases because the dc–dc stage is running with MPPT. When $U_{\rm Bus}$ is greater than $U^*_{\rm Bus}$, the output value of the dc link regulator (I^*_d) increases and the inverter stage injects more current into the grid. Conversely, if the irradiance is decreasing, the inverter stage reduces the amount of current injected into the grid. Low THD is achieved by sensing the injected grid current via *d/q* transformation and causing it to follow the reference current I^*_d. If the power factor is assumed to be unity, the reactive current will be zero after *d/q* transformation (no phase shift). As described in [22], the bidirectional current through the inverter-side inductor (L_1) is also sensed as a part of the internal current loop to achieve ZVS and improve the dynamic response of the inverter stage. Beside the discussed conditions, there is another condition in practical environments. For example, if the irradiance under extremely severe shadow conditions is so weak that the PV panel has not enough energy to make the microinverter connect the grid. Burst mode control [42], [43], a well-known solution used for very light load condition, will be involved in the first stage to keep bus voltage constant. Although the voltage unbalance of the split capacitors is a well-known problem for

three-phase four-wire topology; the split capacitor voltages can be actively balanced by the proposed solutions which have been presented in [44]–[48] over the last one decade is beyond the scope of this paper.

III. Modeling of Three-Phase Four-Wire Inverter

A. Average Model of Three-Phase Four-Wire Inverter With LCL Filter

The schematic of a three-phase four-wire voltage source inverter (VSI) connected to the grid through an *LCL* filter is shown in Fig. 4. The series resistances of the inductors (L_1 and L_2) have been neglected in order to simplify the derivation of average model. An average model of three-phase four-wire inverter may be obtained by neglecting the high-frequency components of both the dc voltage and the ac phase currents. According to Kirchhoff's current and voltage laws, differential equations to illustrate current and voltage as shown in Fig. 4 can be expressed by

$$\dot{I}_1 = -\frac{R_d}{L_1}I_1 + \frac{R_d}{L_1}I_2 - \frac{1}{L_1}U_{\rm cf} + \frac{U_{\rm bus}}{L_1}D - \frac{U_{\rm bus}}{2\cdot L_1}\Gamma \quad (1)$$

$$\dot{I}_2 = \frac{R_d}{L_2}I_1 - \frac{R_d}{L_2}I_2 + \frac{1}{L_2}U_{\rm cf} - \frac{1}{L_2}U_g \quad (2)$$

$$\dot{U}_{cf} = \frac{1}{C_f}I_1 - \frac{1}{C_f}I_2 \quad (3)$$

$$\dot{U}_{\rm Bus} = \frac{i_{\rm bus} - i_{\rm dc}}{\frac{C_1}{2}} = \frac{2}{C_1}i_{\rm bus} - \frac{2}{C_1}D^T I_1 \quad (4)$$

where $\mathrm{I}_1 = [i_{1a}\ i_{1b}\ i_{1c}]^T$ $I_2 = [i_{2a}\ i_{2b}\ i_{2c}]^T$ $U_{cf} = [U_{ca}\ U_{cb}\ U_{cc}]^T$ $U_g = [U_{ga}\ U_{gb}\ U_{gc}]^T$ $D = [d_a\ d_b\ d_c]$ $\Gamma = [111]^T$.

In the steady state, the grid phase currents i_{2a}, i_{2b}, and i_{2c} are controlled to be sinusoidal and in phase with the corresponding grid phase voltages U_{ga},U_{gb} and U_{gc} which can be expressed as

$$\begin{bmatrix} U_{ga} \\ U_{gb} \\ U_{gc} \end{bmatrix} = \begin{bmatrix} U_m\cos(\omega \mathrm{t}) \\ U_m\cos\left(\omega \mathrm{t} - \frac{2\pi}{3}\right) \\ U_m\cos\left(\omega \mathrm{t} + \frac{2\pi}{3}\right) \end{bmatrix} \quad (5)$$

where U_m and ω are the amplitude of the phase voltage and angular frequency of the power source, respectively. The model in the stationary coordinates can be transformed into a synchronous reference (*dq*) frame by the transformation matrix *T* (Park's transformation) as follows:

$$T = \frac{2}{3}\begin{bmatrix} \cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ -\sin(\omega t) & -\sin(\omega t - \frac{2\pi}{3}) & -\sin(\omega t + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}. \quad (6)$$

After transformation into the synchronous three-phase reference frame, the equations of the whole averaged model are expressed by (7)–(9) [36]

$$\dot{I}_{1dq} = -WI_{1dq} - \frac{R_d}{L_1}I_{1dq} + \frac{R_d}{L_1}I_{2dq} - \frac{1}{L_1}U_{cfdq} + \frac{1}{L_1}U_{dq} \quad (7)$$

$$\dot{I}_{2dq} = \frac{R_d}{L_2}I_{1dq} - WI_{2dq} - \frac{R_d}{L_2}I_{2dq} + \frac{1}{L_1}U_{cfdq} - \frac{1}{L_2}U_{gdq} \quad (8)$$

$$\dot{U}_{cfdq} = \omega U_{cfdq} + \frac{1}{C_f}(i_{1dq} - i_{2dq}) \quad (9)$$

where $W = \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix}$, $U_{dq} = U_{\rm Bus}D_{dq}$.

B. Small-Signal Model

The small-signal model can be obtained by using perturbation to the average model around the dc operating point, as shown in (10), *X* and $\hat{x}$ denote the dc operating point and the small signal perturbation, respectively,

$$x = X + \hat{x}. \quad (10)$$

From (7) to (9), combining with the small signal perturbation (10), the mathematical model can be represented by a small signal mode of the form in linear time invariant state space

$$\begin{cases} \dot{\mathrm{X}}(\mathrm{t}) = A\cdot X(\mathrm{t}) + B\cdot U(\mathrm{t}) + F\cdot\delta(\mathrm{t}) \\ Y(\mathrm{t}) = C\cdot X(\mathrm{t}) + D\cdot U(\mathrm{t}) \end{cases} \quad (11)$$

where

$$X = \begin{bmatrix} \hat{I}_{1d} & \hat{I}_{1q} & \hat{I}_{2d} & \hat{I}_{2q} & \hat{U}_{cfd} & \hat{U}_{cfq} \end{bmatrix}^T$$

$$U = [\hat{u}_{dg} \quad \hat{u}_{dq}]^T \quad d = [\hat{u}_{gd} \quad \hat{u}_{gq}]^T.$$

X is the normalized state vector selected as $\hat{I}_{1d}\ \hat{I}_{1q}\ \hat{I}_{2d}\ \hat{I}_{2q}\ \hat{U}_{cfd}\ \hat{U}_{cfq}$, *U* is the normalized inverter output voltage, δ is the normalized grid voltage, and Y is the normalized injected grid current in the *dq* reference frame. *A*, *B*, *C*, *D*, and *F* are matrices with appropriate dimensions as given

$$A = \begin{bmatrix} -\frac{R_D}{L_1} & \omega & \frac{R_D}{L_1} & 0 & -\frac{1}{L_1} & 0 \\ -\omega & -\frac{R_D}{L_1} & 0 & \frac{R_D}{L_1} & 0 & -\frac{1}{L_1} \\ \frac{R_D}{L_2} & 0 & -\frac{R_D}{L_2} & \omega & \frac{1}{L_2} & 0 \\ 0 & \frac{R_D}{L_2} & -\omega & -\frac{R_D}{L_2} & 0 & \frac{1}{L_2} \\ \frac{1}{C_f} & 0 & -\frac{1}{C_f} & 0 & 0 & -\omega \\ 0 & \frac{1}{C_f} & 0 & -\frac{1}{C_f} & -\omega & 0 \end{bmatrix}$$

$$F = \begin{bmatrix} 0 & 0 & -\frac{1}{L_2} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} & 0 & 0 \end{bmatrix}^{\mathrm{T}}$$

$$\mathrm{B} = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{L_1} & 0 & 0 & 0 & 0 \end{bmatrix}^{\mathrm{T}}$$

$$C = \begin{bmatrix} 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \end{bmatrix}^{\mathrm{T}} \qquad D = 0.$$

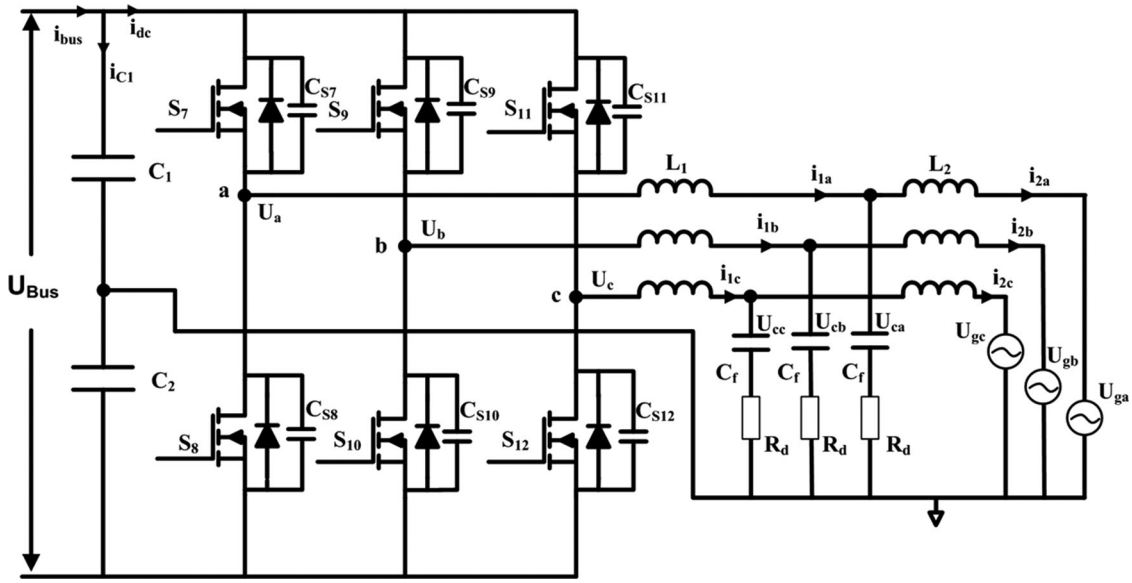

Fig. 4. Three-phase four-wire dc/ac grid-connected converter.

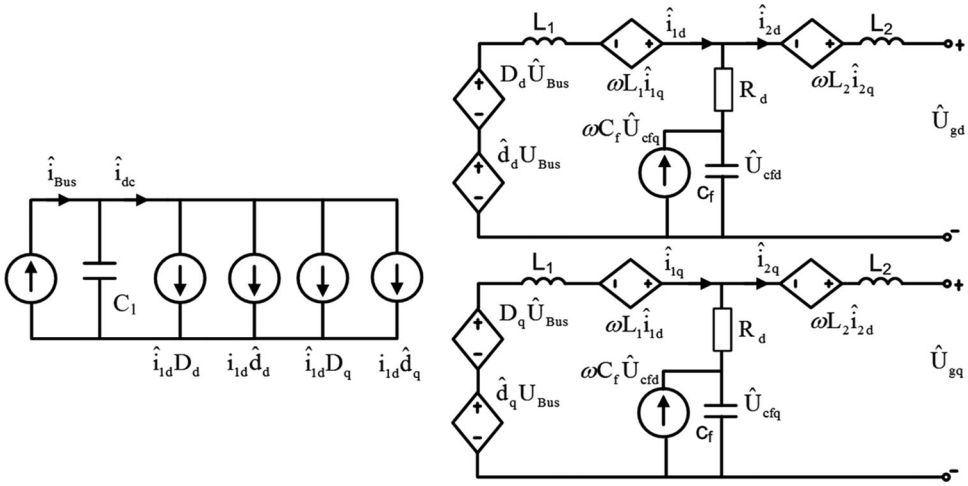

Fig. 5. Equivalent circuit based on small signal modeling.

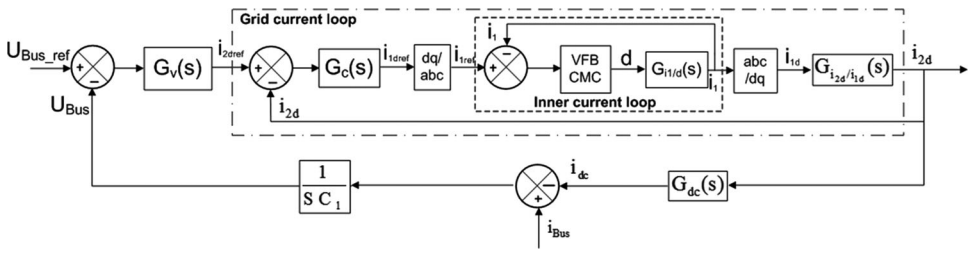

Fig. 6. Diagram of triple-loop control in *d*-axis.

Following the above procedure, the small signal equivalent circuit of the three-phase four-wire inverter with *LCL* filter is shown in Fig. 5.

IV. Triple-Loop Control Design of Inverter Stage

According to the overall control diagram as shown in Fig. 3, a MPPT CPI (center point iteration) algorithm is employed in the first stage, a more detailed description referring to this paper [37]. Step-by-step triple-loop controller design for the

inverter stage is presented in this section followed by small signal modeling of the power stage. Due to the unity power factor requirement for injected grid current, a control block diagram of the multiloop controller in the *d*-axis as shown in Fig. 6 will be presented. It can be seen that the inverter-side inductor current is controlled by the VFBCMC in the inner current loop which improves dynamic response in the whole system. Followed by the inner current loop, grid current i_{2d} is also sensed to track the reference $i_{2\mathrm{dref}}$ by the PI controller $G_c(s)$. The detailed controller design of $G_c(s)$ will be described below. Because the first stage is used for tracking the maximum power of the PV panel, a bus voltage controller $G_v(s)$ of the outer control loop is employed in the inverter stage to keep the bus voltage constant.

A. Inner Current Loop Control of the Inverter-Side Inductor

1) Implementation of the VFBCMC: ZVS in the inverter stage is achieved through bidirectional control of the inductor current in every switching cycle, as shown in Qian's paper [22]. Thus, VFBCMC is proposed to control the inductor L_1 current of the inverter side, and the current envelope of L_1 is followed with upper limit and lower limit as shown in Fig. 7.

It can be seen from Fig. 7, turn-on time is defined as the time required to keep the upper switch ON and make the inductor current traverse from the lower limit to the upper limit. The lower limit and the upper limit are determined by (12) and (13) according to the polarity of grid voltage. Turn-on time (t_{on}) is calculated according to (14). Turn-off time is defined as the required time which lower switch should stay ON to make the inductor current traverse from the upper limit ($i_{1\mathrm{ref}}$) to the lower limit. The off time (t_{off}) is calculated according to (15). The switching frequency is derived using the t_{on} and t_{off} expressions according to (16)

$$\begin{cases} i_{1\mathrm{ref}} = 2\sqrt{2} * I_m * \sin(\omega t) + B_0; & \text{if } \sin(\omega t) > 0 \\ i_{\mathrm{lower}} = -B_0 \end{cases} \tag{12}$$

$$\begin{cases} i_{1\mathrm{ref}} = B_0; & \text{if } \sin(\omega t) < 0 \\ i_{\mathrm{lower}} = 2\sqrt{2}^{*} I_m^{*} \sin(\omega t) - B_0 \end{cases} \tag{13}$$

$$t_{\mathrm{on}} = L_1 \frac{i_{1\mathrm{ref}} - i_{\mathrm{lower}}}{\frac{1}{2}U_{\mathrm{Bus}} - U_m} \tag{14}$$

$$t_{\mathrm{off}} = L_1 \frac{i_{1\mathrm{ref}} - i_{\mathrm{lower}}}{\frac{1}{2}U_{\mathrm{Bus}} + U_m} \tag{15}$$

$$f_s = \frac{(\frac{U_{\mathrm{Bus}}}{2})^2 - U_m^2}{L_1 \cdot U_{\mathrm{Bus}} \cdot (i_{1\mathrm{ref}} - i_{\mathrm{lower}})}. \tag{16}$$

2) Small Signal Modeling of the VFBCMC for One Phase of the Half-Bridge Inverter: From (16), switching frequency is variable at a line frequency with the variation of i_{upper} i_{lower} U_m. Because the duty cycle is nonlinear to control the inductor current in the variable switching frequency converter, there have been some limitations in the application of state space averaging techniques. In order to design the current loop of the inverter-side inductor, referring to papers [30]–[34], the development of the small signal model of VFBCMC for a half-bridge inverter and the derivation of the transfer function are presented in this section.

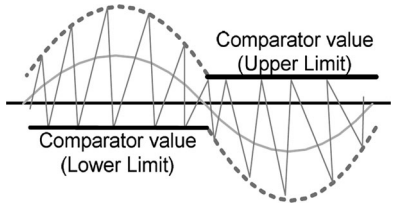

Fig. 7. VFBCM of L_1.

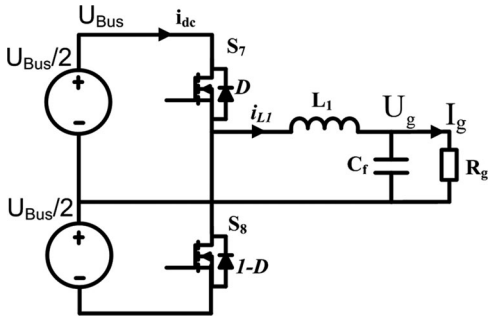

Fig. 8. Half-bridge topology of one inverter phase.

a) Small signal of power stage in a half-bridge inverter: The half-bridge inverter is modeled with an averaged circuit model [30], [31], which uses the PWM switch model. Since the neutral wire of three-phase four-wire inverter is present as shown in Fig. 2, each phase of the inverter is considered to be identical. One phase (as shown in Fig. 8) of the three-phase four-wire topology is discussed in this segment. The following assumptions have been made in order to simplify analysis: 1) the parasitic resistance of L_1 and C_f is neglected, 2) the effect in the grid-side inductor L_2 will not be considered, 3) the impedance of the grid is replaced by an ideal resistance R_g, 4) the dc-link capacitance is large enough to regard U_{Bus} as an ideal voltage source, 5) MOSFETs are assumed to be ideal switches.

The relationship among the input voltage (U_{bus}), output voltage U_g, and the switch duty cycle *D* can be derived according to Fig. 8, since in steady state the time integral of the inductor voltage over one time period T_{s} must be zero

$$\left[\frac{1}{2}U_{\mathrm{Bus}} - U_g\right] \cdot D \cdot T_s - \left[\frac{1}{2}U_{\mathrm{Bus}} + U_g\right] \cdot (1-D) \cdot T_s = 0. \tag{17}$$

Hence, steady-dc-voltage transfer function, defined as the ratio of the output voltage to the input voltage, is

$$U_g = U_{\mathrm{Bus}} \cdot (D - 0.5). \tag{18}$$

Assuming a lossless circuit, input power ($U_{\mathrm{Bus}} * i_{\mathrm{dc}}$) equals to output power ($U_g * i_g$) and the average current through L_1 (i_{L1}) is also equal to I_g

$$U_{\mathrm{Bus}} i_{\mathrm{dc}} = U_g i_{L1}. \tag{19}$$

Substituting (18) into (19)

$$i_{\mathrm{dc}} = (D - 0.5)\, i_{L1}. \tag{20}$$

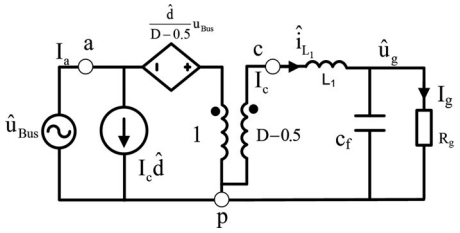

Fig. 9. Equivalent circuit based on switch model for one inverter phase.

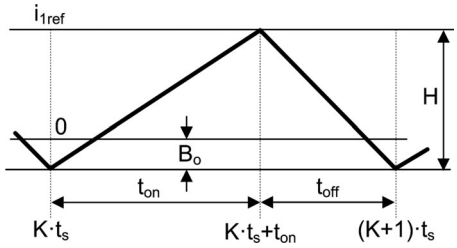

Fig. 10. Extended instantaneous inductor current waveform.

By using perturbation to the average model around the dc operating point in (18) and (20), the small signal model of the PWM switch for one-inverter phase can be obtained as (21) after neglecting second-order terms

$$\begin{cases} \hat{u}_g = \left(U_{\rm Bus}\frac{\hat{d}}{D-0.5} + \hat{u}_{\rm Bus}\right)(D-0.5) \\ \hat{i}_{\rm dc} = I_{L1}\hat{d} + \hat{i}_{L1}\,(D-0.5) \end{cases} \tag{21}$$

where $\hat{d},\ \hat{u}_{\rm Bus},\ \hat{i}_{L1}$ are the small signal variable of D, $U_{\rm Bus}$ and i_{L1}, respectively.

These two switches can be combined into one network with three terminals a, p, and c [30], [31], which stands for active, passive, and common, respectively. Using the linear equivalent circuit, the small signal model of the PWM switch for one phase of the inverter is shown in Fig. 9. Input signals of the power stage are the input voltage and duty cycle, while output signals are the inductor current and voltage.

The transfer function from duty cycle to inductor current can be expressed and further simplified as (22), while the impedance of the grid $R_{\rm g}$ is equal to zero at the ideal condition

$$\begin{aligned} G_{i_{L1}/d}(s) &= \left.\frac{\hat{i}_{L1}(s)}{\hat{d}(s)}\right|_{\substack{\hat{u}_g(s)=0 \\ \hat{u}_{\rm bus}(s)=0}} \\ &= \frac{u_{\rm Bus}}{R_g}\frac{1+sR_gC}{s^2L_1C+s\frac{L_1}{R_g}+1} \approx \frac{u_{\rm Bus}}{sL_1}. \end{aligned} \tag{22}$$

b) Small signal of VFBCMC: Fig. 10 shows the bidirectional inductor current waveform during a switching cycle. H is the difference between the upper trip point ($i_{1\rm ref}$) and lower trip point ($-{\rm B}_0$) of the PWM generator. A linearization of on-time ($t_{\rm on}$) and switching period t_s is introduced to replace duty-ratio d as input variables.

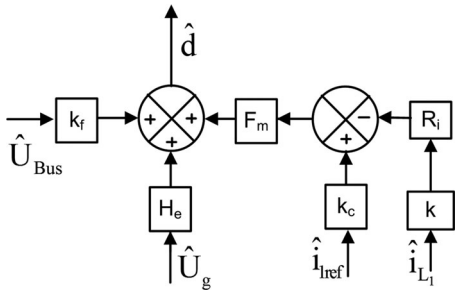

Fig. 11. Small signal model diagram of the VFBCMC.

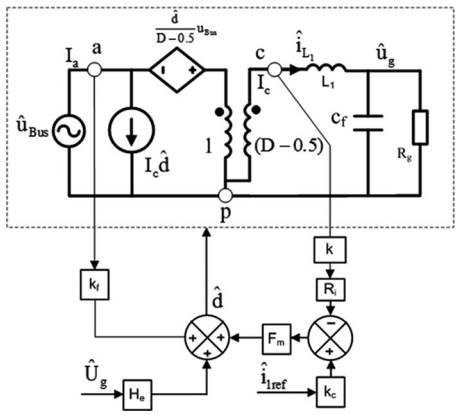

Fig. 12. Inner current loop diagram of one-inverter phase with VFBCMC.

The off-time constraint is determined as follows according to Fig. 10:

$$t_s = t_{\rm on} + t_{\rm off} = t_{\rm on} + L_1\frac{H}{u_g + \frac{1}{2}u_{\rm Bus}}. \tag{23}$$

With (23) small signal perturbed, a small signal modeling of VFBCMC is given by (24). The detailed derivation is shown in the appendix

$$\begin{aligned} \hat{d} = &\frac{2L_1}{u_{\rm Bus}T_sR_i}\left(\hat{i}_{1\rm ref} - 2R_i\hat{i}_{L1}\right) + \left[\frac{D(1-D)}{\left(\frac{1}{2}u_{\rm Bus}+u_g\right)} - \frac{D}{2u_{\rm Bus}}\right] \\ &\times \hat{u}_{\rm Bus} + \left[\frac{2D(1-D)}{\left(\frac{1}{2}u_{\rm Bus}+u_g\right)} + \frac{D}{2u_{\rm Bus}}\right]\hat{u}_g \end{aligned} \tag{24}$$

where

$$F_m = \frac{2L_1}{u_{\rm Bus}T_sR_i};\ k = 2;\ k_c = 1\cdot$$

In order to reduce the power consumption of the current sensing, a current transformer with the turn's ratio of 1:100 is used to replace conventional resistance sensing in the inverter-side inductor. Based on the experimental prototype, the current sensing coefficient (R_i) is selected as 0.6. According to (24), a small signal model of one-phase inverter with VFBCMC is shown in Fig. 11.

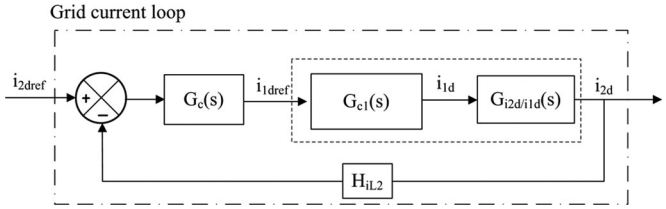

Fig. 13. Grid current control diagram in *d*-axis.

From (24) and Fig. 11, parameters of each block can be derived as follows:

$$k_f = \frac{\hat{d}}{\hat{u}_{\mathrm{Bus}}} = \frac{D\left(1-D\right)}{\left(\frac{1}{2}u_{\mathrm{Bus}}+u_g\right)} - \frac{D}{2u_{\mathrm{Bus}}} \tag{25}$$

$$H_e = \frac{\hat{d}}{\hat{u}_g} = \frac{2D\left(1-D\right)}{\left(\frac{1}{2}u_{\mathrm{Bus}}+u_g\right)} + \frac{D}{2u_{\mathrm{Bus}}} \tag{26}$$

$$\frac{\hat{d}}{\hat{i}_{1\mathrm{ref}}} = \frac{2L_1}{u_{\mathrm{Bus}}T_s R_i k_c} \tag{27}$$

$$\frac{\hat{d}}{\hat{i}_{L1}} = \frac{4L_1}{u_{\mathrm{Bus}}T_s}. \tag{28}$$

c) Complete Model With VFBCMC for One-Inverter Phase: By combining the small signal model of the control loop and the equivalent circuit of the power stage based on the previously derived PWM switch model, a complete model of the inner loop control with VFBCMC for one-inverter phase can be derived as shown in Fig. 12.

From Fig. 12, the complete model of the inner current loop has three input signals and an output signal. Generally speaking, the purpose of the current loop is to make the inductor current follow the control signal. Without the consideration of the disturbances of U_{bus}(s) and U_g(s), according to (22) and Fig. 12, the inner current loop dc gain of the transfer function G_{c1}(s) from $i_{1\mathrm{ref}}$ to i_{L1} is

$$G_{c1}\left(s\right) = \frac{i_{L1}\left(s\right)}{i_{1\mathrm{ref}}\left(s\right)} = F_m k_c G_{i_{L1}/d}\left(s\right). \tag{29}$$

B. Controller Design of the Grid Current Loop

In order to achieve high loop gain at the harmonic frequency and improve the stability of the system, a second current control loop is implemented by sensing the injected grid current. If I_q^* is set to zero in the system control diagram of Fig. 3, unity power factor can be obtained at the grid side. The grid current controller design in the *d* axis is discussed in this section. Because the inner current control loop can be regarded as a real-time control system, the response of the inner current loop is much faster than that of the grid current loop. The VFBCMC of the inner loop is replaced by G_{c1}(s) as shown in Fig. 13.

Ignoring grid disturbances and referring to the equivalent circuit in Fig. 5, the transfer function $\hat{i}_{2d}\left(s\right)/\hat{i}_{1d}\left(s\right)$ from the reference of the inductor (L_1) current to the grid-side current in *d* axis can be expressed by

$$G_{\frac{i_{2d}}{i_{1d}}}\left(s\right) = \frac{\hat{i}_{2d}\left(s\right)}{\hat{i}_{1d}\left(s\right)} = \frac{sR_dC_f+1}{s^2L_2C_f+sR_dC_f+1}. \tag{30}$$

TABLE I
KEY PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Three-Phase Four-Wire DC–AC Converter	
Output voltage	120 V_{ac}
Output frequency	60 Hz
Rated output power	400 W
Bus voltage (U_{Bus})	400 V
Bus capacitor (C_1 and C_2)	B32776G4406K (40 μF EPCOS)
Secondary switch S_7–S_{12}	FCB20N60TM
Inductor L_1	270 μH
Grid interface inductor L_2	600 μH
Output capacitor C_f (B32923 X2 MKP)	1 μF (R_d = 10 mΩ)
Switching frequency f_s	20–180 kHz
Grid current sensing coefficient H_{iL2}	1.2

Fig. 14 shows the bode plot of the product of G_{c1}(s) and $G_{i2d/i1d}$(s) in the grid current control loop according to parameters in Table I. A PI controller is designed to increase the low frequency gain and reduce the steady-state error between the desired and the actual injected grid current. The transfer function of the PI controller is given by

$$G_c\left(s\right) = k_p + \frac{k_i}{s} = \frac{k_p s + k_i}{s}. \tag{31}$$

The loop gain L of the grid current loop is

$$T_{oL2} = G_c\left(s\right)\cdot G_{c1}\left(s\right)\cdot G_{\frac{i_{2d}}{i_{1d}}}\left(s\right)H_{iL2}\left(s\right). \tag{32}$$

Substitution of (29), (30), and (31) into (32) leads to

$$T_{oL2} = k_{kc}\frac{a_2s^2+a_1s+a_0}{b_4s^4+b_3s^3+b_2s^2+b_1s+b_0} \tag{33}$$

where

$$k_{kc} = H_{iL2};\ b_4 = L_2C_fT_sR_i; b_3 = C_fT_sR_iR_d;\ b_2 = T_sR_i;$$
$$b_1 = b_0 = 0$$
$$a_2 = k_pC_fR_d;\ a_1 = k_p + k_iC_fR_d;\ a_0 = k_i.$$

The controller G_c(s) is designed to make the overall system satisfy the following requirements: 1) zero-steady-state error, 2) more than 45° phase margin, 3) greater than 2-kHz system bandwidth. The bode plot of the compensated grid current control loop that meets the design requirements is shown in Fig. 15. The PI controller parameters are designed to obtain a PM of 58° at the gain crossover frequency of 3 kHz. To achieve the required frequency response, the parameter k_i/k_p is selected as 714 ($k_p = 14$), respectively. As shown in Fig. 15, low frequency gain is significantly improved and the gain margin (GM) is 12 dB.

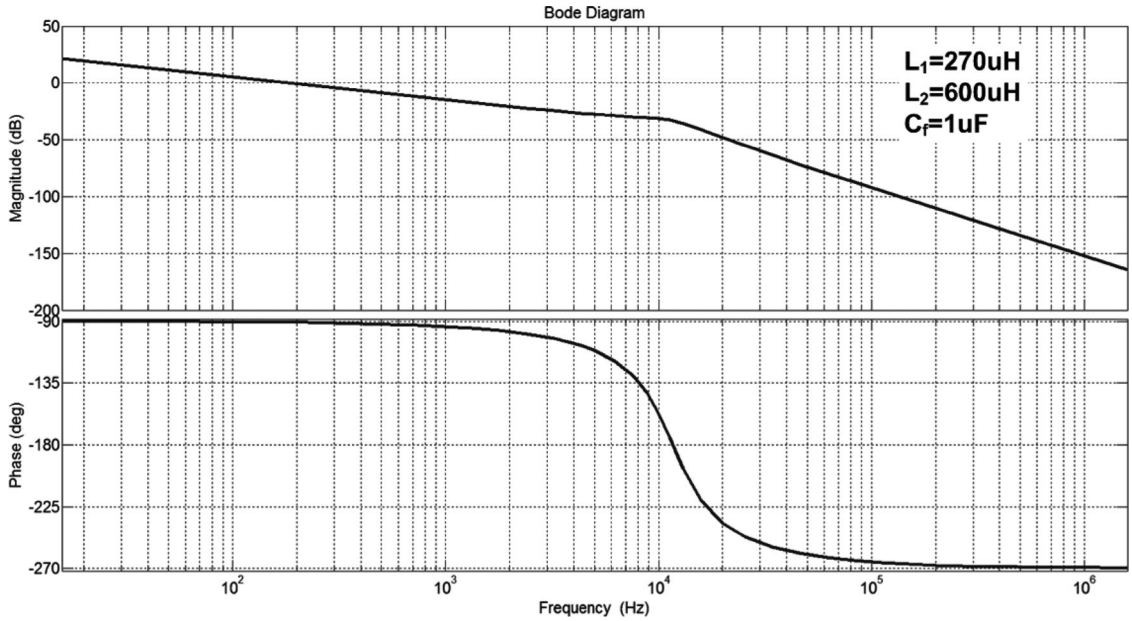

Fig. 14. Bode plot of current control loop without controller.

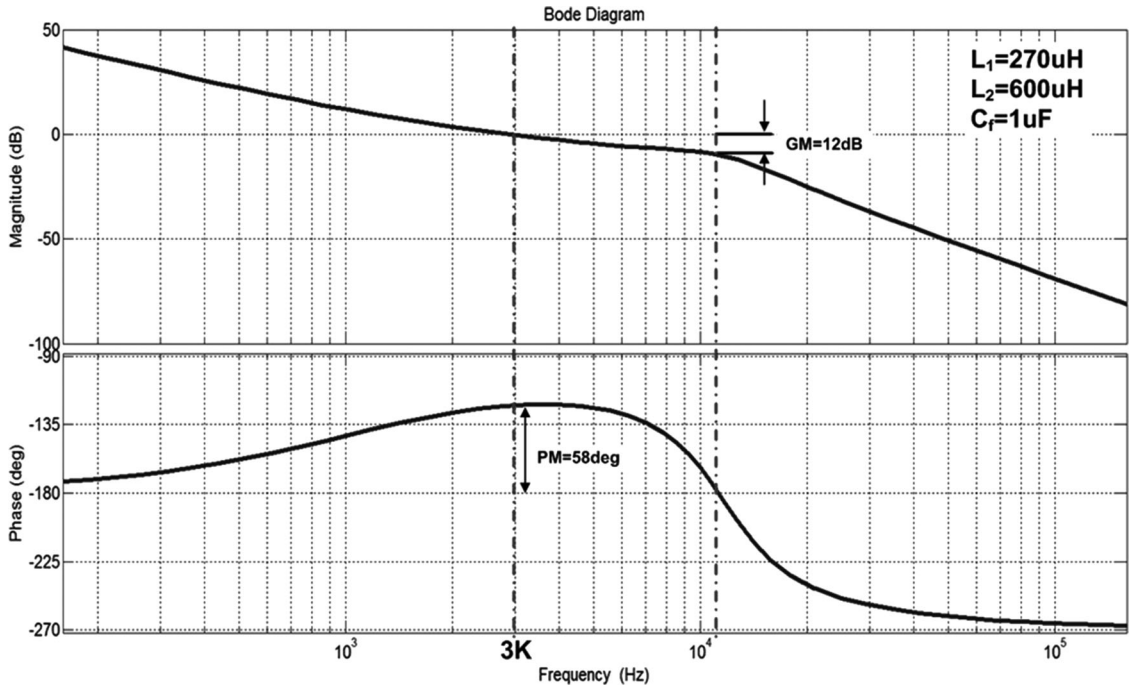

Fig. 15. Bode plot of current control loop with PI controller: $\mathrm{PM} = 58^{\circ}$ at $f_c = 3\,\mathrm{kHz}$.

C. Controller Design of the Bus Voltage Loop

The outer voltage control loop regulates the bus voltage at the reference value by changing the injected grid current according to the overall control block diagram as shown in Fig. 6. Two current control loops are assumed as a part of the control object in the voltage control loop. The control diagram of the dc link voltage is redrawn in Fig. 16 showing the inner current control

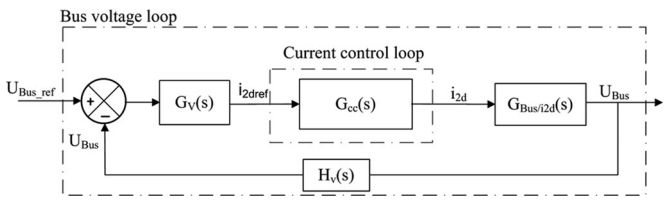

Fig. 16. Outer bus voltage control loop diagram.

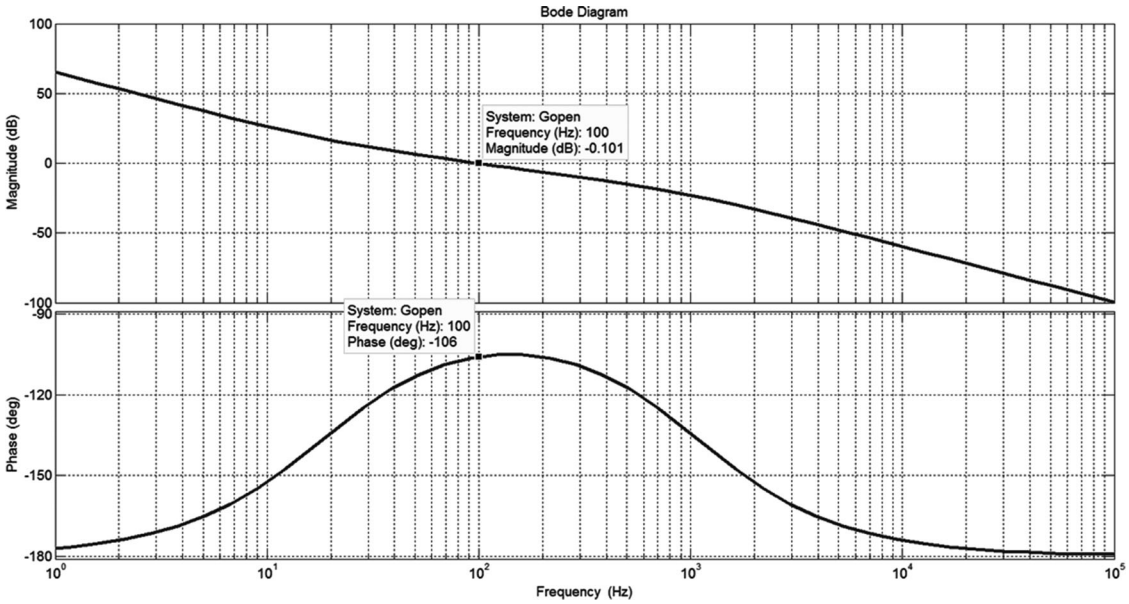

Fig. 17. Bode plot of outer bus voltage loop with PI compensation: $\mathrm{PM} = 74^{\circ}$ at $f_c = 100\,\mathrm{Hz}$.

loop and outer bus voltage control loop with the *d*-axis current loop inside the dashed block.

As shown in Fig. 6, the grid voltage $\mathrm{U_g}$ and the output current of the first-stage dc/dc converter i_{Bus} are regarded as the disturbances to the inner current loop and the outer dc-link voltage control loop, respectively. In most cases, the PV MPPT algorithm is relatively slow and grid voltage disturbances are small. As a result, these disturbances can be neglected to a certain extent. Consequently, the transfer function from the injected grid current $\mathrm{i_{2d}}$ to dc link voltage can be derived as $G_{\mathrm{Bus}}/i2\mathrm{d(s)}$ as shown in Fig. 16. Usually, the bandwidth of the outer voltage loop should be lower than the current loop in order to ensure the stability of the system. These two loop controllers are designed independently and their interaction can be neglected. The outer voltage control loop regulates the output voltage at the reference value by setting the inductor current reference. According to Fig. 16, the open loop transfer function of the bus voltage loop is expressed by (34). The bode plot of the voltage control loop gain is shown in Fig. 17. The PI controller parameters are calculated to achieve a PM of 74° at the gain crossover frequency of 100 Hz. The parameter $k_{\mathrm{iv}}/k_{\mathrm{pv}}$ is obtained as 117.4 ($k_{pv} = 8.5$)

$$G_{\mathrm{Bus\_open}}(s) = G_v(s)\, G_{cc}(s)\, H_v(s)\, G_{\frac{\mathrm{Bus}}{i_{2\mathrm{d}}}}(s) \tag{34}$$

where

$$G_{cc}(s) = \frac{1}{1 + 3 \cdot s \cdot T_{\mathrm{delay}}} = \frac{1}{1 + 10^{-4}s}[38];\; H_v(s) = \frac{1}{200}$$

$$G_v(s) = k_{pv} + \frac{k_{iv}}{s};$$

$$G_{\frac{\mathrm{Bus}}{i_{2d}}}(s) = \frac{\sqrt{3}}{4sC_1}.$$

V. Simulation and Experimental Results

A. Simulation Results

A three-phase two-stage microinverter with triple-loop compensation was simulated with MATLAB/Simulink. Fig. 18(a) shows the current waveform of inverter-side inductor L_1 and Fig. 18(b) shows the injected grid current of each phase with less than 0.5% THD.

B. Experimental Results

A three-phase four-wire microinverter prototype with both-stage ZVS was built based on the following specifications: maximum output power 400 W and output voltage $208/120\ \mathrm{V_{AC}}$. Key parameters are shown in Table I. The detailed calculation of key parameters in the proposed ZVS three-phase four-wire inverter which we presented in [40] and [41] is beyond the scope of this paper. The input voltage range of the PV panel for maximum power tracking is from 35 to 55 $\mathrm{V_{DC}}$. A three-phase four-wire voltage source inverter is employed in the second stage that connects the dc bus to the grid through an inductance of 600 μH. The nominal dc-bus voltage is 400 V and the grid voltage rms value is 120 V L-N.

The inverter-side inductor current waveform and injected grid current at rated output power in the three-phase inverter are shown in Fig. 19. Although the inverter-side inductor current has a high ripple, the THD of the injected grid current is less than 2.5%, and meets the IEEE 1547 standards [39]. In addition, Fig. 20 shows the experimental waveforms of the injected grid current at different power level with 20% and 50% of rated output power. According to the theoretic analysis and simulation, low THD of the injected grid current still can be achieved even at small output power. From Fig. 20, the injected grid current THD has a little bit higher than full rated output power. The reason is that the relative error of the measurement of the current

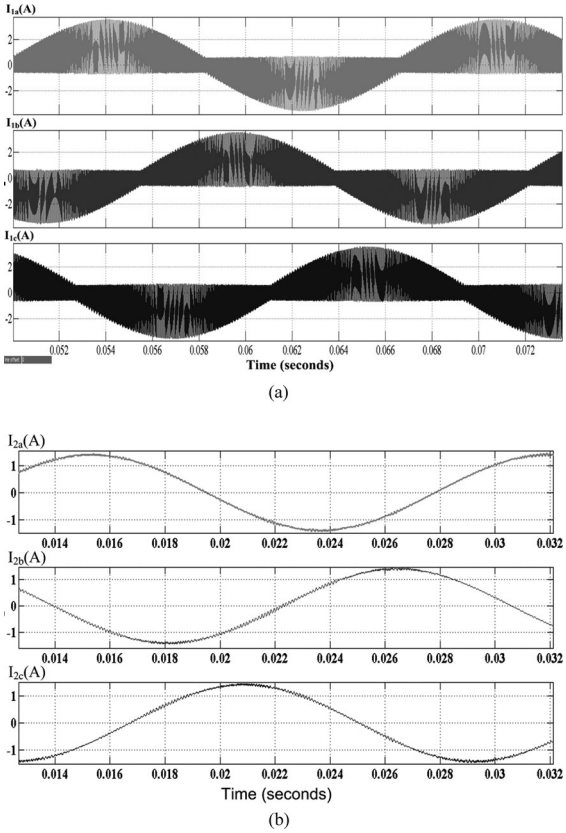

Fig. 18. Inductor current waveform and injected grid current in the inverter stage. (a) Each phase inductor current. (b) Three-phase injected grid current.

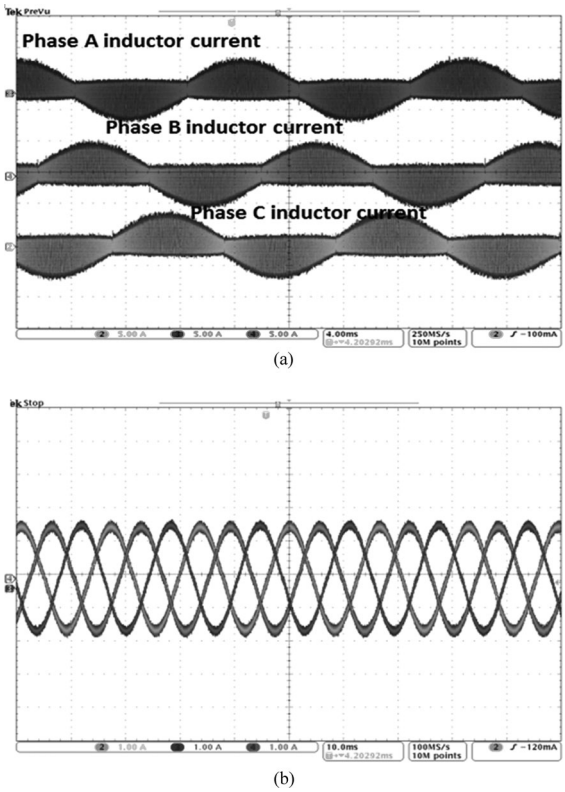

Fig. 19. Inductor current waveform and injected grid current in the inverter stage. (a) Each phase inverter-side inductor current. (b) Three-phase injected grid current.

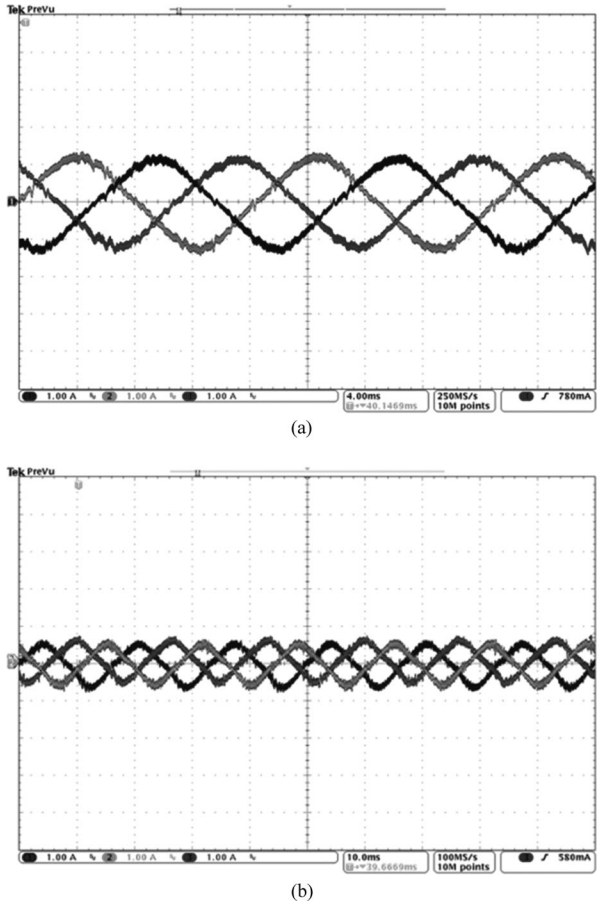

Fig. 20. Injected grid current with different power levels. (a) Three-phase injected inductor current (50% rated output power). (b) Three-phase injected inductor current (20% rated output power).

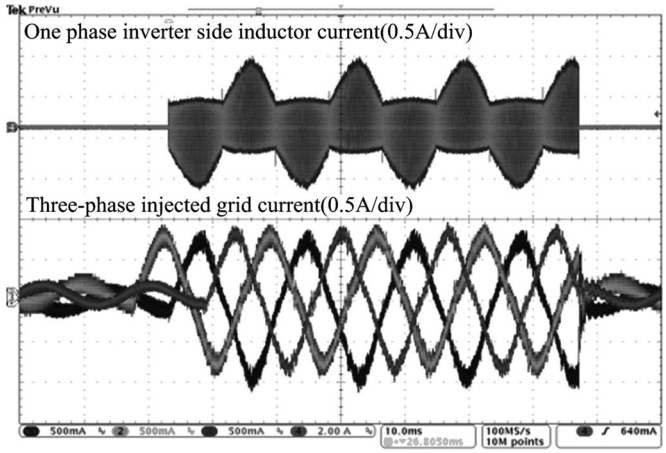

Fig. 21. Shows the load dynamic response of the inverter to a step change 0% to 50% rated output power.

sensor is high at light output power. The injected grid current THD will be reduced with the current sensing improvement.

The inverter output dynamics with a step change of the current reference from 0% to 50% rated output power and from half to full rated output power are separately shown in Figs. 21 and 22. It can be seen from Figs. 21 and 22, the injected grid

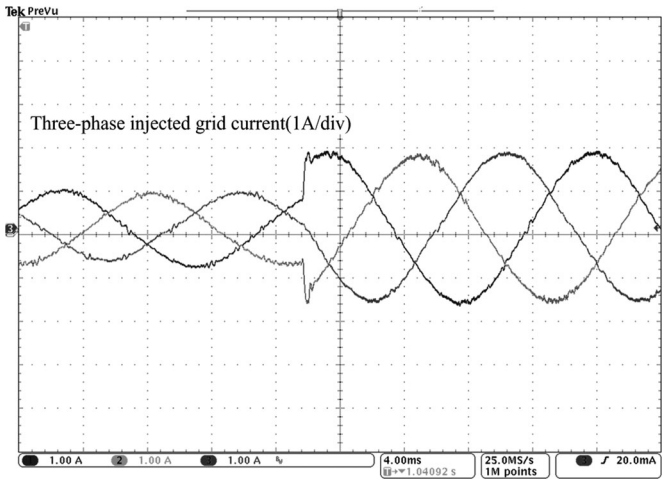

Fig. 22. Shows the load dynamic response of the inverter to a step change 50% to 100% rated output power.

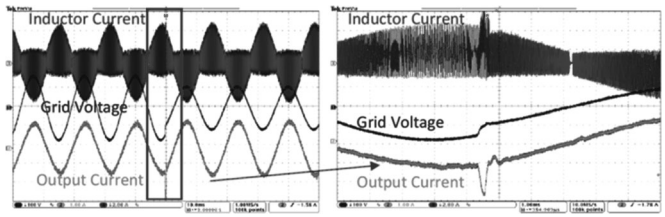

Fig. 23. Dynamic response to a step change in the grid voltage from 120 to 80 V.

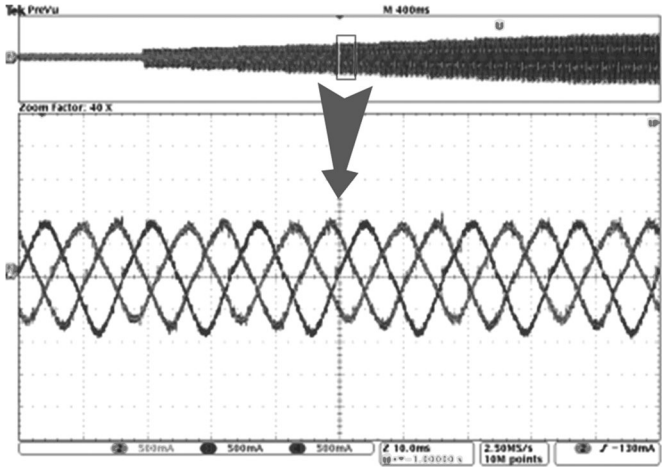

Fig. 24. Soft start function of the three-phase four-wire grid-connected inverter (0.5 A/div).

current tracks quickly the current reference due to the action of VFBCM control in the inner current loop. In addition, the dynamic response of the inverter to a step change in the grid voltage from 120 to 80 $V_{\rm rms}$ is shown in Fig. 23. In order to observe the performance of the soft start function, the measured waveform of the injected grid current increased gradually is shown in Fig. 24.

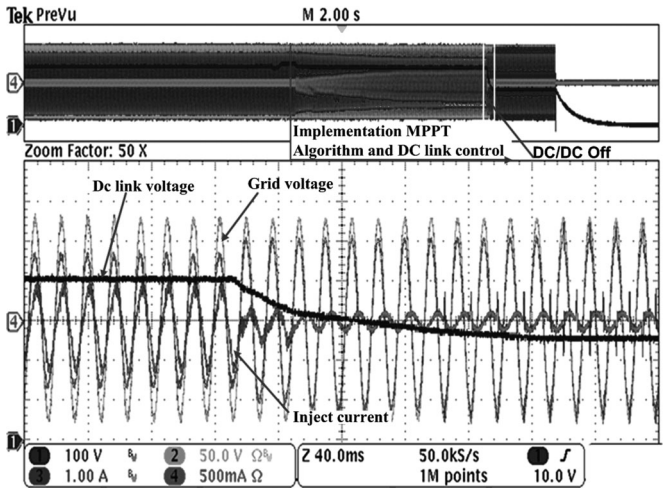

Fig. 25. Experimental waveform of overall system with grid connected.

Fig. 25 shows the experimental waveform of overall system when connected to the grid. The dc-link regulator is employed to keep the bus voltage constant while the CPI MPPT algorithm is active. As shown in Fig. 25, the injected current (green channel) to the grid is gradually increasing with the MPPT which is tracking the maximum power of the PV panel.

VI. Conclusion

A small signal model of the inner loop control with VFBCMC is presented. The fast dynamic response of the three-phase four-wire grid-connected inverter is achieved due to VFBCM control. In order to use the PI regulator of the grid current control in the second loop, a small signal equivalent circuit of three-phase four-wire inverter in the rotating synchronized frame is derived based on average signal model. Once the design of the two inner current control loops was completed, design of the dc link controller was addressed for two-stage microinverter applications. Lastly, the modeling and triple-loop controller design from the inner current loop to outer bus voltage loop are verified by experimental results based on a 400 W two-stage microinverter prototype.

Appendix
Derivation Procedure for the Small Signal Model of the VFBCMC

The relationship between the duty cycle, on time, and switching period is represented by (A1) based on the perturbed and linearized small signal model [32]–[34]

$$\begin{cases} \hat{d} = \frac{\hat{t}_{\rm on} - D \cdot \hat{t}_s}{T_s} \\ \hat{t}_s = \hat{t}_{\rm on} + \hat{t}_{\rm off} \end{cases} \tag{A1}$$

and

$$\hat{t}_{\rm off} = \frac{2L_1}{u_g + \frac{1}{2}u_{\rm Bus}}\hat{i}_{L1} - \frac{2L_1 \cdot i_{L1}}{\left(u_g + \frac{1}{2}u_{\rm Bus}\right)^2}\left(\hat{u}_g + \frac{1}{2}\hat{u}_{\rm Bus}\right)\hat{V}_o. \tag{A2}$$

Substituting (A2) into (A1) and simplifying, we get

$$\hat{d} = \frac{\hat{t}_{\rm on}(1-D)}{T_s} - \frac{2DL_1}{(u_g + \frac{1}{2}u_{\rm Bus})T_s}\hat{i}_{L1} + \frac{2DL_1 i_{L1}}{(u_g + \frac{1}{2}u_{\rm Bus})^2 T_s}\hat{u}_g + \frac{DL_1 i_{L1}}{(u_g + \frac{1}{2}u_{\rm Bus})^2 T_s}\hat{u}_{\rm Bus}. \quad \text{(A3)}$$

From on-time constraints, the relationship between peak current and average current is derived as

$$i_p = i_{L1} + \left(\frac{1}{2}u_{\rm Bus} - u_g\right)\frac{t_{\rm on}}{2L_1}. \quad \text{(A4)}$$

In order to remove $\hat{\rm t}_{\rm on}$ in (A3), linearize (A4)

$$\hat{t}_{\rm on} = \frac{2L_1}{\frac{1}{2}U_{\rm Bus} - U_g}\left(\hat{i}_p - \hat{i}_{L1}\right) - \frac{DT_s}{\frac{1}{2}U_{\rm Bus} - U_g}\left(\frac{1}{2}\hat{U}_{\rm Bus} - \hat{U}_g\right). \quad \text{(A5)}$$

Substitution of (A5) into (A3) leads to

$$\begin{aligned}\hat{d} = {} & \frac{2(1-D)L_1}{\left(\frac{1}{2}u_{\rm Bus} - u_g\right)T_s}\hat{i}_p \\ & - \left[\frac{2(1-D)L_1}{\left(\frac{1}{2}u_{\rm Bus} - u_g\right)T_s} + \frac{2DL_1}{\left(\frac{1}{2}u_{\rm Bus} + u_g\right)T_s}\right]\hat{i}_L \\ & + \left[\frac{DL_1 i_{L_1}}{\left(u_{\rm Bus} + \frac{1}{2}u_{\rm Bus}\right)^2 T_s} - \frac{D(1-D)}{2\left(\frac{1}{2}u_{\rm Bus} - u_g\right)}\right]\hat{u}_{\rm Bus} \\ & + \left[\frac{D(1-D)}{2\left(\frac{1}{2}u_{\rm Bus} - u_g\right)} + \frac{2DL_1 i_{L_1}}{\left(u_g + \frac{1}{2}u_{\rm Bus}\right)^2 T_s}\right]\hat{u}_g \end{aligned} \quad \text{(A6)}$$

and we know the steady-state equation (A7) according to Fig. 8

$$\begin{cases} \dfrac{L_1 i_{L1}}{u_{\rm Bus}T_s} = \dfrac{\left(\frac{1}{2}u_{\rm Bus} - u_g\right)t_{\rm on}}{u_{\rm Bus}T_s} = \dfrac{(u_{\rm Bus} - Du_{\rm Bus})D}{u_{\rm Bus}} = (1-D)D \\ \left[\dfrac{1}{2}u_{\rm Bus} - u_g\right]D = \left[\dfrac{1}{2}u_{\rm Bus} + u_g\right](1-D) \\ \dfrac{(1-D)}{\frac{1}{2}u_{\rm Bus} - u_g} = \dfrac{D}{\frac{1}{2}u_{\rm Bus} + u_g} = \dfrac{D}{\frac{1}{2}u_{\rm Bus} + u_{\rm Bus}\left(D - \frac{1}{2}\right)} = \dfrac{1}{u_{\rm Bus}}. \end{cases} \quad \text{(A7)}$$

Substitution of (A7) into (A6) leads to

$$\hat{d} = \frac{2L_1}{u_{\rm Bus}T_s R_i}\left(\hat{i}_{1\rm ref} - 2R_i\hat{i}_{L1}\right) + \left[\frac{D(1-D)}{\left(\frac{1}{2}u_{\rm Bus} + u_g\right)} - \frac{D}{2u_{\rm Bus}}\right] \times \hat{u}_{\rm Bus} + \left[\frac{2D(1-D)}{\left(\frac{1}{2}u_{\rm Bus} + u_g\right)} + \frac{D}{2u_{\rm Bus}}\right]\hat{u}_g. \quad \text{(A8)}$$

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