Exponential ADE Solution Based Compact Model of Planar Injection Enhanced IGBT Dedicated to Robust Power Converter Design

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***Abstract*—The compact model of an injection enhanced insulated gate bipolar transistors based on the exponential solution of the ambipolar diffusion equation is presented in this paper. To model plasma carrier distribution, an exponential shape function is used, and in steady-state forward bias operation, the plasma carrier concentration has a distribution of catenary form with just two exponential basis functions, while in transient operation, more complex profiles can be approximated using a number of exponential basis functions with a range of decay length parameters, shorter than the steady state ones. The device model developed has been implemented in Saber circuit simulator and successfully tested against complete set of high current, high voltage experimental results.**

***Index Terms*—Ambipolar diffusion equation (ADE), circuit design, compact model, double pulse switching, IE-IGBT, modeling.**

I. Introduction

INSULATED gate bipolar transistors (IGBTs) are devices of choice in modern power converter systems targeting medium to high voltage and current applications [1]–[5]. IGBT has a significantly lower on-state voltage drop compared to the unipolar devices, due to minority carrier high level injection leading to the conductivity modulation of its drift region. However, this improvement comes at an expense of an increase turn-off time, i.e., lower switching frequencies, and higher power losses. Furthermore, it is usually difficult to select the same device design parameters that will secure the low on-state voltage and large superior safe operation area (SOA) in a basic IGBT. To address the aforementioned contradictory issues, many progenies of the conventional IGBT have been developed. Devices such as dynamic N-buffer IGBT (DB-IGBT) [6], double trench insulated IGBT (DT-IGBT) [7], or injection efficiency controlled IGBT (IEC-IGBT) [8], achieved low on-voltage and superior SOA by enhancing the anode injection of minority carriers during on-state and by weakening it during the device turn-off [6], [7]. Another basic IGBT descendant is injection enhanced IGBT (IE-IGBT) devices aiming to reduce the on-state voltage, i.e., power losses [9]. During power electronic circuit design incorporating IE-IGBTs, to optimize the trade-off between the low energy loss and the low overshoot, one would need to employ unavoidably an accurate physics based model.

During the power circuitry early design stages, it has been a practice to consider an IGBT to be a binary on–off switch, thus achieving very fast simulation of the converter operation. However, this modeling approach cannot be used to analyze some key aspects of the device and converter performance such as heat dissipation for example, very important design parameter especially during operation at high switching frequencies [11]–[13]. Obviously, this will not lead to robust equipment design, as it does not provide any information regarding switch failure mechanisms. To overcome this issue, one could develop and use the IGBT models based on full internal physics of the device. These would be typically 2-D or 3-D finite-element (FE) models developed and run in some of the commercially available simulation tools. This modeling approach will provide designers with detailed knowledge of the IGBT devices, but it requires very long simulation time, and it is numerically prohibitive if one would like to study complex circuits containing multiple power devices requiring many switching events [14].

The compact modeling approach is placed between these two extremes [15]–[33]. Compact models are lower complexity models, but yet fully physically based and very accurate models of the power devices dedicated to circuit simulation. This physical modeling approach could be based on certain mathematical simplifications of the fundamental semiconductor charge transport equations, as discussed, for example, in [15], [17], [26], [28]. In order to develop an IGBT model that will describe correctly its static and dynamic behavior, the main challenge is to incorporate into a device model conductivity modulation and nonquasistatic charge storage effects [26], [27]. The absence of an industry-accepted IGBT model and the pronounced industry-need for more accurate IGBT compact model have triggered very intensive research in this area for more than a decade. The distinct challenge in developing IGBT compact model for circuit simulation lays in the fact that model needs to satisfy some refuting requirements. It needs to provide high quantitative accuracy, short CPU time, and physical, yet easy to determine model parameters. As a result, different IGBT compact models have been developed and presented in the literature, some of those suitable for long time inverter simulations (minutes) [23]. The IGBT compact models could be classified into two groups, one that solves ambipolar diffusion equation (ADE) and one that does not, typically classified as subcircuit compact models.

Manuscript received February 14, 2014; revised April 10, 2014 and May 22, 2014; accepted March 26, 2014. Date of publication June 12, 2014; date of current version November 3, 2014. This work has been supported by the ERDF WEFO SOLCER Grant. Recommended for publication by Associate Editor A. Lindemann.

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Digital Object Identifier 10.1109/TPEL.2014.2330655

To describe IGBT's static and dynamic behavior, it is vital that the ADE solution based models incorporate conductivity modulation and nonquasistatic charge storage effects [15], [26]. When the excess carrier density overcomes the IGBT's n^- base doping level by several orders of magnitude within the carrier storage region, the assumption that the excess electron concentration and excess hole concentration are equal is valid. Then, the carrier transport is determined by the ADE. An exponential approximation based solution for this equation has been developed and, in order to model the plasma carrier distribution, set of exponential shape functions is used [26]. These shape functions are found to model the shape of the plasma correctly, without oscillations in the internal distribution [26]. There is also a well-known Fourier series ADE solution based model as described in [28]. It has been based on the research results showing that the diffusion equation could be solved by means of an electrical analogy [27] and the plasma carrier concentration has a distribution of a sum of Fourier series components in space. These models could be implemented in any general purpose simulation software having nonlinear elements and variable parameters [28].

Common feature of all subcircuit compact models is that they are not trying to solve ADE in order to reproduce measurement data or predict device characteristics. Recently, HiSIM-IGBT compact model has been developed and presented [29]–[31]. This model is based on the consistency of the potential distribution within the IGBT device by considering in great details the MOSFET surface potentials and the BJT junction potentials, as described in [29] and [31]. The model has been originally developed for Trench IGBT device. The IGBT's MOSFET part is described with a conventional model, and the main model development effort has been put into extending the BJT, since IGBT output current is managed by the bipolar transistor theory. Another IGBT model has been presented in [22] and [24]. In [22], the physics-based IGBT subcircuit model which successfully included the effects of localized lifetime control (LLC) on device electrical performance has been described. In particular, the model depicts the non punch trough IGBTs with different locations of LLC region.

Thermal compact model of an IGBT is equally important as its electrical counterpart to accurately predict circuit performance [11]–[13]. The work presented in [11] and [15] describes an electro-thermal (ET) modeling strategy that has been widely accepted by compact modeling research community and successfully applied since. It could be briefly described in what follows. Adding an extra node, thermal node, to the electrical compact model of the IGBT device an ET models can be formulated. This thermal node has information regarding junction temperature of the device and it represents a connection between the active devices and rest of the circuit thermal network [11]. The thermal parts of the compact models are represented using a thermal RC network due to an electrical analogy [12]: thermal resistance is represented by an electrical resistance, thermal capacitance by an electrical capacitance, and dissipated power by current source [32]. Either Foster or Cauer RC networks can be used for this purpose [32]. Since the Foster network is not directly suitable for the heat-flow path identification (because of the node-to-node heat capacitances), the Cauer RC network is preferred choice for thermal device characterization. Cauer network includes only node-to-ground capacitances and it represents a discretized image of the real heat-flow structure. Network elements can be determined by using a deconvolution method for extraction of the RC thermal network parameters from the thermal transient response of the device for a step function excitation. Namely, applying an abrupt dissipation step onto the chip, the time-function of the rise of the chip temperature has to be determined. Either experimental method or 3-D Finite Element Model could be employed to obtain these thermal transient responses [32].

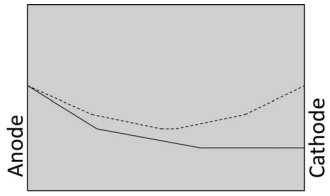

Fig. 1. Schematic of the carrier profile comparison between conventional IGBT (solid line) and IE-IGBT (dashed line).

In what follows, an exponential ADE solution based compact model for planar injection enhanced IGBT device, similar to the one described in [34], has been presented and tested against full set of high current, high voltage experimental results.

II. IE-IGBT Device Structure and Compact Model Development

Fig. 1 shows the comparison on the carrier profiles in the n-base of an IGBT and injection enhanced IGBT (IE-IGBT or sometimes denoted as IEGT) for the lower operating frequency case. In the case of the conventional IGBT, carrier concentration in the n-base region is poor, and this is due to built-in hole bypass structure in the IGBT's MOS cathode region. This can lead to a large on-state voltage in high voltage devices, typically above 3 kV. As shown in Fig. 1, the IE-IGBT has carrier profile very similar to that of GTO or a PiN diode leading to a good tradeoff between on-state voltage drop and switching losses. The IE-IGBT has been proposed in the early nineties and has been studied by many researchers [10]. The IE effect was simply defined as higher level of electron injection from n-channel to the n-base, than the one expected from the basic IGBT. This was explained as a result of the IE-IGBT's higher electron injection efficiency, and has been since confirmed theoretically and experimentally [9], [10]. The higher electron efficiency occurs in both, planar and trench structures. Technology parameters determining the injection efficiency are half of unit cell length and the ratio of the gate length and source/body region length in the planar structure and product of half unit cell length and trench depth in the trench structure.

The schematic cross section of a planar IE-IGBT considered in this study is shown in Fig. 2. In order to achieve the n-base carrier profile similar to one presented in Fig. 1, the device can be represented by a simplified electric circuit consisting of a

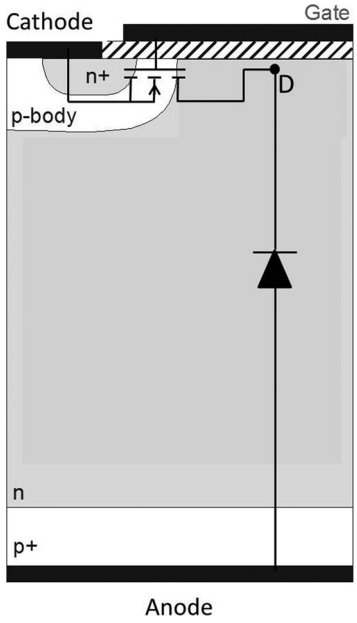

Fig. 2. Schematic of a planar IE-IGBT and simplified equivalent circuit.

MOSFET and PiN diode as shown in Fig. 2. When positive voltage is applied at the gate contact to invert the p-body and create the device's channel, the n-base area underneath the gate is in accumulation; this electron accumulation region can act as a cathode of the PiN diode shown in Fig. 2. This is used as a starting point in development of a compact IE-IGBT model as described in what follows.

A. MOSFET Section Model

The dc characteristics of the MOSFET part of the overall IE-IGBT model has been well represented with a basic SPICE type model with the addition of some effects. Significant change in output resistance due to the expansion of the drain depletion region with drain voltage can be well modeled by the channel length modulation parameter λ, found in SPICE level 1. The device transconductance reduces with increasing gate bias, and this can be adequately modelled with the use of the SPICE level 3 parameter θ controlling the effects of velocity saturation due to high electric fields.

This results in the following well-known overall expression for the MOSFET current:

$$I_D = K_{p(\mathrm{lin})}\left(\left(V_{GS}-V_{TH}\right)V_{DS}-\frac{K_{p(\mathrm{lin})}}{2K_{p(\mathrm{sat})}}V_{DS}^2\right)\times\frac{M\left(1+\lambda V_{DS}\right)}{2\left(1+\theta\left(V_{GS}-V_{TH}\right)\right)} \tag{1}$$

in the linear region, and

$$I_D = K_{p(\mathrm{sat})}\left(V_{GS}-V_{TH}\right)^2\frac{M\left(1+\lambda V_{DS}\right)}{2\left(1+\theta\left(V_{GS}-V_{TH}\right)\right)} \tag{2}$$

in the saturation region. Here, M is the avalanche Multiplication factor given by

$$M=\frac{1}{1-\left|\frac{V_{DS}}{BV}\right|^{BV_n}}. \tag{3}$$

In (1), (2), and (3), $K_{p(\mathrm{lin})}$ stands for the device transconductance in the linear region, $K_{p(\mathrm{sat})}$ represents the device transconductance in the saturation region, *BV* represents the breakdown voltage, and BV_n is the breakdown voltage index. The other symbols have their usual meanings.

Next, the transient behavior is modeled with a series of capacitors, between pairs of device terminals. The Miller capacitance has the most significant effect on the switching behaviour of the device; it is also very nonlinear as it is comprised of the series combination of the gate-drain oxide capacitance, C_{oxd}, and the gate drain depletion capacitance. This results in the following nonlinear capacitance:

$$C_{DG}=\frac{C_{\mathrm{oxd}}}{1+\frac{C_{\mathrm{oxd}}W_{DGj}}{A_{DG}\varepsilon_0\varepsilon_S}} \tag{4}$$

where A_{DG} represents the gate-drain overlapping area, and other symbols have usual meanings. Combining these effects, the model for the MOSFET portion of the overall IE-IGBT model has been developed. MOSFET's drain node (D) shown in Fig. 2, is an internal node within the overall model.

B. PiN Diode Section Model

In order to describe correctly static and dynamic behavior of the power bipolar devices, one has to incorporate into a device model conductivity modulation and nonquasistatic charge storage effects [17], [21], since they are the dominant factor in determining the dynamic and static current and voltage characteristics of these devices. When the excess carrier density overcomes the base doping level by several orders of magnitude ('plasma' condition), the assumption that $n \approx p$ is valid (*n* and *p* represent the total electron and hole concentration respectively). Then, the carrier transport is determined by the ADE

$$D\frac{\partial^2 p\left(x,t\right)}{\partial x^2}=\frac{p\left(x,t\right)}{\tau}+\frac{\partial p\left(x,t\right)}{\partial t} \tag{5}$$

where *D* represents the ambipolar diffusion constant and τ represents the ambipolar carrier lifetime. The ambipolar diffusion constant is related to the real electron and hole diffusion constants by

$$D=2D_nD_p/\left(D_n+D_p\right) \tag{6}$$

where D_n and D_p have their usual meaning, i.e., represent the diffusion constants for electrons and holes. The boundary conditions for the (5) are

$$\left.\frac{\partial p}{\partial x}\right|_{x_l}=\frac{1}{2qS}\left(\frac{I_{nl}}{D_n}-\frac{I_{pl}}{D_p}\right) \tag{7}$$

$$\left.\frac{\partial p}{\partial x}\right|_{x_r}=\frac{1}{2qS}\left(\frac{I_{nr}}{D_n}-\frac{I_{pr}}{D_p}\right) \tag{8}$$

and are valid for the concentration gradient at the left (x_l) and right (x_r) ends of the carrier storage zone. In the aforementioned

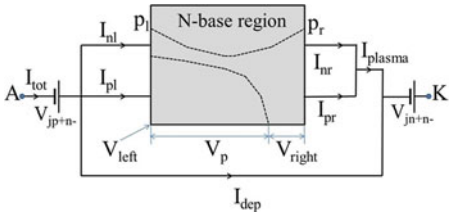

Fig. 3. Schematic of the PiN diode section model. The diode's cathode contact (K) corresponds to internal node D shown in Fig. 2. The dashed lines within the N-base region depict schematically on-state carrier distribution and carrier distribution at an arbitrary point during IE-IGBT device turn-off.

equations, *q* and *S* stand for the electron unity charge and cross section, respectively. I_{nl} and I_{pl} represent the electron and hole currents at the anode end of the carrier storage region and I_{nr} and I_{pr} represent electron and hole currents at the cathode end of the carrier storage region (see Fig. 3). The $I_{\rm plasma}$ is a total current flowing through the base region excluding the current component that charges and discharges anode-base depletion capacitor and is referred to as the plasma current.

A compact model for the PiN diode section model is shown in Fig. 3, the internal voltages and currents are incorporated in the diagram. The total voltage across the diode is the sum of various components as shown in Fig. 3. Voltages V_{jp+n-} and $V_{\rm left}$ represent the junction and depletion voltage drops across the p + n- junction, respectively.

Similarly, V_{jn+n-} and $V_{\rm right}$ account for the n + n- junction. Once again, n+ region exists due to n-base accumulation layer underneath the IE-IGBT gate. In addition, there is an ohmic voltage drop V_P across the plasma (carrier storage region), where conductivity modulation takes place whenever the plasma is present. The total plasma current, $I_{\rm plasma}$, consists of both hole and electron components within the plasma, additionally the depletion capacitance current, $I_{\rm dep}$, contributes to the total current $I_{\rm tot}$. The currents I_{pl}, I_{nl}, I_{pr}, and I_{nr} represent the individual electron and hole currents entering the plasma at the diode's anode and cathode.

To model plasma carrier distribution, an exponential shape function is used. In steady-state forward bias operation, the plasma carrier concentration has a distribution of catenary form with just two exponential basis functions giving

$$p = Ae^{x/L} + Be^{-x/L} \tag{9}$$

where the diffusion length, $L = \sqrt{D\tau}$. In transient operation, more complex profiles can be approximated using a number of exponential basis functions with a range of decay length parameters, shorter than the steady state ones.

In forward bias, the junction voltage drops can be calculated using the following:

$$V_{jp^+n^-} = V_T \log_e \left(\frac{p_l}{n_i} + \frac{n_i}{N_d} \right) \tag{10}$$

for the left hand (p^+n^-) side and

$$V_{jn^+n^-} = V_T \log_e \left(\frac{p_r + N_d}{n_i} \right) \tag{11}$$

for the right hand (n^-n^+) side, where V_T represents the thermal voltage, n_i represents the intrinsic carrier concentration and N_d stand for the n-base doping level.

The ohmic voltage drop across the plasma V_P is found by integrating the electric field E responsible for driving the drift currents in the plasma region

$$V_p = \int_{x_l}^{x_r} E dx \tag{12}$$

where E is found from the total hole and electron current in the plasma

$$I_{\rm plasma} = I_{\rm hole} + I_{\rm elec.} = qS\left(\mu_n\left(p + N_d\right) + \mu_p p\right) E. \tag{13}$$

Thus, from (12) and (13) the ohmic resistance R_P is found to be

$$R_P = \frac{V_p}{I_{\rm plasma}} = \frac{V_T}{qS\left(D_n + D_p\right)} \int_{x_l}^{x_r} \frac{1}{p\left(x\right) + N_{\rm eff}} dx \tag{14}$$

where Einstein's relation has been used to replace the mobilities μ_n and μ_p and the effective doping concentration in the base is defined as

$$N_{\rm eff} = \frac{N_d D_n}{D_n + D_p} \tag{15}$$

which arises from substituting (13) into (12). In order to solve (14) and determine R_P, the plasma region is divided in $n-1$ panels. Then, a linear plasma distribution *p(x)* is assumed inside every panel, this makes it possible to evaluate (14) analytically, thus R_P is determined as

$$R_P = \sum_{i=1}^{n-1} R_{i,i+1} \tag{16}$$

where $R_{i,i+1}$ is the resistivity associated with the panel between x_i and x_{i+1}.

In negative bias, V_{jp+n-} becomes zero and the depletion voltage ($V_{\rm left}$) is developed, this is related to the depletion width x_l, for a uniformly doped base region, as

$$V_{\rm left} = -\frac{qN_d}{2\varepsilon_0\varepsilon_s} x_l \left(x_l + 2x_0\right) \tag{17}$$

where $\varepsilon_0\varepsilon_s$ is the permittivity of the base region and x_0 is related to the junction in-built voltage V_{bi}, which is given as an external parameter, as

$$x_0 = \sqrt{\frac{2\varepsilon_0\varepsilon_s V_{bi}}{qN_d}}. \tag{18}$$

Note that $V_{\rm left} = 0$ when $x_l = 0$, so that, for convenience, the origin for *x* has been taken as the edge of the depletion region at zero bias rather than at the metallurgical junction. Similar expressions may be obtained for $V_{\rm right}$ in terms of the depletion width $w - x_r$. Under high reverse current conditions, such as during turn off, N_d in (17) must be modified by the presence of large numbers of holes flowing through the depletion region,

it is thus replaced by

$$N_d + \frac{|I_{\rm plasma}|}{qSv_{psat}} \tag{19}$$

where v_{psat} is the high field saturation velocity of the holes.

The presence of the depletion region gives rise to a small extra current component under high-speed transient conditions

$$I_{\rm dep} = -qSN_d \frac{dx_l}{dt} \tag{20}$$

where $I_{\rm dep}$ is in the forward direction and is added to the plasma current $I_{\rm plasma}$ giving a total current of

$$I_D = I_{\rm tot} = I_{\rm plasma} + I_{\rm dep}. \tag{21}$$

The diode model is implemented with the aid of a suitable set of system variables which are nonlinearly coupled through the preceding equations to the diode voltage and current. The system variables chosen were

$$[V_{\rm anode}, V_{\rm cathode}, I_{\rm tot},\ p_l,\ p_r,\ x_l,\ x_r]\,.$$

An equation is associated with each system variable and solved in conjunction with the other equations of the connected external network at each time step of the simulation. The model is originally developed in FORTRAN programming language, and could easily be transferred to MATLAB for example. More details on the model implementation and exponential function representation of the carrier distribution is given in [26], and they are not repeated here for the sake of clarity.

C. Assembly of the Compact IE-IGBT Model

The model of the planar IE-IGBT is obtained combining two previously described models for the MOSFET and PiN devices.

On the left hand side of the carrier storage region, we have the same conditions as the ones described for the PiN diode (electrons penetrate the p^+ region and recombine there giving rise to recombination current I_{nl}, and p-emitter injects hole into the n-base region, giving rise to the diffusion current I_{pl}) and no changes are needed in the model. On the right hand side, the electron current I_{nr} is actually MOSFET channel current I_{ch} (see Fig. 4) this writing the boundary condition for the carrier storage region as

$$\left.\frac{\partial p}{\partial x}\right|_{x_l} = \frac{1}{2qS}\left(\frac{I_{nl}}{D_n} - \frac{I_{\rm plasma} - I_{nl}}{D_p}\right) \tag{22}$$

$$\left.\frac{\partial p}{\partial x}\right|_{x_r} = \frac{1}{2qS}\left(\frac{I_{ch}}{D_n} - \frac{I_{\rm plasma} - I_{ch}}{D_p}\right) \tag{23}$$

and the MOSFET and bipolar parts of the model are coupled together in this way. (23) denotes an important boundary condition for the ADE and, unlike the Hefner model [15], which assumes that the carrier concentration at the device's cathode side is zero, the carrier concentration at the cathode side is determined by solving the model equations self-consistently for the given boundary conditions. Finally, the capacitances $C_{\rm GD}$ and $C_{\rm GS}$ shown in Fig. 4 are the same as the ones described for the MOSFET model, and the capacitance existing between anode and the cathode of the IE-IGBT is modeled by the depletion current $I_{\rm dep}$

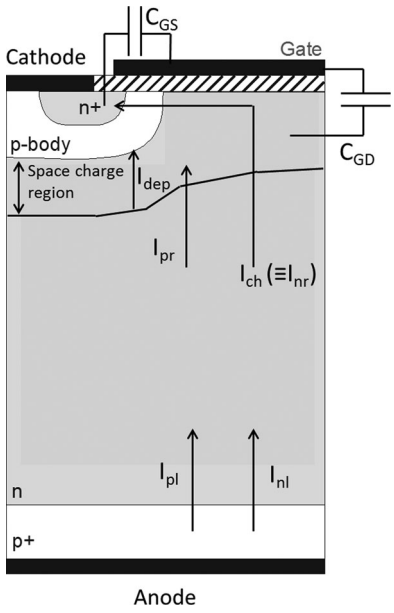

Fig. 4. Schematic of the planar IE-IGBT compact model.

$$I_{\rm dep} = -qSN_d \frac{d\,(w - x_r)}{dt}. \tag{24}$$

III. Measurement Test Rig

IE-IGBT measurement test rig is presented in Fig. 5.

The double-pulse switching test circuit incorporates two IE-IGBTs (TOSHIBA's press-pack 4.5 kV/1.5 kA devices), named TR1 and TR2 on the schematic, and two capacitors, denoted as C1 and C2. There are two gate drive circuits feeding the gates of the transistors 1 and 2. All the inductances, except the 400-nH load inductance $L_{\rm load}$, shown on the schematic are stray inductances, and their values are included in the schematic. The higher value stray inductances (above 30 nH) have been measured and the others are estimated. When switch S1 closes, capacitor C1, also called energy storage capacitor, is charged to a high voltage just below 3 kV by the high-voltage power source. From the circuit diagram, capacitor C2 will be charged to the same level. Once the transistor 1 is turned ON by the gate driver generated pulse, current flows from C1, through load inductance and transistor 1 back to C1. Capacitor C1 has a large value securing linear current increase and the duration of the pulse is selected to guarantee that the current reaches required level at the time TR1 is turned OFF. Once TR1 is OFF, the voltage starts to build across its output terminals. When this voltage rises above the value of the voltage across capacitors C1 and C2, the current commutates into the freewheeling diode D2 associated to TR2, at a rate determined by the voltage rise rate and the stray inductances. The duration of first pulse on-time is usually set to around 100 μs for these voltage and current levels. The current decays very slowly as it pass through $L_{\rm load}$ and D2.

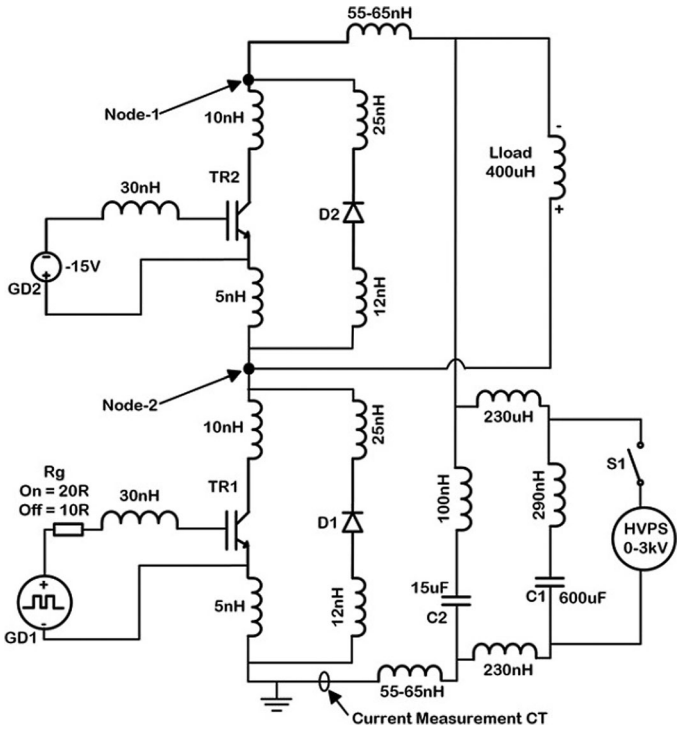

Fig. 5. Circuit diagram of characterization double-pulse switching test rig.

TABLE I
SUMMARY OF THE EXPERIMENTAL VERSUS MODELING RESULTS, INCLUDING RELATIVE ERROR

Parameter Description	Experiment	Model	Error (%)
First Pulse End–Current Level	1123 A	1177 A	5
First Pulse End–Voltage Overshooting	2962 V	3156 V	6
Second Pulse Start–Voltage Level	2338 V	2331 V	0.2
Second Pulse Start–Current Overshooting	2038 A	1847 A	10
Second Pulse Start–Current Level	1029 A	1079 A	5
Second Pulse End–Current Level	1413 A	1461 A	3
Second Pulse End–Voltage Overshooting	2895 V	3103 V	7
First Pulse End–Current Fall Time	0.62 μs	0.63 μs	2
First Pulse End–Voltage Rise Time	0.98 μs	0.89 μs	10
First Pulse End–Current Delay Time	7.73 μs	7.23 μs	7
First Pulse End–Voltage Delay Time	6.54 μs	6.21 μs	5
Second Pulse Start–Current Delay Time	4.89 μs	4.56 μs	7
Second Pulse Start–Voltage Delay Time	4.99 μs	4.97 μs	0.4

Capacitor C2 provides a lower loop inductance at turn-off and turn-on.

After few hundred microseconds, transistor TR1 is turned ON again by second gate pulse. Current starts to build in TR1, C1, and C2, and simultaneously it reduces in D2. Once its current reaches zero value, diode D2 starts conducting the reverse recovery current also flowing in C1, C2, and TR1 (in addition to load current). Approximately after further 100 μs, transistor 1 is turned OFF again. Once again, current commutates into D2 and flows around $L_{\rm load}$ and D2, until it decays to zero. The single test cycle is now over. The transients of the great interest are the first turn-off and the second turn-on. Note that they are occurring at the similar load current (see Table I). The voltages

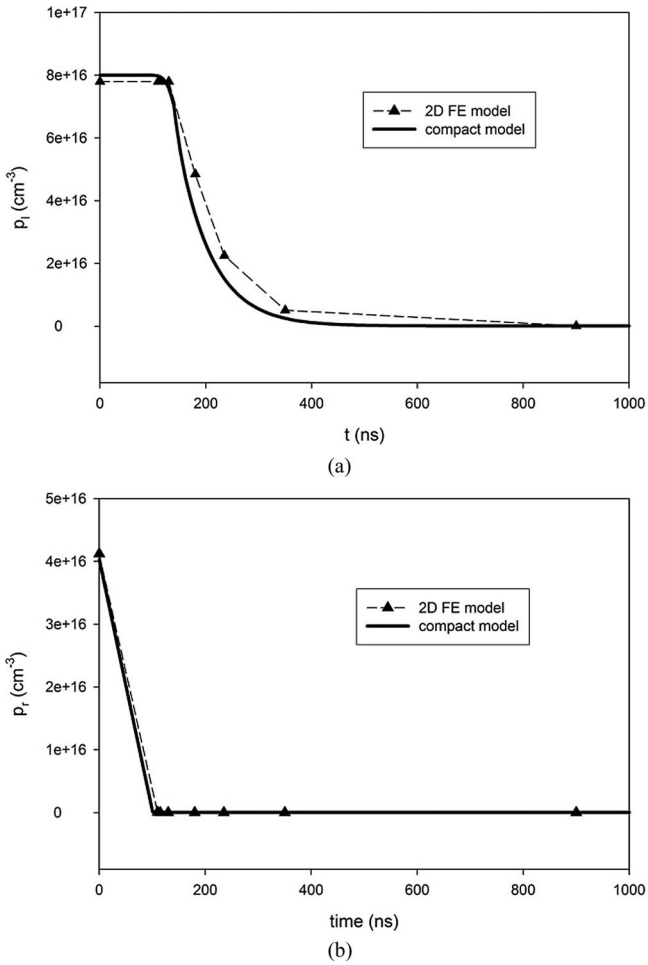

Fig. 6. Prediction of the excess carrier storage evolution during IE-IGBT turn-off (a) at the anode/n-base end and (b) at the cathode end (at the point D of Fig. 2).

are measured at two points denoted as Node 1 and Node 2 in the Fig. 5, and these values are used to determine the potential across TR1 and TR2. The current measurement point is also shown at the diagram, and the high accuracy current transformer has been employed for these measurements.

IV. RESULTS AND DISCUSSIONS

A dozen IE-IGBTs have been subjected to double-pulse switching test, and the experimental results were averaged. In this way, compact model parameters extracted could be used to represent any of these devices rather than the single one. The simulation circuit that mimics the experimental test circuit has been assembled and simulation of the double pulse test executed. The values of the IE-IGBT's model parameters are as follows: the total device area, $A = 25$ cm^2, width of the n-base region, $w = 600$ μm, doping of the n-base region, $N_d = 2 \times 10^{13}$ cm^{-3}, ambipolar lifetime, $\tau = 0.4$ μs, device transconductance in the linear region, $K_{p(\rm lin)} = 63$ A/V^2, device transconductance in the saturation region, $K_{p(\rm sat)} = 36$ A/V^2, the gate source capacitance (see Fig. 4), $C_{\rm GS} = 0.6$ nF, gate drain capacitance, $C_{\rm GD} = 1.6$ nF, the

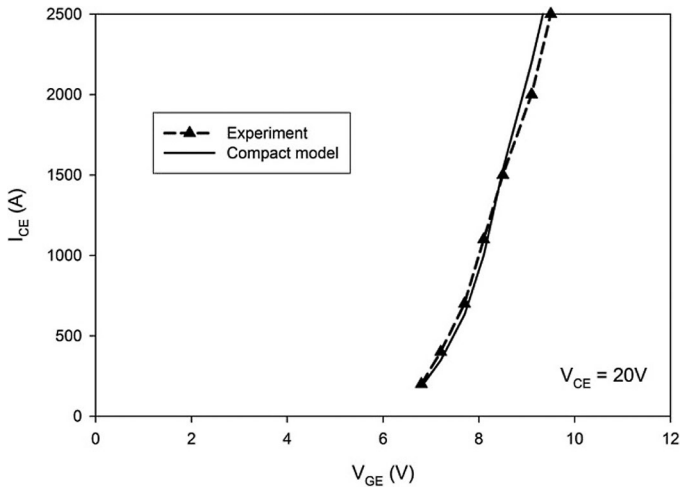

Fig. 7. DC $I_{CE}-V_{GE}$ transfer characteristic, compact model result versus experiment.

breakdown voltage $BV = 4500$ V, and the breakdown voltage index $BV_n = 4$. The physically based PiN diode compact model, as well as model parameters, described in great details in [26] has been used to model the freewheeling diode D2. The values of the diode model parameters are as follows: the diode area, $A_D = 9\ \mathrm{cm}^2$, width of the diode n-base region, $w_D = 600\ \mu\mathrm{m}$, doping of the n-base region, $N_{dD} = 2 \times 10^{13}\ \mathrm{cm}^{-3}$, ambipolar lifetime, $\tau_D = 0.4\ \mu$s, hole end leakage saturation current, $I_{rp0} = 2 \times 10^{-11}$ A, electron end leakage saturation current, $I_{\mathrm{ln}0} = 2 \times 10^{-12}$ A.

To indicate the IE-IGBT model accuracy, the characteristics showing decay of the excess carrier concentration at the anode/n-base junction, p_l, and at the cathode end (at the point D of Fig. 2), p_r, during the device turn-off are shown in Fig. 6, and compared against the results obtained from the fully physical drift-diffusion 2-D FE model. As set within the compact model, the carrier concentration change follows the Gaussian profile determined by two parameters, the pic excess carrier concentration and the Gaussian spreading factor. It can be seen from the Fig. 6(a), the carrier concentration p_l reduces monotonically during the turn-off, and the results are in very good agreement with the FE ones. The Hefner model described in [15] predicts sudden rise in the carrier concentration during the turn off, but this has since not been confirmed theoretically or experimentally. From Fig. 6(b), one can see that the excess carrier concentration at the cathode end reduces at greatly faster rate; the depletion region forms at the cathode end at around 100 ns and it spreads toward the anode region swiping the excess charge carriers away.

The dc transfer characteristic $I_{CE}-V_{GE}$ is shown in Fig. 7.

The long-time current waveforms during the double pulse switching test are shown in Fig. 8, Fig. 8(a) and (b) show experimental results, and Fig. 8(c) shows simulation results. The long-time voltage waveforms are shown in Fig. 9, experimental results in Fig. 9(a), and simulation results in Fig. 9(b). To avoid voltage oscillations seen in Fig. 9(a) and to reduce CPU time, models for several stray capacitors needed to be included in

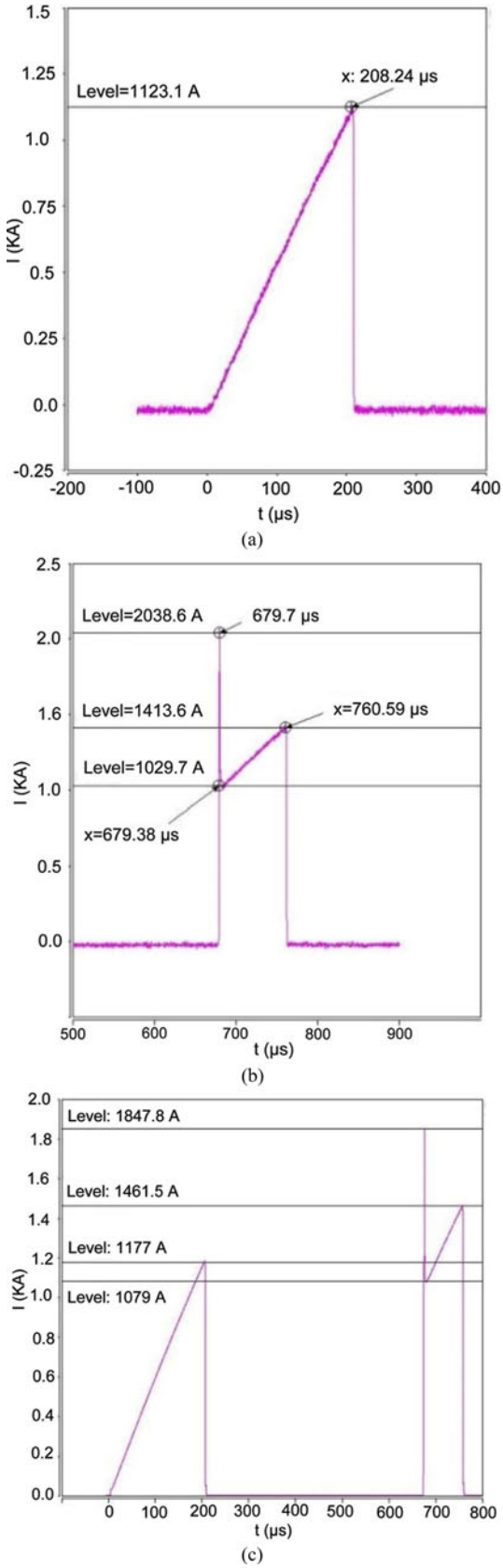

Fig. 8. Double pulse switching test: (a) experimental results, first pulse long-time current waveform, (b) experimental results, second pulse long-time current waveform (c) simulation results, complete long-time current waveform.

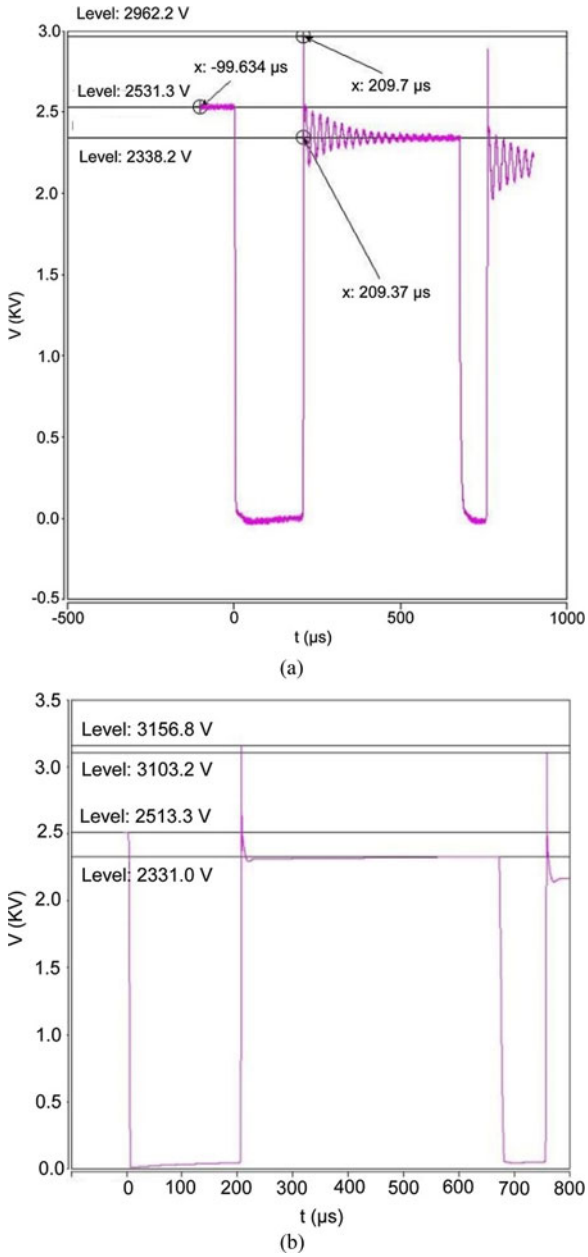

Fig. 9. Double pulse switching test: (a) experimental result, complete long-time voltage waveform, and (b) simulation result, complete long-time voltage waveform.

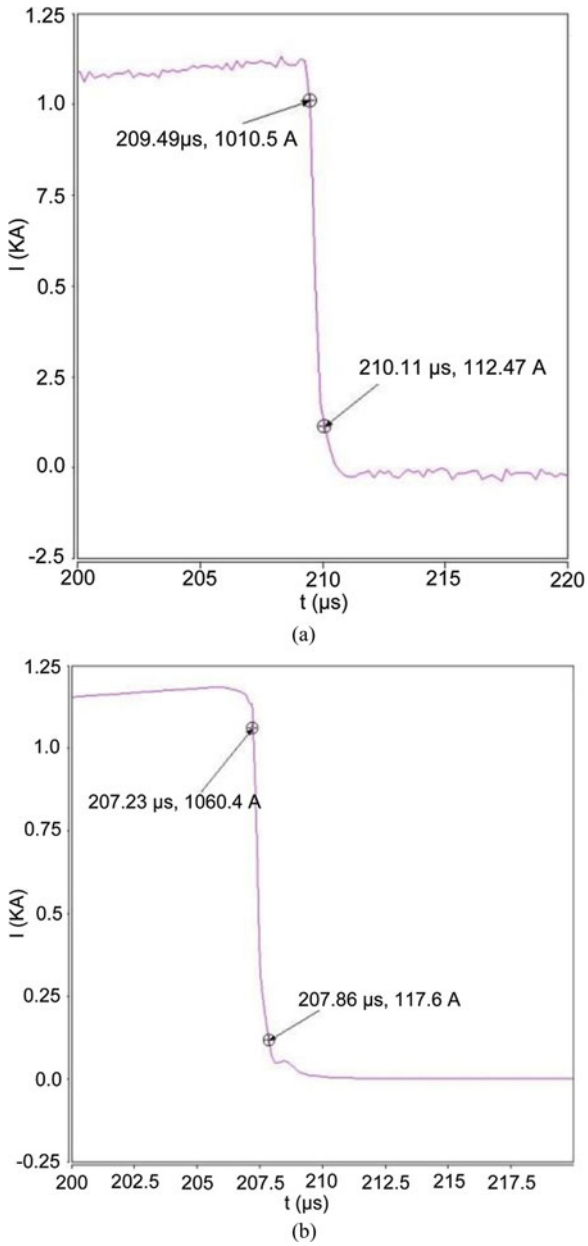

Fig. 10. Double pulse switching test: (a) first pulse current turn-off experimental result, (b) first pulse current turn-off simulation result.

the simulation circuit. Fig. 10(a) shows the first pulse current turn-off experimental result and Fig. 10(b) includes simulation result. Fig. 11 shows the voltage waveforms (rise of the anode voltage) during the same time instance, i.e., first pulse turn-off. Fig. 12 shows current waveform (current rise) during second pulse turn-on, (a) experimental and (b) simulation results.

Large spike seen on both, experimental and simulation curves, corresponds to freewheeling diode reverse recovery current. Fig. 13 shows anode voltage decay during second pulse turn-on time.

The most important voltage and current signal parameters are listed in Table I, their experimental and simulation values extracted from the appropriate graphs are included for comparison. The voltage and current levels compared are clearly indicated in Figs. 8 to 13. The current (voltage) fall time has been defined as the time needed for current (voltage) to fall from 90% of its original value to 10% of its original value. Similarly, the current (voltage) rise time has been defined as the time needed for current (voltage) to rise from 10% of its final value to 90% of its final value. Those current (voltage) points (or the nearest available ones) are also clearly indicated in the Figs. 8 to 13. The original aim of the exercise, specified to satisfy industrial needs, was to develop compact model capable of achieving match with experimental results with a maximum error of 10%

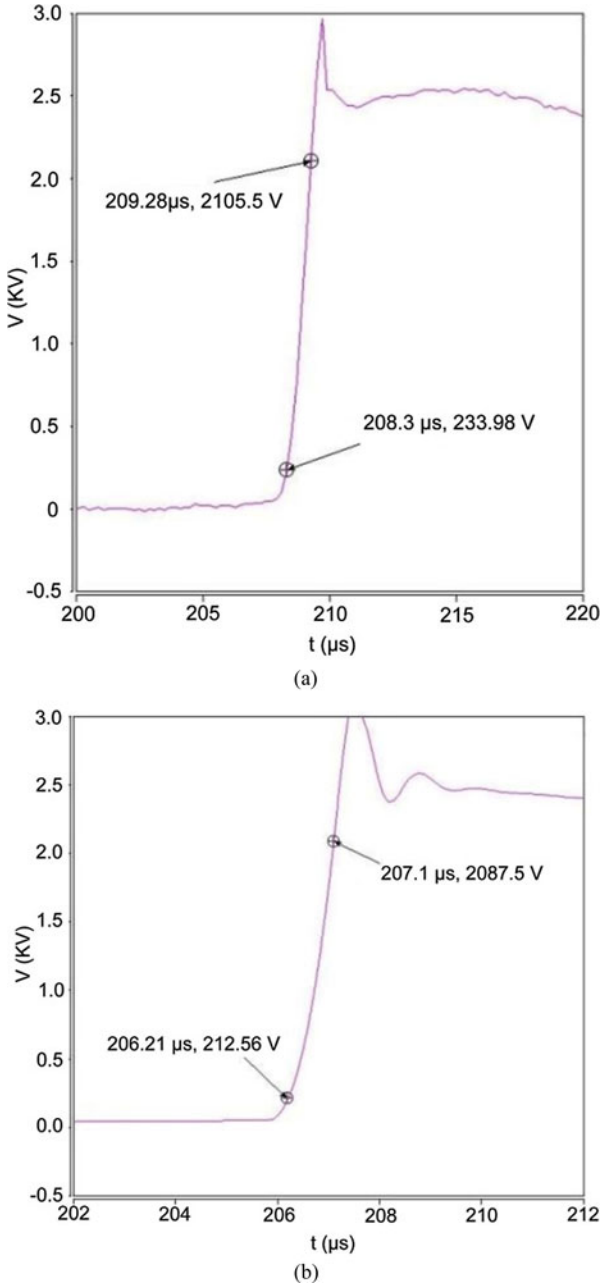

Fig. 11. Double pulse switching test: (a) first pulse voltage turn-off experimental result, (b) first pulse voltage turn-off simulation result.

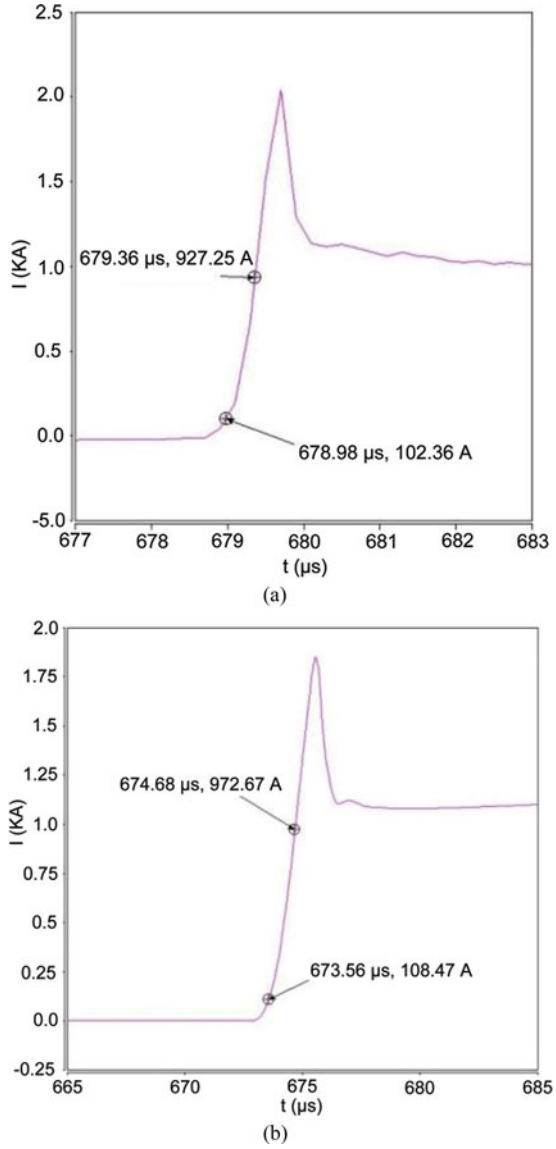

Fig. 12. Double pulse switching test: (a) second pulse turn-on current experimental result, (b) second pulse turn-on current simulation result.

across all the parameters. As can be seen from the Table I, this has been successfully achieved.

V. Conclusion

The compact model of a planar injection enhanced IGBT based on the exponential solution of the ADE is presented in this paper. To model plasma carrier distribution, an exponential shape function is used, and in steady-state forward bias operation, the plasma carrier concentration has a distribution of catenary form with just two exponential basis functions, while in transient operation, more complex profiles can be approximated using a number of exponential basis functions with a range of decay length parameters, shorter than the steady state ones.

The compact model has been originally developed in FORTRAN and MATLAB, and then implemented into Saber circuit simulator. The part of the code providing the exponential solution of the ADE has been included in the Saber simulator as FORTRAN library file.

Device model developed has been successfully tested against complete set of the high current, high voltage experimental results, with a maximum error of 10% across all the parameters.

The model does not have limitations regarding applicable breakdown voltage range; the breakdown voltage value is set as a model parameter. The model can also be applied for the wide range of devices with different cell pitch sizes and current capabilities by adjusting correctly total device area model parameter.

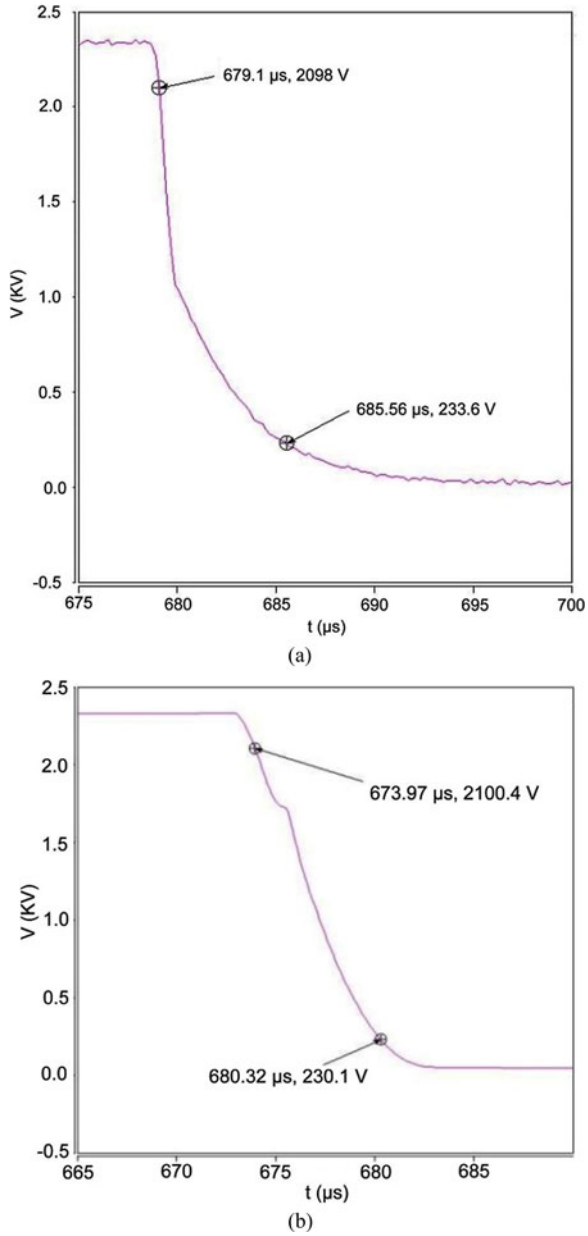

Fig. 13. Double pulse switching test: (a) second pulse turn-on voltage experimental result, (b) second pulse turn-on voltage simulation result.

ACKNOWLEDGMENT

The author would like to thank ALSTOM T&D for providing experimental data for this study.

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