Double-Phase High-Efficiency, Wide Load Range High- Voltage/Low-Voltage *LLC* DC/DC Converter for Electric/Hybrid Vehicles

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***Abstract*—In this paper, a 2.5-kW 330–410-V/14-V, 250-kHz dc/dc converter prototype is developed targeted for electric vehicle/hybrid vehicle applications. Benefiting from numerous advantages brought by the *LLC* resonant topology, this converter is able to perform high efficiency, high power density, and low EMI. To arrange high-output current, this paper proposes a parallel-connected *LLC* structure with developed novel double-loop control to realize an equal current distribution and an overall efficiency improvement. Considering the *LLC* cell's dimensioning, this paper establishes a more precise model by taking the secondary leakage inductance into consideration. System amelioration and design considerations of the developed *LLC* are also presented in this paper. A special transformer is presented, and various types of power losses are quantified to improve its efficiency. This converter also implements synchronous rectification, power semiconductor module, and an air-cooling system. The power conversion performance of this prototype is measured and the developed prototype attains a peak efficiency of 95% and efficiency is higher than 94% from 500 W to 2 kW, with a power density of 1 W/cm^3. Finally, the EMC results of this prototype are also measured and presented.**

***Index Terms*—Current sharing, efficiency improvement, *LLC* resonant converter, magnetic components, prototype development.**

I. Introduction

THE electric vehicle is principally powered by a high-voltage (HV) battery permitting to drive the traction chains. The HV battery is selected according to the required power and the targeted autonomic distance, varying from 100 to 400 km. A dc/ac inverter converts the HV battery voltage to three-phase ac voltage to drive the electric motors. Other equipments are all powered by a classical 14-V low-voltage (LV) network. In order to charge the LV network, all the electric vehicles are equipped with an HV/LV dc/dc converter generating an insulated 14-V voltage based on the HV battery. A secondary 14-V battery is connected at the LV network for the start, stop, and diagnostic phases, while the HV battery is not activated during these phases. In electric/hybrid vehicles, the targeted 2.5-kW automobile dc/dc converter may operate at any power from 0 to 2.5 kW, but the estimated operation time is different at different power ranges: the converter has higher probabilities in operating mainly at two power ranges: 600–900 W and 1.5–1.8 kW. Assuring high conversion efficiency at these above two power ranges is very important to improve the overall performance of the converter in energy savings.

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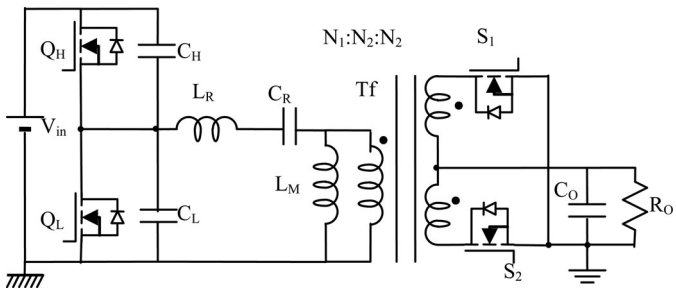

Fig. 1. Half-bridge *LLC* converter with synchronous rectification.

The *LLC* converter, with its topology shown as in Fig. 1, is now in rapid development and application in front-end energy conversion systems. The *LLC* converter is able to perform ZVS at primary switch and ZCS at secondary switch; thus, the switching frequency of *LLC* is higher than the traditional PWM converter. The resonant tank contains two inductors: one resonant capacitor and a transformer. The inductor $L_{\rm m}$ can be integrated into the transformer as its magnetizing inductance. Furthermore, the resonant inductor can be fully or partially integrated into the transformer's leakage inductance. The overall volume of magnetic components thus can be minimized; this is also a great advantage of the *LLC* converter over other converter types.

For HV/LV power conversion, the *LLC* resonant converter generally keeps a very competitive efficiency in designing dc/dc power supplies in low- or medium- power level [1]–[7]. Generally, the reported *LLC* resonant converters in the literature are under 1 kW, especially between 300 W and 1 kW [8]–[10]. Increasing load brings the following two main difficulties.

The first difficulty lies in the transformer core realization. The required transformer's magnetizing inductance in *LLC* is proportional to its load resistance. For 2.5-kW *LLC*, the required $L_{\rm m}$ is 21 μH, with a transfer ratio $N_1/N_2 = 16$. Even if the secondary turn number is set to $N_2 = 1$, an inductance factor of $A_L = 82$ nH is needed, which is too low to be realized practically and the required air-gap length is about 4 mm. Currently, no commercial magnetic cores are available in the market with such a huge

air gap. Furthermore, huge air gap enables more fringing flux penetrating the windings and causes additional winding losses due to eddy current. If the output power is half reduced, the inductance factor is then increased to $A_L = 165$ nH. A rational air-gap length $e \approx 2$ mm is sufficient for creating the required inductance factor and many magnetic cores are available at the market, such as E41/21/15, E41/21/20, E42/33/20, etc.

The second difficulty is that higher power increases sharply the conduction losses at the semiconductor devices and transformers. The high RMS current at the primary and secondary side leads to parallel more MOSFETs at both HV switch and LV switch. The number of strands in transformer's windings should also be increased; thus, it results in a larger transformer volume, which makes it even more difficult for obtaining a low magnetizing inductance.

II. Proposed Parallel–Parallel Topology and Current Sharing Control Strategy

As increasing the power level brings the above described difficulties, it is a more suitable solution to adopt more power cells to share the total current. Adopting two power cells to share the current is selected in this converter development.

A. Traditional Phase-Shift Control LLC and Its Current Sharing Problem

The double-phase interleaving *LLC* with 90° phase-shift control method has appeared in several literature works [11]–[16] as a good candidate to manage high-power applications. The method described in the above papers is to operate both the two phases at the same frequency with one same controller driver, but with a phase shift of 90° between adjacent cells to get an output current with fewer ripples. However, resonant cell component mismatch causes the two cells to exhibit different voltage conversion ratio characteristics; as a result, the load current is no longer equally distributed among the two power cells. This is also to say, supersymmetry should be kept among both the power cells. For example, if the cell A adopts the calculated tank parameters with $L_r = 7.5$ μF, $L_m = 42$ μF, $C_r = 50$ nF; the cell B adopts -10% capacitor tolerance with $L_r = 7.5$ μF, $L_m = 42$ μF, and $C_r = 45$ nF. The current sharing results are shown in the Fig. 2.

The given input voltage and output voltage imposes a power cell gain of 1.3 required for both the two cells. If the output current is equally distributed between the two cells, the cell A operates at the point "a" with a gain less than 1.3 and the cell B operates at the point "b" with a gain more than 1.3. With parallel connection, both the two power cells should perform the same gain as they share the same input/output voltage at the same operational frequency of 169 kHz. Thus, the cell A tends to share less load to increase its voltage conversion ratio, and the cell B turns to share more load to decrease its voltage ratio. The operational point of cell A shifts from "a" to "c" (with gain curve shift from black line to blue line), and the operational point of cell B shifts from "b" to "c" (with gain curve shift from red line to green line). The system then stabilizes and voltage conversion ratios of both the two power cells are equal

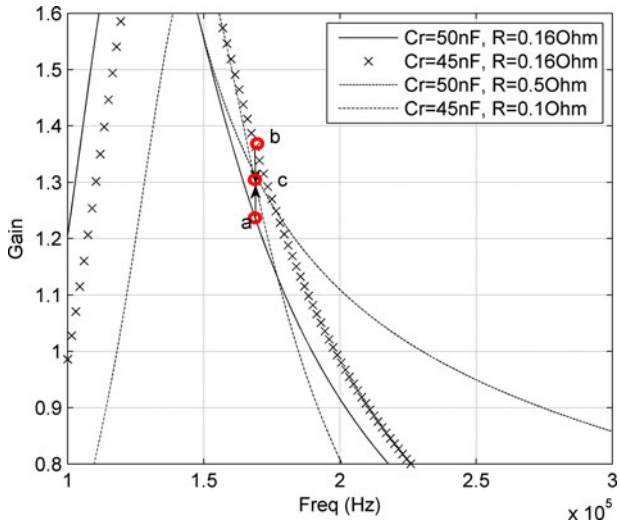

Fig. 2. Operational point movement with component mismatch at $V_{\rm in} = 360$ V, $V_o = 14$ V, and $P = 1250$ W under phase-shift control.

to 1.3. The cell A's load resistance is increased to 0.5 Ω, and the cell B's load resistance is decreased to 0.1 Ω, which causes a current dissymmetry of 16.7%. It is obvious that the phase-shift double-cell interleaved *LLC* experiences current sharing problems and is difficult to keep an equal current sharing. In the automobile industry, with high quantities of dc/dc to produce, a certain number of prototypes will encounter current sharing problem and will be failed products due to components value dispersions.

B. Proposed Double-Cell Topology and Double-Loop Control for Equal Current Sharing

In order to satisfy the equal current balancing requirements in double-phase parallel–parallel *LLC* resonant converter, a novel control circuit is proposed in this paper [17]. The novel control method adopts two regulation loops: external output voltage loop and internal input current loop. It assures a current balancing among different paralleled power cells by controlling each cell's input current. Fig. 3 shows the proposed double–phase resonant converter with primary input current sensors R_A and R_B.

The block schematic of the proposed novel control circuit for input current balancing adapted to the double-phase *LLC* converter is depicted in Fig. 4. The current shunt R_A of the power cell A and R_B of the power cell B forward the sensed input current signals in forms of $V_{\rm RA}$ and $V_{\rm RB}$, separately. The sensed signals are filtered and amplified to a suitable level (noted as $I_{\rm mA}$ and $I_{\rm mB}$) and they reflect the average active input current of each cell. The whole control loop contains an external voltage control loop and an internal current control loop. The output voltage is compared with the reference voltage $V_{\rm ref}$ and the comparison error e_V is regulated by a PI corrector. The voltage regulation gives a unique current reference $I_{\rm ref}$ for both the two power cells. This $I_{\rm ref}$ should be isolated from LV part and limited to a certain value to avoid overcurrent problems. The measured currents

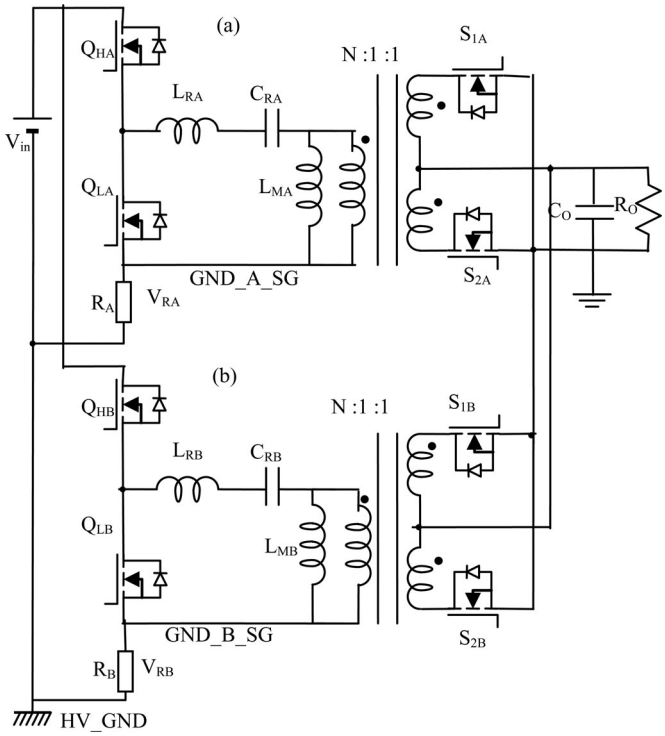

Fig. 3. Proposed double-phase *LLC* resonant converter with primary current sensors.

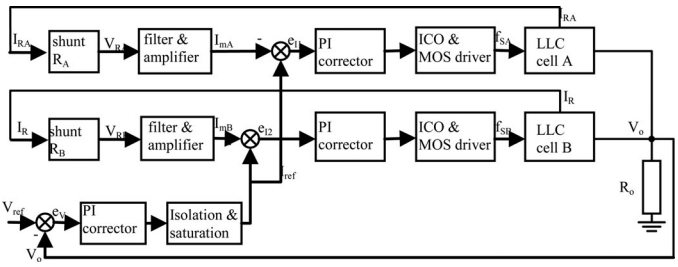

Fig. 4. Block schematic of the control circuit for input current balancing applied to the double-phase *LLC* converter.

I_{mA} and I_{mB} are regulated to I_{ref} by its respective PI corrector, while a uniform input current balancing among different power cells can be assured. The signals after current corrector are sent to different current controlled oscillators and MOSFETs drivers to drive different *LLC* power cells. It is apparent that under component mismatch, two converters operate at different frequencies f_{SA} and f_{SB} to keep the same voltage conversion ratio. The operational difference of these two control strategies can be explained essentially in Fig. 5.

As reported in Fig. 5, using proposed double-loop control, the case is not the same as that in Fig. 2. Other than varying its load to adapt to the same voltage conversion ratio, the power cell varies its switching frequency to attain the same target. With double-control loop and different drivers for different power cells, the switching frequencies for the two cells are not forced to be the same but to be independent of each other. The power cell A operates at 163.5 kHz and power cell B operates at 173 kHz.

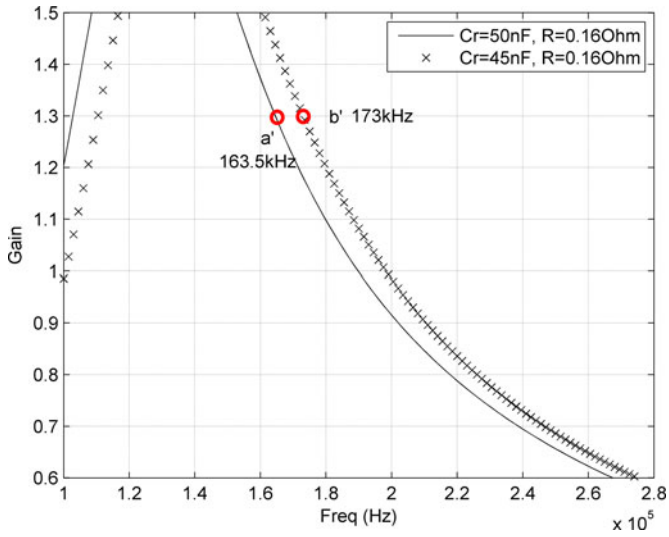

Fig. 5. Operational points determination for two-phase parallel *LLC* with component mismatch at $V_{\mathrm{in}} = 360$ V, $V_o = 14$ V, and $P = 1250$ W under the proposed double-loop control.

Each cell shares a load resistance of 0.16 Ω and there is no current sharing problem in this control strategy. It has to be reminded that although the proposed control strategy is applied to double-phase *LLC* resonant converters, but the principle can be easily promoted to *N* phase ($N \geq 2$) *LLC* resonant converters by adjusting the number of current control loops.

The ameliorations brought by the proposed double-phase *LLC* topology not only lies in the aspects of current sharing, but also in the following aspects: first, at light load, one power cell is switched OFF to obtain high-conversion efficiency. A predefined cell switching logic is applied to ensure an equal aging speed of the two power cells by switching OFF cell A or B following a given sequence. The converter's operating life can also be greatly extended. Second, at high load, if one power cell is OFF by incident, the maximum power of the other cell is limited by the saturation of I_{ref}, which avoids that all the power passes through another cell. Overcurrent problems can be easily avoided.

III. *LLC* Converter Modeling

The first harmonic analysis (FHA) method is a common method for establishing the equivalent electrical circuit of *LLC* converter by approximating the voltage/current waveforms as first-order sinusoidal wave, while neglecting the impacts of the other high-order harmonics [18]. The gain of the resonant tank at normalized frequency domain following the FHA analysis is represented as follows:

$$G = \frac{1}{\left(1 + \lambda - \lambda \frac{1}{f_n^2}\right) + jQ\left(f_n - \frac{1}{f_n}\right)} \tag{1}$$

where $Q = \sqrt{L_r/C_r}\Big/R_{\mathrm{ac}}$ is the quality factor of the resonant converter, $f_n = f_s/f_r$ is the switching frequency after normalization, $f_r = 1/2\pi\sqrt{L_r C_r}$ is the main resonant frequency,

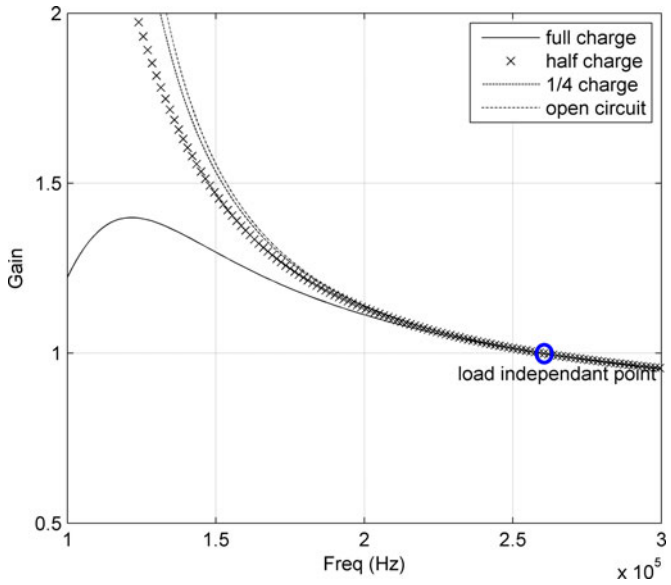

Fig. 6. Ideal *LLC* characteristics with $L_r = 7.5\ \mu$H, $C_r = 50$ nF, and $L_m = 42\ \mu$H.

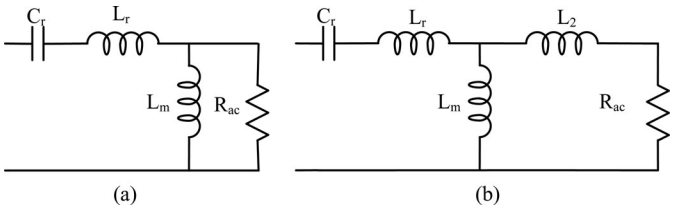

Fig. 7. Equivalent circuit of the *LLC* resonant converter cell (a) without or (b) with secondary leakage inductance.

$f_{r2} = 1\Big/2\pi\sqrt{(L_r + L_m)\,C_r}$ is second resonant frequency, and $\lambda = L_r/L_m$ is the ratio between the leakage inductance and the magnetizing inductance. Equation gives the voltage conversion ratio for an ideal *LLC* power cell, with its characteristics shown as in Fig. 6.

Working at the ZVS discontinuous current mode is highly preferred in *LLC* dimensioning, since the operational frequency region is limited between two resonant frequencies and the ZVS at full load range can be assured. The primary leakage inductance of a transformer can be integrated with the series resonant inductor; however, the influence of the secondary leakage inductance can neither be integrated nor neglected. Secondary leakage inductance exists in all transformers, whose value depends on the coupling factor and its external wire length. In this project, an additional wire length of 14 cm is needed at the transformer's secondary side to connect the LV MOSFET module and the output PCB filter board, while the leakage inductance is measured to be $l_2 = 100$ nH. In this particular application, the impedance of this secondary leakage inductance is increasing (116 mΩ at 150 kHz, 193 mΩ at 250 kHz) and even rise up to be the same order as the nominal load $R = 160$ mΩ. Its effect should thus be considered in the design and dimensioning of power cell parameters [19]. Fig. 7 shows the ac equivalent circuits of an ideal

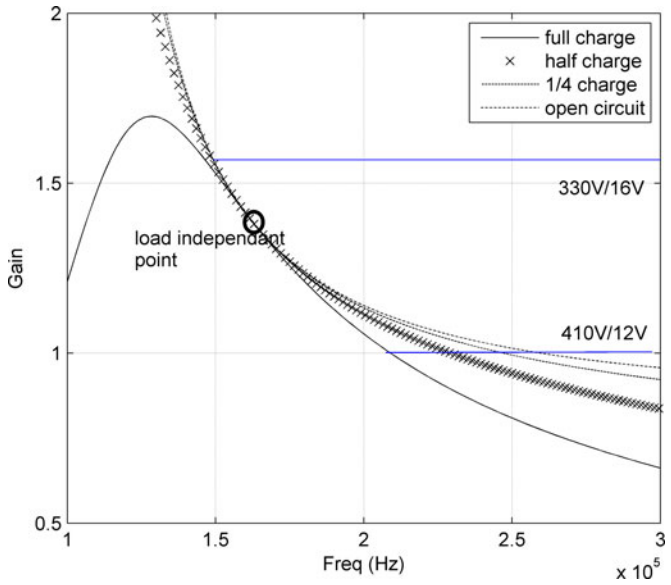

Fig. 8. Voltage conversion ratio of the *LLC* resonant cell with $L_r = 7.5\ \mu$H, $C_r = 50$ nF, $L_m = 42\ \mu$H, and $l_2 = 100$ nH.

LLC resonant cell and an *LLC* cell including secondary leakage inductance.

The voltage conversion ratio of *LLC* converter including the leakage inductance after normalization can be written as

$$G = \frac{1}{\left(1+\lambda-\lambda\frac{1}{f_n^2}\right)+jQ\left(\left(\frac{L_2}{L_m}\left(1+\frac{1}{\lambda}\right)+1\right)f_n-\left(\frac{L_2}{L_m}+1\right)\frac{1}{f_n}\right)} \tag{2}$$

where L_2 is the secondary leakage inductance transferred to the primary side, $L_2 = l_2/n^2$. The *LLC* characteristics considering secondary leakage inductance are presented in Fig. 8.

Several conclusions can be drawn based on the developed equation.

1) At no load, $Q = 0$, the voltage gain remains the same as in ideal *LLC* resonant converters. This is easy to understand, since there is no current in the secondary leakage inductance.
2) At the normalized frequency $f_n = 1$, the gain expression can be written as
$$G = \frac{1}{1+jQ\left(\frac{L_2}{L_r}+1\right)}. \tag{3}$$
Due to the imaginary part in the above equation, the gain at $f_n = 1$ is less than 1, except for open circuit. This means that the main resonant frequency is no longer a load independent point. At low $R_{\rm ac}$ (high Q), the gain is lower. This is due to the fact that at lower $R_{\rm ac}$, the leakage inductance's impedance is closer to the load resistance and it plays a role of voltage divider.
3) By imposing the imaginary part of (2) equal to 0, it is possible to derive the new load-independent point at the

following frequency:

$$f_{\text{ind}} = \sqrt{\frac{\frac{L_2}{L_m}+1}{\frac{L_2}{L_m}\left(1+\frac{1}{\lambda}\right)+1}}. \quad (4)$$

The gain at the new load-independent point can be obtained as

$$G_{f=\text{find}} = \frac{L_m + L_2}{L_m}. \quad (5)$$

Equation (5) shows that the voltage conversion gain at load- independent point including secondary leakage inductance is higher than 1; moreover, it increases with the increase of L_2. By developing (4), the frequency at the independent point can be derived as

$$f_{\text{ind}} = \frac{1}{2\pi\sqrt{C_r(L_r + L_m//L_2)}}. \quad (6)$$

From (6), it is obvious that the new load-independent point appears at a frequency where C_{r} is in resonant with all the three inductors. The new independent frequency locates between the main resonant frequency and second resonant frequency. In conclusion, the leakage inductance moves the load-independent point to left with a gain higher than one.

4) As to a same Q value, the maximum voltage conversion ratio is increased by including secondary leakage inductance compared with the ideal *LLC*. As studied in the above section, the maximum gain obtained in ideal *LLC* resonant cell at full load is 1.4 and this gain increases to 1.7 for the resonant cell with secondary leakage inductance.

In conclusion, the resonant parameters dimensioning should consider the secondary leakage inductance into consideration for a more precise component dimensioning and gain prediction, especially for high-current low-output voltage conditions, where the secondary leakage inductance may change greatly the *LLC*'s characteristics.

IV. System Design and Improvement

A. Design of the Inserted Molded Lead-Frame (IML) Power Module

One challenge of this project is how to handle significant power loss caused by high output current circulating at LV MOSFETs. Standard discrete MOSFETs components are difficult to use here due to limited thermal conductivity and packaging interconnection resistance. More discrete MOSFETs should be paralleled in order to overcome this problem and this increases the overall number of semiconductor devices and increases the overall volume. In this case, an interesting solution is to use a dedicated power module integrating all the LV MOSFETs [20].

In this project, an IML power module is designed, as shown in Fig. 9. Metal lead-frames are inserted into a plastic molding, which present horizontal open areas, where the MOSFETs dies are placed and brazed on. Not only holding the bare dies, the lead-frame also spreads to the outside, forming out electrical connection terminals. To adapt to the proposed double-phase

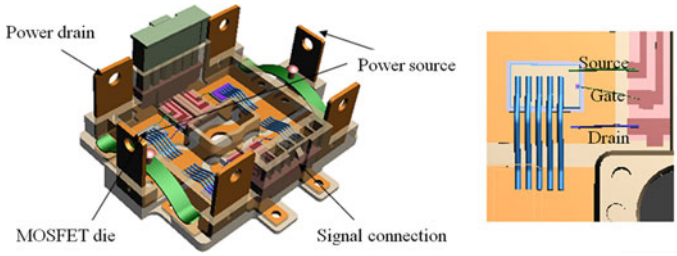

Fig. 9. Integration of the four LV MOSFET dies in the IML power module (3-D model).

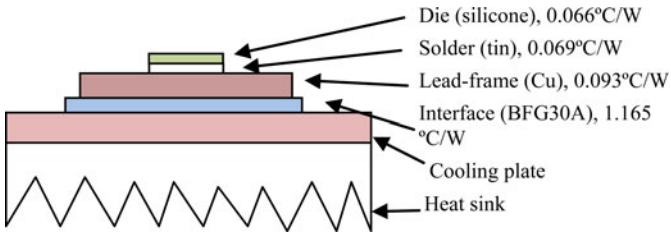

Fig. 10. Thermal resistances of the IML power module.

LLC topology, the designed power module consists of four dies arranged in a double-phase configuration. For each MOSFET die, the die's drain is soldered to the metal lead-frame and all the four dies share the same source connections. The power module itself is fixed to the cooling plate by screws and turnbuckles. The lead-frame is made up from copper of 0.8-mm thickness for high electrical and thermal conductivity. The adopted bare die is Infenion IIPC22S4N06, with an internal resistance $R_{\text{dson}} = 1.3$ mΩ, a gate charge of $Q_g = 208$ nC and a breakdown voltage of $V_{\text{DSS}} = 60$ V. The total resistance including metal lead-frame is less than 2 mΩ.

The main advantage of adopting the IML power module is that the heat dissipation of MOSFETs dies is greatly facilitated through the metal lead-frame. A thermal interface (BFG30A, $c = 5$ W/mK, 300 μm) should be inserted below the power module to ensure an electrical insulation between lead-frame and cooling plate. The thermal characteristics of designed module are shown in Fig. 10.

The total thermal resistance from the MOSFET die to the cooling plate is $R_{\text{th}} = 1.4$ °C/W. As the power loss is 15 W for each MOSFET, a temperature difference of about 20 °C is expected between the cooling plate and the MOSFET dies. The IML power modules have significant advantages in thermal performances over discrete FET components. Fewer components, simpler assembly, and good current carrying capability can be obtained with the proposed IML power module technology.

B. Transformer Design

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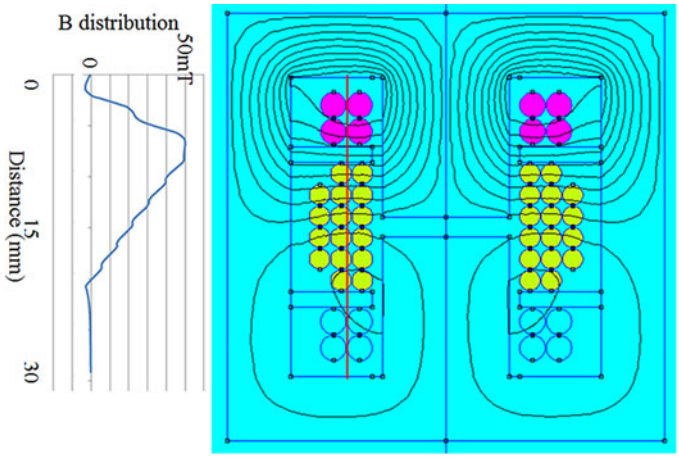

Fig. 11. Leakage induction distribution for the proposed transformer structure, $l_f = 1.5\ \mu$H.

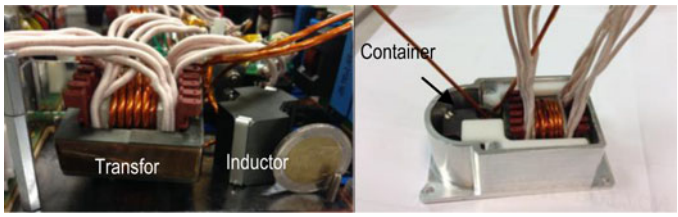

Fig. 12. Transformer structure with additional resonant inductor RM12 without cooling container (left) and in a cooling container (right).

The targeted magnetizing inductance of the *LLC*'s transformer is $L_m = 42\ \mu$H. To create the required magnetizing inductance is not a problem, with 16 turns at the transformer's primary side, magnetic cores with a low inductance factor $A_L \approx 165$ nH should be selected. Higher leakage inductance is possible to be realized by separating the secondary windings from the primary windings. The adopted winding solution is by winding the 16 turns of primary winding at the center and secondary winding at two extremities, as shown in Fig. 11.

As shown in Fig. 11, higher flux density is detected at the insulation layer, $B_{\rm pk} \approx 50$ mT. With a large interspace between primary and secondary side, this transformer performs a high leakage inductance of $l_f = 1.5\ \mu$H. The remaining resonant inductor shall be completed by an additional RM12 core, with six turns. A photo of transformer prototype is shown in Fig. 12.

The transformer design details are summarized in Table I.

Litz wire is here used to avoid skin effect and reduce proximity effect of windings in transformer construction. As insulators are inserted among different strands, Litz wire then has a poor thermal conductivity compared to pure copper wire. If not properly designed, heat produced by Litz wire will be difficult to be dissipated and the wire strands may be melted. Therefore, the power losses of Litz wire should be precisely estimated and controlled.

In Litz wire, the diameter of each strand should be less than the skin depth defined in the following equation:

$$\sigma = \sqrt{2\rho/\omega\mu}. \tag{7}$$

TABLE I
TRANSFORMER DESIGN SUMMARY

Description	Types	Values
Transformer Magnetic core	Core type	E42/21/15-3C97
	Inductance factor ($A_{\rm L}$)	170 nH
	Effective area (Ae)	1.78 cm^2
	Volume (V)	17.3 cm^3
	Air-gap length (e)	2 mm
	Magnetic inductance ($L_{\rm m}$)	42 μH
	Leakage inductance ($l_{\rm f}$)	1.5 μH
	Peak induction ($B_{\rm pk}$)	160 mT
Transformer Wire	Primary turns (N_1)	16
	Primary wire size	Round Litz 800 strands of 44AWG, Kapton insulated
	Secondary turns (N_2)	1
	Secondary wire size	Round Litz 1200 strands of 44AWG, 4 in parallel
	Fill factor	80%
	Primary AC resistance (Rac_p)	25 mΩ
	Secondary AC resistance(Rac_s, including external connections)	1.5 mΩ

Under this condition, the current distribution is expected to be homogenous. However, considerably high loss can still be generated due to proximity effect. It may still further be divided into internal proximity effect and external proximity effect. Internal proximity effect is the current distribution effect affected by the adjacent strands and windings. Lee *et al.* [19] proposed an equation to calculate the ac resistance caused by internal proximity effect based on the further development of the Dowell function. The proposed equation is possible to predict the ac resistance of transformer winding composed by Litz wire under no external field. When Litz wire is exposed to an external magnetic field generated by transformer's air gap, fringing flux penetrates into the Litz wire and the equation described in [21] is no further applicable.

In order to analyze the eddy current loss when wire is exposed to an external flux $B_{\rm pk}$, an equation is proposed to approximate the loss where conductor's diameter is smaller than skin depth [22]–[24]

$$P = \frac{\pi\omega^2 l B_{\rm pk}^2 d^4}{128\rho} \tag{8}$$

where ρ is the resistivity of the conductor, d is the strand diameter, l is the length of the conductor, and $B_{\rm pk}$ is the peak external magnetic field perpendicular to the axis of the wire at a radian frequency ω. One turn of Litz wire with N strands exposed under a certain magnetic field can then be approximated as follows:

$$P = \frac{N\pi\omega^2 l B_{\rm pk}^2 d^4}{128\rho}. \tag{9}$$

In order to further explore the relationship of eddy current loss and strand's diameter, (9) can further be written as

$$P = \frac{4\omega^2 l B_{\rm pk}^2 d^2 S}{128\rho} \tag{10}$$

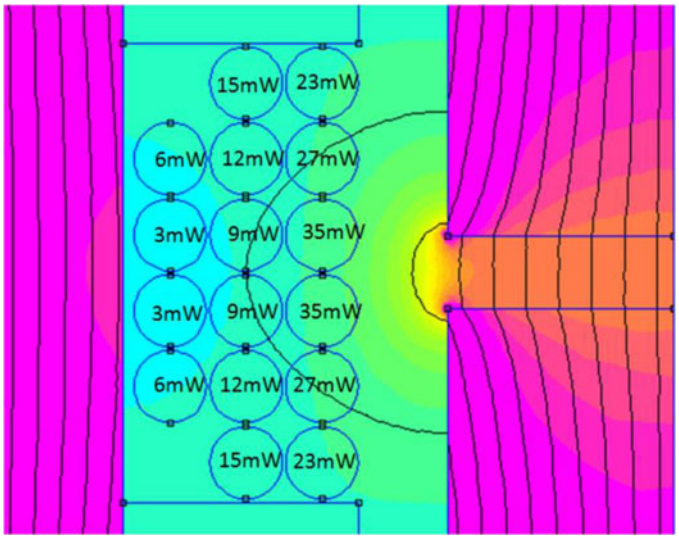

Fig. 13. Proposal of shifting the primary winding to get a reduced proximity effect (Peddy = 1.5 W).

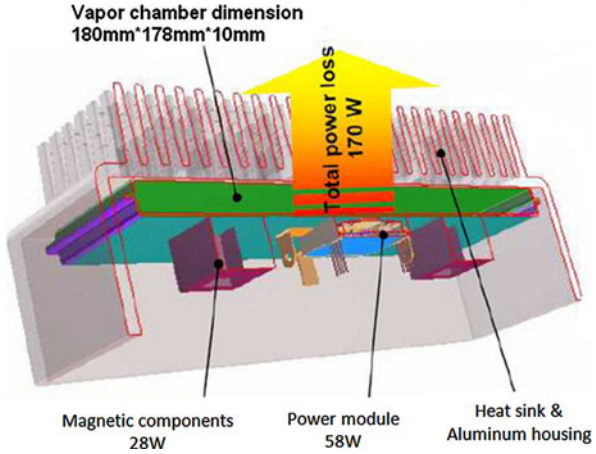

Fig. 14. Insertion of a vapor chamber into the base of the heat sink for efficient cooling.

where S is the total effective conductive section of Litz wire, $S = N\pi d^2/4$. From (10), it is obvious that under the same total effective conductive section, decreasing the strand diameter greatly reduces the eddy current loss in a Litz wire. To obtain a low eddy current loss, choosing a large number of fine strands and decreasing the strand's diameter is an effective solution. However, as the number of strands increases, the fraction of the window area filled with insulator increases and these results in an increase in dc resistance. Furthermore, finer strands are more expensive and difficult to precisely control its configuration. Thus, the strand diameter should be carefully selected and verified for efficiency, feasibility, and cost compromise. In this project, we select Litz wire 800∗44AWG with $d = 50$ μm ($\sim \sigma/3$).

In order to estimate the eddy current loss of the proposed transformer, it is possible to obtain simulation results from FEMM software. As the primary windings close to air gap are penetrated by fringing flux, the adopted solution to reduce the eddy current loss is to increase the thickness of coil-formers and keep the windings away from air gap, as shown in Fig. 13.

Keeping the windings away from the air gap, all the primary turns see a reduced magnetic field induction and the proximity effect can be reduced. By increasing the coil former's thickness from 1 to 2.5 mm, the obtained eddy current loss is decreased from 3.5 to 1.5 W.

C. Air-Cooling System and Prototype Assembly

One challenge of the actual designed *LLC* resonant converter is the ability to implement an innovative cooling solution. As for air-cooling solution, standard aluminum extrusions no longer have the capacity to sufficiently spread the power losses generated by electronic components and hot points exist. The cooling solution adopted here is by inserting a vapor chamber into the base of the heat sink, as shown in Fig. 14.

Vapor chambers are flat heat pipes that use the principles of evaporation and condensation to produce a heat spreading device with a very high conductivity thermal plane [25]. Like traditional cylindrical heat pipes, heat is evacuated using the working fluid, assuring a uniform temperature distribution and an elimination of hot spots [26]. Furthermore, the capillary action enables the vapor chamber to work in any orientation effectively with respect to gravity. Physically, the vapor chamber enables to better distribute the heat among its total surface.

Fig. 15 shows the components integration within the prototype. As the input filter PCB's power loss is rather limited, it is mounted vertically to reduce the overall volume. HV MOSFETs are placed at the bottom of the input filter PCB, and they are mounted directly to the vapor chamber and fixed by screws to improve the cooling effect. Magnetic components, LV MOSFETs modules, are mounted also on the vapor chamber directly. The control PCB board is mounted on the four spacers, above the power components. An external connection with 16 lines is used for exchanging control signals and export measurement results. After assembly, the prototype performs an overall volume of 2.5 L, 3 kg, and 2.5 kW nominal power (3-kW peak power). The power density is 1 W/cm^3.

V. Experimental Results

A. Operation and Efficiency Measurement

The following figures show the experimental results of the prototype at primary sides and secondary sides.

As the adopted HV superjunction MOSFET (STW88N65M5) performs high nonlinear output capacitor characteristics ($C_{\rm oss}$ is very high, at low $V_{\rm ds}$ voltage), the drain–source voltage is held on at the beginning of ZVS for about 150 ns, this permits the MOSFET to exhibit ZVS switch-off, shown as in Fig. 16. Then, the voltage decreases linearly to zero during the dead time before the other MOSFET switches ON; thus, the ZVS switch-on is also obtained. The finally adopted dead time is 400 ns. Secondary sides are implemented with synchronous rectifications, while the secondary conduction loss is greatly reduced. As reported in

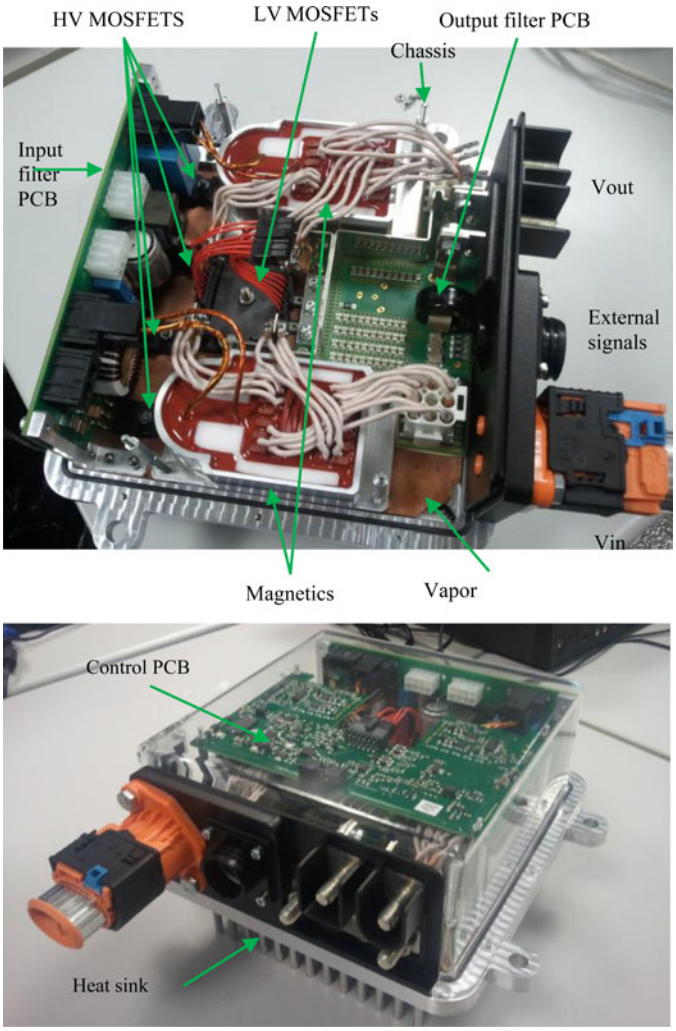

Fig. 15. Prototype assembly of the *LLC* converter, power density 1 W/cm3.

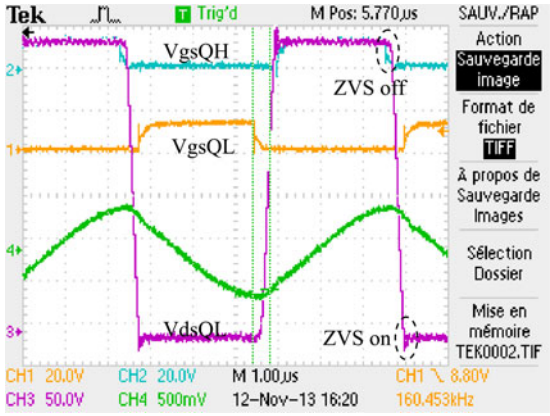

Fig. 16. Key operational waveforms of primary ZVS waveform for phase B, at $I_o = 150$ A. (I_r: 10 A/div).

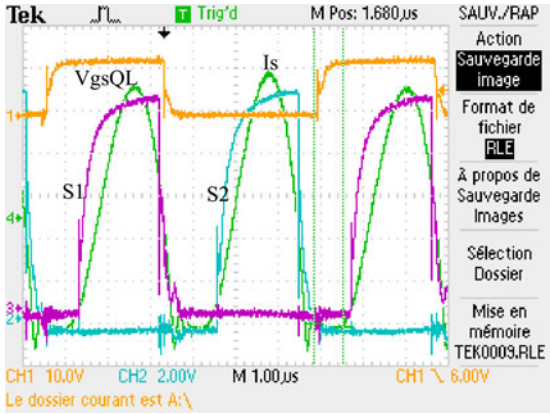

Fig. 17. Key operational waveforms of synchronous rectification for phase B, at $I_o = 150$ A. (I_s: 20 A/div).

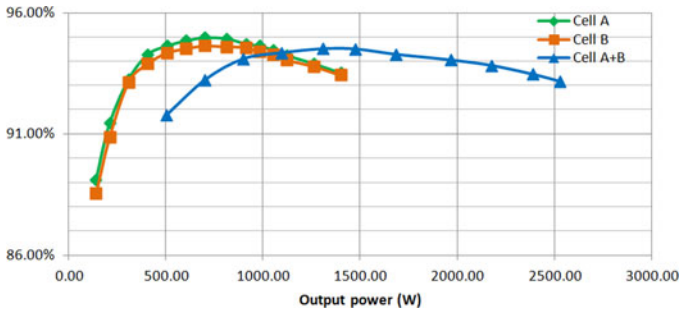

Fig. 18. Measured efficiency result for $V_{\text{in}} = 330$ V at different output currents.

Fig. 17, the synchronous rectification signal is in phase with the output current and a slightly phase lost is detected (synchronous rectification ends with 400 ns earlier than current falls to zero). A diode conduction loss is expected, but this conduction loss is rather limited by its conduction time. In addition, the reverse recovery current (∼10 A) causes an extra power loss of about 1.5 W per FET.

Efficiency has been measured for the power cell A, power cell B, and for the two power cells operating in parallel together, as shown in Fig. 18.

The conversion efficiency of a single cell *LLC* converter is maximal at 700 W, with a peak efficiency of 95% for phase A and 94.7% for phase B. Efficiency begins to decrease when load power exceeds 700 W. Setting $P = 1.1$ kW as the boundary for single-cell operation and double-cell operation is a good choice to keep a high efficiency over a high output power range. When output current exceeds 1.1 kW, both the two cells operate and efficiency continues to increase from 1.1 to 1.5 kW.

In all, the designed double-phase *LLC* converter exhibits very good conversion efficiency at a large load variation range: Efficiency $> 94\%$ from 500 W to 2 kW; Efficiency$> 93\%$ from 300 W to 2.5 kW. Even at very low load (140 W), the conversion efficiency is around 89%. The loss breakdown of the developed *LLC* resonant converter is shown in the Table II. The calculations are in good agreement with the experimental results.

TABLE II
CALCULATED LOSS BREAKDOWN OF THE DESIGNED *LLC* CONVERTER AT 2.5 KW, $V_{\rm in} = 330$ V (DOUBLE-CELL OPERATION)

Description	Types	Values
Primary MOSFET	Conduction loss	3.43 W
	Gate loss	0.60 W
	Switching loss	~0 W
	Total loss (x4)	16.12 W
Secondary MOSFET	Driving loss	0.72 W
	FET Conduction loss	9.8 W
	Diode conduction loss	3.4 W
	Reverse recovery loss	1.5 W
	Total loss (x4)	61.68 W
Inductor	Core loss	1.85 W
	Copper loss	1.96 W
	Total Loss (x2)	7.62 W
Transformer	Primary copper loss Primary Eddy current loss	3.92 W 1.5 W
	Secondary copper loss	14.7 W
	Total copper loss	20.12 W
	Core loss	8.4 W
	Total loss (x2)	56.24 W
Input filter	Conduction loss	2.20 W
Output filter	Conduction loss	4.20 W
Snubber	Conduction loss	8.00 W
RS filter	Conduction loss	5.33 W
fuse	Conduction loss	10 W
Total	Total Loss	171.39 W
Efficiency(driver included)		93.5%
Efficiency		93.7%

B. Conducted EMC Measurement

Fig. 19 reports the measured EMC results at HV side.

As reported in Fig. 19, all the noises are kept under the specified limits of car makers. The main switching noise is detected at 2k $f_{\rm s}$ frequencies (In *LLC* the input or output noise is twice the switching frequency). Transformer secondary asymmetries cause additional noises at $(2k-1)f_{\rm s}$ frequencies. Particularly for $f_{\rm s}$, the generated noise level is far less than that at $2f_{\rm s}$, but as the designed filters' attenuation at fs is 15 dB less than $2f_{\rm s}$, the noise at $f_{\rm s}$ becomes significant in front of $2f_{\rm s}$ (72 versus 78 dBμV). The asymmetries of transformer secondary windings should be precisely controlled in order to minimize this noise.

For the fundamental and the first harmonic frequency, it is not able to distinguish the difference of f_a and f_b, due to the measurement resolution. Starting from the $5f_{\rm s}$, the differences of two adjacent frequencies become apparent. The noises levels at adjacent frequencies are equal, verifying that the noise is superposed in frequency domain. One can design the input/output filters based on the conducted noise levels of one phase, the other phase benefits naturally the same attenuation at the adjacent frequency.

In the designed converter, the interaction between the switching noises of each resonant cell creates the undesired beat frequencies, at multiples of the differences between their operating frequencies [27], [28]. Low frequency (LF) component at $2(f_b - f_a)$ appears at both the input and output sides. As the two frequencies are close to each other, this LF beating noise may not be sufficiently attenuated by the input or output LP filter.

To damp this LF beating, sufficient bypass capacitors are necessary at the input of each power cell to reduce the voltage level of $v_{\rm a}$. Furthermore, input and output filters should not contain any resonant points at LF range; if not, this ripple may be amplified by the filters and is harmful to the stable operation of the *LLC* resonant converter. Thus, the filter's gain should be precisely designed and controlled. The measured input beating at this converter prototype is shown in Fig. 20.

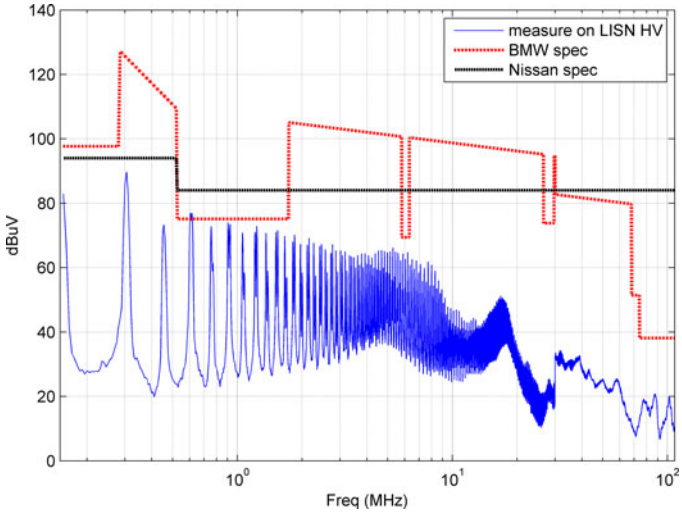

Fig. 19. EMC-conducted emission measurement at LISN HV+ (AVG detector, $V_{\rm in} = 330$ V.

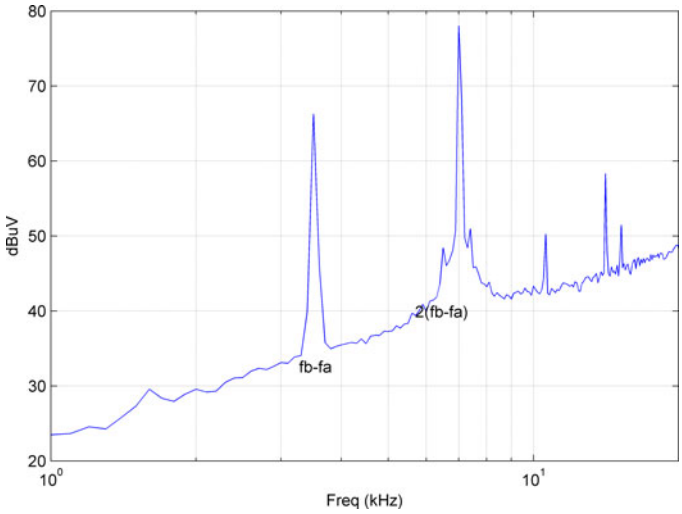

Fig. 20. EMC measurement for LF at LISN LV+ (AVG detector, $V_{\rm in} = 410$ V).

The main beat frequency $2(f_b - f_a)$ is measured at 78 dBμV and another beat frequency $(f_b - f_a)$ at 65 dBμV appears due to transformer asymmetries. As the beating noise is kept less than the main switching noise, it will not influence the correct circuit converter operation behavior.

VI. CONCLUSION

The proposed double-phase parallel arrangement to handle 180-A output current is able to keep a high efficiency at a wide load range. High efficiency at light load is assured by switching

OFF one power cell. In order to avoid the current dissymmetry problems in parallel interleaving *LLC*, the proposed double-loop control strategy can equalize the current distribution between two power cells. This paper also proposes many new implementations for improving the performance of *LLC* converter. Transformer with *E* structure integrating magnetizing inductor and partial resonant inductor is verified to be a good solution to get a compact magnetic integration. The Litz wire is a good solution implemented to reduce eddy current loss, but its strand diameter should be carefully selected and should be kept away from the air gap. The LV MOSFETs in the IML module proved its effectiveness in reducing thermal resistances and it is a good solution to handle high output current conduction loss. The air-cooling system with vapor chamber as heat spreader is effective in rapid and homogenous heat spreading.

The double-cell *LLC* with equal current distribution has two operational frequencies close to each other. The dimensioning of input/output filter can be simplified by considering the noises of only one phase; the other cell at adjacent frequency beneficed the same damping naturally. LF beatings should be filtered by bypass capacitors close to each power cell.

In conclusion, the proposed double-phase *LLC* converter is an ideal solution for building 2.5-kW dc/dc HV/LV power converters for future electric vehicles.

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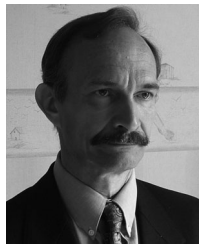

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