Discontinuous SVPWM Techniques of Three-Leg VSI-Fed Balanced Two-Phase Loads for Reduced Switching Losses and Current Ripple

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***Abstract*—In this paper, various types of discontinuous space vector pulse-width modulation techniques for a three-leg voltage source inverter supplying balanced two-phase loads are proposed. The main objectives of the paper are to analyze switching loss characteristics associated with semiconductor devices and to reduce output current ripple by dealing with various types of zero space vector time in each switching sequence. Capabilities of reductions in switching losses and current ripple for both balanced and unbalanced output phase voltages at high modulation index and load power factor angle of 30° lagging are focused. The validity of the proposed techniques is verified by simulation and experimental results in terms of voltage spectrum, current waveforms, reductions in switching losses, and output current ripple at high modulation index when compared to a continuous space vector pulse-width modulation technique.**

***Index Terms*—Current ripple, discontinuous space vector pulse-width modulation (SVPWM), switching losses, three-leg voltage source inverter (VSI), two-phase loads.**

I. Introduction

PRESENTLY, voltage source inverters (VSIs) serve as variable speed drives, active power filter, uninterruptible power supplies, etc. Better performances of VSIs such as efficiency and output current ripple can be improved with pulse-width modulation (PWM) schemes. Space vector PWM (SVPWM) is very popular for VSIs due to better characteristics such as wider linear modulation range, less total harmonic distortion, and easier implementation. Means of a reduction in power losses with discontinuous space vector pulse-width modulation (DSVPWM) caused by semiconductors can be found in [1] and [2]. In order to improve the performance of a three-phase three-leg VSI in terms of reductions in switching losses and current ripple, previous works proposed discontinuous modulation which provided PWM patterns allowing one switching device for each phase-leg without switching in a certain interval when compared to continuous modulation. The requirement of such interval or clapping time is dependent on power factor of the load connected to the inverter output. Several papers proposed various types of DSVPWM such as 120° clamping classified as DPWMMIN and DPWMMAX, 60° clamp classified as DPWM 1, DPWM 2, and DPWM 0 [2]–[5] which suits to a reduction in switching losses for unity, lagging and leading power factor, respectively. These techniques offer switching losses and output current ripple in higher modulation index when compared to the continuous space vector pulse-width modulation (CSVPWM) technique. Applications of the DSVPWM strategy in three-phase induction motor drives at full load to reduce torque ripple can be found in [6]–[8]. In addition, a discontinuous modulation technique of three-phase inverters was developed towards advanced bus clamping PWM techniques and hybrid PWM techniques in order to reduce switching losses and output current ripple [9]–[12].

Generally, for industrial applications, two-phase loads are symmetrical and asymmetrical parameter type two-phase induction motors which can be supplied with two-leg, three-leg, and four-leg VSIs [13]. A discontinuous PWM technique for a symmetrical parameter type two-phase induction motor drive with a three-leg VSI can be implemented in the same manner as for a three-phase induction motor drive proposed in [13]. The objectives of this technique are to increase efficiency and performance of the motor drive. For asymmetrical parameter two-phase induction motor drives with a three-leg VSI, the importance is the control of magnetomotive force (MMF) of both main and auxiliary windings to be of symmetry in order to eliminate backward torque by current control [14]. CSVPWM for analog and digital implementation for three-leg VSI-fed unbalanced two-phase induction motors can be found in [15]–[17]. With this method, output voltage can also be controlled so as to eliminate the asymmetry of MMF leading to performance improvement. There are a few publications analyzing switching loss characteristics and current ripple for three-leg VSI-fed two-phase loads with DSVPWM. Although DSVPWM techniques proposed by Tomaselli *et al.* [13] were implemented for symmetrical two-phase induction motor drives, various types of DSVPWM have not been fully studied yet. Therefore, this paper will present the principle in detail and analyze DSVPWM using a three-leg VSI for two-phase balanced RL loads. The proposed main power circuit is shown in Fig. 1. Each phase has 30° lagging load power factor. This paper focuses on the analysis of switching loss characteristics and output current ripple when compared to the conventional modulation by the alternative placement of zero space vectors of $\overline{SV_7}$ and $\overline{SV_0}$ for each sector. With the proposed DSVPWM, switching losses for

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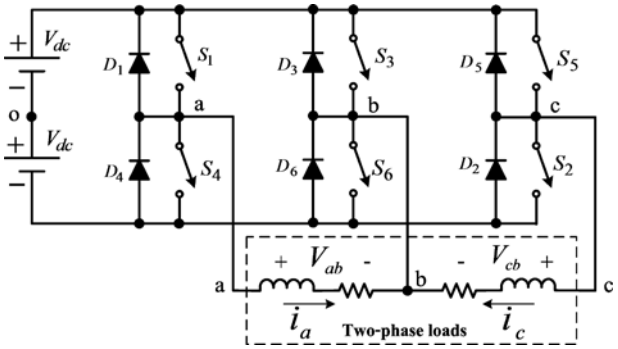

Fig. 1. Three-leg VSI supplying two-phase loads.

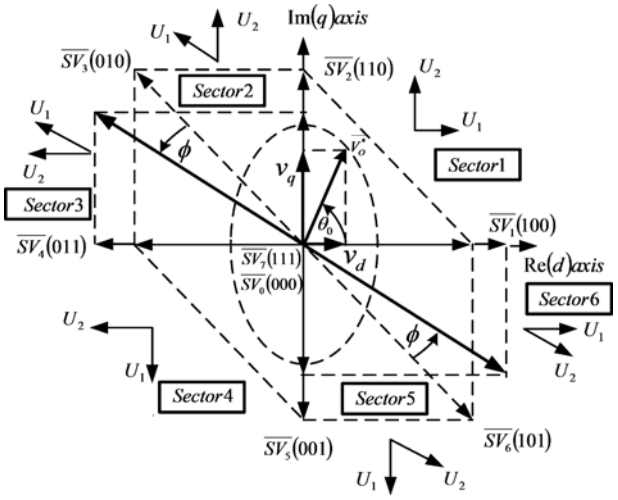

Fig. 2. Location of eight active space vectors and an arbitrary output desired voltage.

each leg are almost equal under balanced and unbalanced output phase voltage conditions. The advantage of having symmetrical (or equal) switching losses in each leg of the VSI is the junction temperature balance for each device. Note that high junction temperature results in degradation of electrical characteristics of switching devices.

The proposed technique is implemented on TMS320F28335 EZDSP [18] for generating PWM gating signals of the switching devices in the main power circuit. The simulation and experimental results are given under testing conditions of switching losses and output current ripple to verify the correctness of the proposed principle.

II. Review of Conventional Unbalanced SVPWM

Before deriving modulating functions of the proposed DSVPWM for the two-phase three-leg VSI, the review of CSVPWM is given. The principle of carrier-based unbalanced two-phase SVPWM applied to a three-leg VSI is modified from that of the conventional balanced two-phase SVPWM [16], [17]. The differences between balanced and unbalanced phase voltages of the two-phase three-leg VSI are the magnitude and the location of the basic space vectors. The desired output voltage (V_o^*) and space vector plane can be displayed in Fig. 2. Unlike

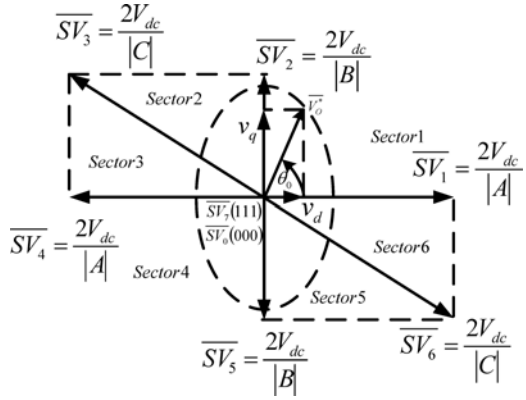

Fig. 3. Relationship between active space vectors and voltage factors $|A|$, $|B|$, and $|C|$.

the desired balanced output voltage yielding a circular trajectory, the desired unbalanced output voltage gives an elliptical trajectory as the dotted line. Due to the similar principle to the conventional balanced SVPWM, mathematical calculation of switching times for the proposed method can be dealt with in the same manner as for the conventional one [17].

The desired output voltage in vector form which is a rotating vector can be calculated in terms of the average of a number of these space vectors within a switching period in each sector as

$$\overline{V_0^*} = V_0 \angle \theta_0 = \frac{t_1}{\Delta T/2}\overline{U_1} + \frac{t_2}{\Delta T/2}\overline{U_2} \tag{1}$$

where

$$\overline{U_1} = V_1 \mathrm{e}^{j\alpha_1} \tag{2}$$

$$\overline{U_2} = V_2 \mathrm{e}^{j\alpha_2} \tag{3}$$

and

$$\frac{\Delta T}{2} = t_1 + t_2 + t_0 + t_7. \tag{4}$$

Note that the sum of active times in each sector is less than the half carrier period (i.e., $t_1 + t_2 \leq {}^{\Delta T}/_2$).

$\overline{U_1}$ and $\overline{U_2}$ are two basic adjacent vectors; V_1 and V_2 are magnitudes of the two basic adjacent space vectors; θ_0 is sampled angular position; α_1 and α_2 are angles for the two basic adjacent vectors; t_1 and t_2 are active times for the two basic adjacent vectors; t_0 and t_7 are times for null vectors; and ΔT is a carrier period. Generally, for a symmetrical space vector pattern, space vector time for each zero switching state (t_0 and t_7) is set to be equal. The magnitude of the proposed space vectors is obtained by scaling the magnitude of the conventional ones by voltage factors $|A|$, $|B|$, and $|C|$, as shown in Fig. 3. Voltage factors can be determined based on the principle of trigonometry which can adjust the magnitude of the output voltage reference (V_o^*) by adjusting unbalanced voltage degree (δ). For balanced two-phase voltages case, the value of δ is equal to zero. As a result, $|A|$ and $|B|$ is equal to 1 and $|C|$ is equal to 0.707. For unbalanced two-phase voltages, case δ can be adjusted as positive or negative. Calculated results of voltage factors $|A|$, $|B|$, and $|C|$ can be found in [17].

TABLE I
DISCONTINUOUS PWMMIN TYPE 1

	Angular position	Phase-leg reference voltages
Sector 1	$0 < \theta_0 < \frac{\pi}{2}$	$\frac{v_{ao}}{V_{\rm dc}} = M\,\lvert A\rvert \sin\left(\frac{\pi}{2} - \theta_0\right) + M\,\lvert B\rvert \sin(\theta_0) - 1$
		$\frac{v_{bo}}{V_{\rm dc}} = M\,\lvert B\rvert \sin(\theta_0) - 1$
		$\frac{v_{co}}{V_{\rm dc}} = -1$
Sector 2	$\frac{\pi}{2} < \theta_0 < \frac{3\pi}{4} + \phi$	$\frac{v_{ao}}{V_{\rm dc}} = \frac{M\,\lvert B\rvert \sin\left(3\pi/4 + \phi - \theta_0\right)}{\sin\left(\pi/4 + \phi\right)} - 1$
		$\frac{v_{bo}}{V_{\rm dc}} = \frac{M\,\lvert C\rvert \sin\left(\theta_0 - \pi/2\right)}{\sin\left(\pi/4 + \phi\right)} + \frac{M\,\lvert B\rvert \sin\left(3\pi/4 + \phi - \theta_0\right)}{\sin\left(\pi/4 + \phi\right)} - 1$
		$\frac{v_{co}}{V_{\rm dc}} = -1$
Sector 3	$\frac{3\pi}{4} + \phi < \theta_0 < \pi$	$\frac{v_{ao}}{V_{\rm dc}} = -1$
		$\frac{v_{bo}}{V_{\rm dc}} = \frac{M\,\lvert C\rvert \sin(\pi - \theta_0)}{\sin\left(\pi/4 - \phi\right)} + \frac{M\,\lvert A\rvert \sin\left(\theta_0 - 3\pi/4 - \phi\right)}{\sin\left(\pi/4 - \phi\right)} - 1$
		$\frac{v_{co}}{V_{\rm dc}} = \frac{M\,\lvert A\rvert \sin\left(\theta_0 - 3\pi/4 - \phi\right)}{\sin\left(\pi/4 - \phi\right)} - 1$

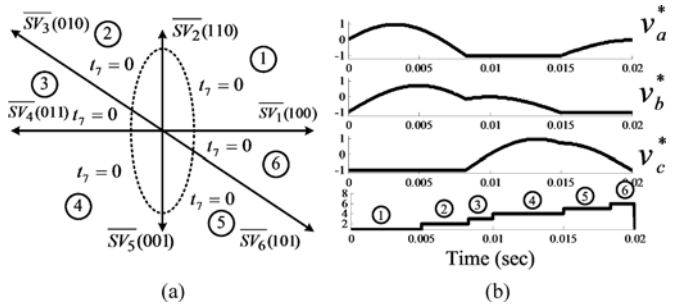

Fig. 4. Discontinuous PWMMIN type 1 (a) location of active space vectors and placement of zero space vector time and (b) phase-leg reference voltage waveforms in each sector.

For example, space vector active times t_1 and t_2 for sector 1 are

$$t_1 = \frac{M\,|A|}{2} \sin\left(\pi/2 - \theta_0\right) \Delta T/2 \tag{5}$$

$$t_2 = \frac{M\,|B|}{2} \sin\left(\theta_0\right) \Delta T/2 \tag{6}$$

where $M = \frac{V_o}{V_{\rm dc}}$ is the modulation index, and $0 \le M \le \sqrt{2}$.

The magnitudes of the orthogonal output voltages for the unbalanced two-phase system can be expressed as

$$V_{ab} = MV_{\rm dc}\sqrt{2}\sin\left(\frac{\pi/2 - \delta}{2}\right) \text{(using peak voltage)} \tag{7}$$

$$V_{cb} = MV_{\rm dc}\sqrt{2}\cos\left(\frac{\pi/2 - \delta}{2}\right) \text{(using peak voltage)}. \tag{8}$$

From (7) and (8), output voltages can be adjusted by changing values of the modulation index and δ which depend on the voltage factors. Therefore, desired unbalanced output voltages are achieved by changing such parameters. This will benefit an asymmetrical parameter type two-phase induction machine for improving the performance [16].

III. PROPOSED DSVPWM STRATEGY

This section describes the proposed DSVPWM. The purposes of this strategy are to reduce the switching losses and the output current ripple. Basically, DSVPWM for a three-phase system occurs when zero space voltage vectors either $\overline{SV_0}$ (000) or $\overline{SV_7}$ (111) is selected instead of both resulting in removal of zero voltage vector in successive half carrier intervals [1]–[5]. For example, for 120° discontinuous modulation, $\overline{SV_0}$ is only selected for all six sectors so-called DPWMMIN (clamp to lower dc bus) for one-third of the fundamental cycle. In the same manner, if only $\overline{SV_7}$ is selected, the zero space vector is continuously locked to the upper dc bus which is called as DPWMMAX [5]. As a result, a reduction in switching number can be achieved about one-third of total switching number over the fundamental cycle. Other types of discontinuous modulation such as 60° discontinuous modulation alternately place zero space vector voltage for successive 60° segments of the fundamental cycle in order to achieve symmetry of switching pattern. The position of the zero clamp is at positive and negative peaks of its fundamental reference voltage which is so-called DPWM 1 which is suitable for a resistive load [5]. Also, for 60° clamp, the nonswitching period occurs at peak zone of the load current with power factor of 0.866. The types of discontinuous modulation are called DPWM 2 and DPWM 0 for lagging pf of 0.866 and leading pf of 0.866, respectively. Both types give higher reduction of switching losses than DPWM 1. The proposed discontinuous modulation strategies for unbalanced two-phase output voltages using three-leg VSI are modified from three-phase balanced output voltages using the three-leg VSI. The calculation of space vector active times for continuous SVPWM modulation providing unbalanced two-phase output voltages has already been mentioned in [17]. For analysis of DPWMMIN, for

TABLE II
DISCONTINUOUS PWMMAX

	Angular position	Phase-leg reference voltages
Sector 1	$0 < \theta_0 < \frac{\pi}{2}$	$\frac{v_{ao}}{V_{\rm dc}} = +1$
		$\frac{v_{bo}}{V_{\rm dc}} = -M\,\lvert A\rvert \sin\left(\frac{\pi}{2} - \theta_0\right) + 1$
		$\frac{v_{co}}{V_{\rm dc}} = -M\,\lvert A\rvert \sin\left(\frac{\pi}{2} - \theta_0\right) - M\,\lvert B\rvert \sin(\theta_0) + 1$
Sector 2	$\frac{\pi}{2} < \theta_0 < \frac{3\pi}{4} + \phi$	$\frac{v_{ao}}{V_{\rm dc}} = \frac{-M\,\lvert C\rvert \sin\left(\theta_0 - \pi/2\right)}{\sin\left(\pi/4 + \phi\right)} + 1$
		$\frac{v_{bo}}{V_{\rm dc}} = +1$
		$\frac{v_{co}}{V_{\rm dc}} = \frac{-M\,\lvert C\rvert \sin\left(\theta_0 - \frac{\pi}{2}\right)}{\sin\left(\frac{\pi}{4} + \phi\right)} - \frac{M\,\lvert B\rvert \sin\left(3\pi/4 + \phi - \theta_0\right)}{\sin\left(\frac{\pi}{4} + \phi\right)} + 1$
Sector 3	$\frac{3\pi}{4} + \phi < \theta_0 < \pi$	$\frac{v_{ao}}{V_{\rm dc}} = \frac{-M\,\lvert C\rvert \sin(\pi - \theta_0)}{\sin\left(\pi/4 - \phi\right)} - \frac{M\,\lvert A\rvert \sin\left(\theta_0 - 3\pi/4 - \phi\right)}{\sin\left(\pi/4 - \phi\right)} + 1$
		$\frac{v_{bo}}{V_{\rm dc}} = +1$
		$\frac{v_{co}}{V_{\rm dc}} = \frac{-M\,\lvert C\rvert \sin(\pi - \theta_0)}{\sin\left(\pi/4 - \phi\right)} + 1$

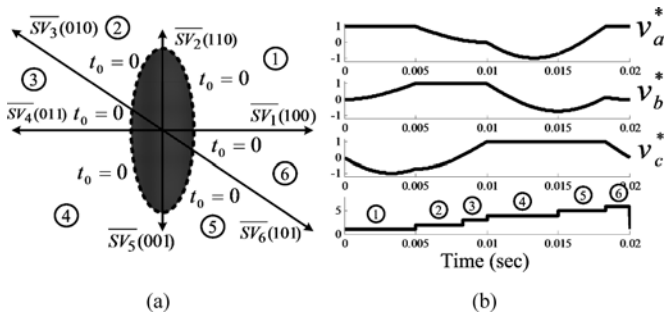

Fig. 5. Discontinuous PWMMAX (a) location of active space vectors and placement of zero space vector time and (b) phase-leg reference voltage waveforms in each sector.

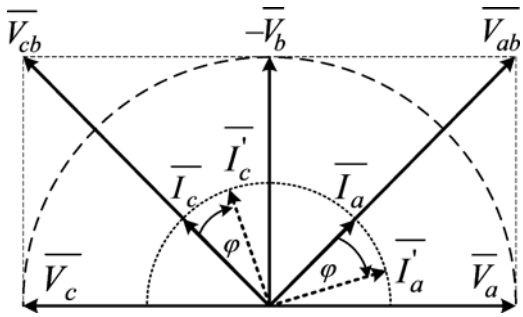

Fig. 6. Relationship of phasor diagram between two-phase voltages and output currents at load power factor with $\varphi = 30°$ lagging for balanced outputs.

unbalanced output voltages, only zero space vector voltage $\overline{SV_0}$ is selected. The zero space vector time t_0 is

$$t_0 = \frac{\Delta T}{2} - t_1 - t_2. \tag{9}$$

For example, phase-leg reference voltage of phase a in sector 1 is given by

$$v_{ao} = V_{\rm dc}\left[\frac{t_1}{\Delta T/2} + \frac{t_2}{\Delta T/2} - \frac{t_0}{\Delta T/2}\right]. \tag{10}$$

Substituting t_1, t_2, and t_0 from (5), (6), and (9) in (10) phase-leg "a" average voltage normalized with the midpoint of dc-link voltage is

$$\frac{v_{ao}}{V_{\rm dc}} = M\,\lvert A\rvert \sin\left(\frac{\pi}{2} - \theta_o\right) + M\,\lvert B\rvert \sin(\theta_o) - 1. \tag{11}$$

The equations of each normalized phase-leg reference voltage for three successive sectors are shown in Table I. Note that the remaining sectors can be derived in the same manner. Phase reference waveforms for DPWMMIN with unbalanced voltage angle (δ) of 30° are plotted as shown in Fig. 4.

For DPWMMAX, only $\overline{SV_7}$ is chosen, then zero voltage vector time (t_0) of $\overline{SV_0}$ is zero. Phase-leg reference voltage functions are illustrated in Table II. According to phase-leg reference voltage equations in Table II, when unbalanced voltage angle (δ) is zero or it is a balanced output voltage case, the output voltages of two-phases are equal by clamping to the positive dc bus in sectors 1 and 6 for phase-leg a. The clamping interval is 135° while phase-leg b is clamped in sectors 2 and 3 with interval of 90° and phase-leg c is clamped in sectors 4 and 5 with interval of 135°. For unbalanced phase voltages, the unbalanced voltage angle is adjusted greater than zero, resulting in change of interval for clamping to the positive dc bus as shown in Fig. 5. For example, as shown in Fig. 5(a), the unbalanced voltage angle is 30°. As a result, intervals for clamping of sectors 1 and 4 are constant and equal to 90°. Intervals for sectors 2 and 5 are longer, while those for sectors 3 and 6 are shorter compared with those for balanced case. As shown in Fig. 5(b), the reference voltages for each phase are plotted by using Table II.

Unlike DPWMMAX and DPWMMIN in a three-phase system with 120° discontinuous modulation, according to principles of the proposed modulation, the clamping intervals are asymmetrical. In order to improve the balanced switching losses, this paper proposes the alternate placement of zero space vectors of $\overline{SV_7}$ and $\overline{SV_0}$ for each sector. The assignment of the zero active space vector is mainly considered from output voltage and

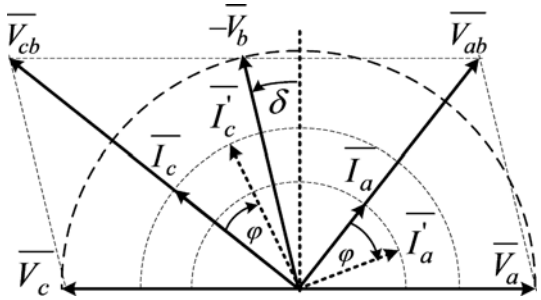

Fig. 7. Relationship of phasor diagram between two-phase voltages and output currents at load power factor with $\varphi = 30°$ lagging for unbalanced outputs.

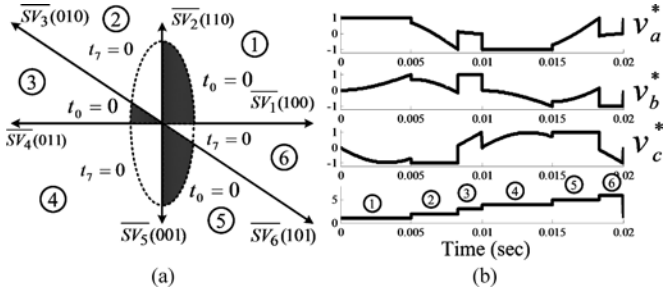

Fig. 9. DSVPWM type 2 (a) location of active space vectors and placement of zero space vector time and (b) phase-leg reference voltage waveforms in each sector.

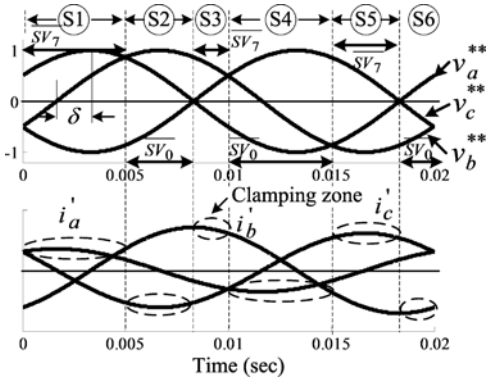

Fig. 8. Clamping zone at 30° lagging power factor angle for the unbalanced output voltage case (type 2).

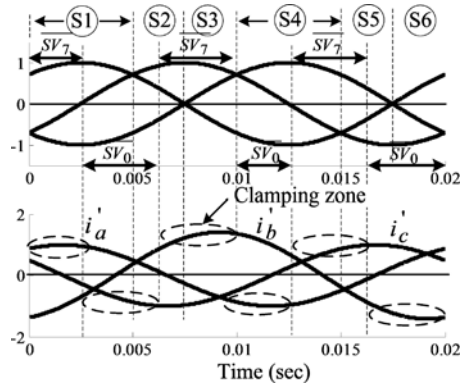

Fig. 10. Clamping zone at 30° lagging power factor for a balanced output voltage case ($\delta = 0°$).

current vectors. The 0.866 lagging load power factor is focused in accordance with Fig. 1.

According to the two-phase three-leg VSI, from Fig. 6 for balanced output voltages in case of the resistive load, phase a current (i_a) is in-phase with line voltage v_{ab} while phase c current (i_c) is in-phase with line voltage v_{cb} (i.e., phase-leg b is common). For the RL load, both currents lag these for the resistive load case with angle of φ as shown in Fig. 6. When power factor angle is 30°, both phase currents (i_a' and i_c') lag line voltages with 30° as shown in Figs. 6 and 7 for balanced and unbalanced voltage cases, respectively.

According to Figs. 6 and 7, voltage and current waveforms at the lagging power factor angle of 30° for balanced and unbalanced voltages can be plotted in Fig. 8. It is found that the clamping zone of peak values for positive and negative cycle of i_a' is at sectors 1 and 4, respectively. The clamping zone of peak values for positive and negative cycle of i_b' is at sectors 3 and 6, respectively. The clamping zone of peak values for positive and negative cycle of i_c' is at sectors 5 and 2, respectively. Therefore, 30° lagging clamp modulation is defined as type 2 as shown in Fig. 9. $\overline{SV_7}$ is only used for sector 1 and $\overline{SV_0}$ is only used for sector 2. The phase-leg reference voltages are calculated by using equations given in Table I and II.

From the analysis of DSVPWM type 2 as mentioned earlier, time intervals for each phase in clamping are unequal as shown in Figs. 8 and 9. Particularly, phase b gives the shortest time interval resulting in unequal switching losses. In order to balance

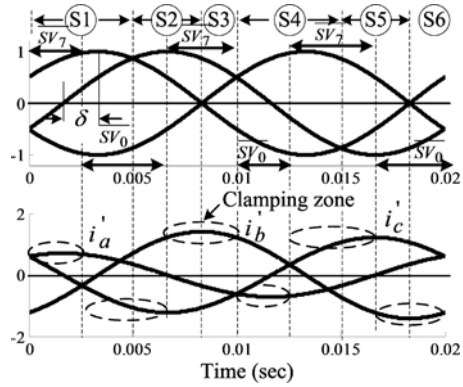

Fig. 11. Clamping zone at 30° lagging power factor for an unbalanced output voltage case ($\delta = 30°$).

the clamping interval and switching losses, improvement of DSVPWM by dividing the zone of clamping is proposed as shown in Figs. 10 and 11 for balanced and unbalanced voltage cases, respectively. It is found that sectors 1, 2, 4, and 5 are divided into two equal parts while sectors 3 and 6 are not divided. Sectors are divided into ten subzones as shown in Figs. 10 and 11. The clamping time intervals for δ of 0° and 30° are equal resulting in equal switching losses for each phase-leg. Fig. 12(a) and (b) illustrates vector placement in each sector in complex plane divided into ten subzones for balanced and

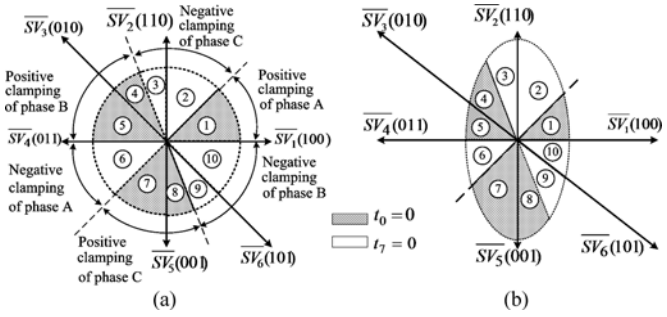

Fig. 12. Location of active space vectors and placement of zero space vector time for discontinuous SVPWM (type 3). (a) Balanced output voltages. (b) Unbalanced output voltages.

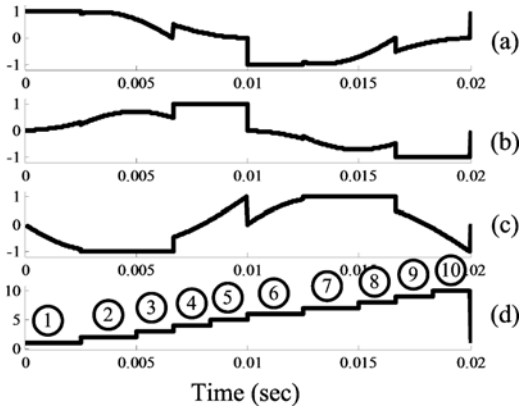

Fig. 13. Phase-leg reference voltage waveforms in each sector of discontinuous SVPWM (type 3). (a) Phase-leg a waveform. (b) Phase-leg b waveform. (c) Phase-leg c waveform. (d) Ten zone sectors.

unbalanced output phase voltages, respectively. From Fig. 12, modulating functions in sector 1 (Zone 1) are obtained from Table II calculating only t_7 which is the time of zero space vector $\overline{SV_7}$ while those in sector 1 (Zone 2) are obtained from sector 1 in Table I for only t_0 which is the time of zero space vector $\overline{SV_0}$. The plotted reference voltage waveforms for the three-leg VSI in a period of fundamental frequency are shown in Fig. 13. The DSVPWM with ten zone division is called type 3.

IV. Switching Loss Analysis and Current Ripple

A. Switching Loss Analysis

For this analysis, conduction loss is not included. There is an evidence about how conduction losses vary with modulation index and switching frequency [8]. Three types of modulation strategy (SPWM, SVPWM, and DPWM) were compared for conduction losses and switching losses with the variation of switching frequency and modulation index. It was found that at high modulation index and high switching frequency, the conduction losses for DPWM are slightly higher than those for other types. On the other hand, switching losses for DPWM are significant lower than those for other types. Therefore, the increase

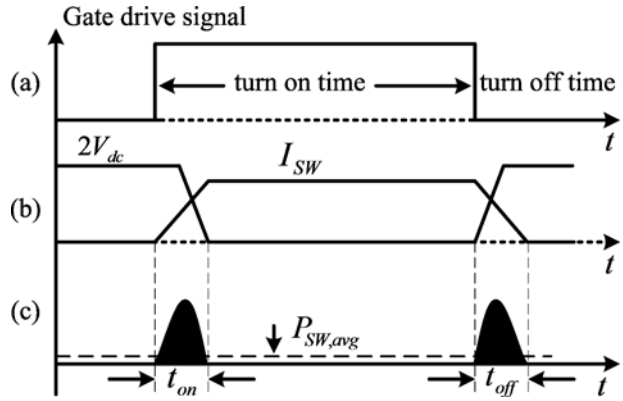

Fig. 14. Linearized switching characteristics (a) pulse switching pattern, (b) switching waveforms, and (c) instantaneous switching loss.

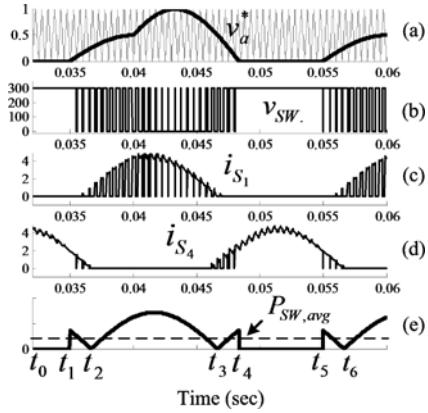

Fig. 15. Example of switching waveforms for DSVPWM type 1 in phase-leg a (a) modulating signal of phase-leg a, (b) voltage across switching device S_1, (c) current flowing through switching device S_1, (d) current flowing through switching device S_4, and (e) the solid line: average switching power loss in a switching period and the dotted line: average switch power loss of phase-leg a over a fundamental period.

of the conduction losses under the variation of modulation index and switching frequency is insignificant while the decrease of the switching losses is significant. As a consequence the conduction losses are neglected. Assume that the switching devices have linearity of voltage and current changes during the turn-on and turn-off process. Gate drive signal for turn-on and turn-off is shown in Fig. 14(a). Waveforms of current flowing in a switch and voltage across a switch are shown in Fig. 14(b). Fig. 14(c) shows switching power loss during turn-on and turn-off process and the average in a switching period [2], [8], [20].

From Fig. 14, during turn-ON ($t_{\rm ON}$) and turn-OFF ($t_{\rm OFF}$), switch current rises linearly and voltage across switch decreases linearly as a function of times. The switch voltage and current equations with a given input dc voltage and magnitude of the load current ($I_{\rm SW}$) are as follows:

$$i_{\rm SW}(t) = I_{\rm SW}\frac{t}{t_{\rm ON}} \tag{12}$$

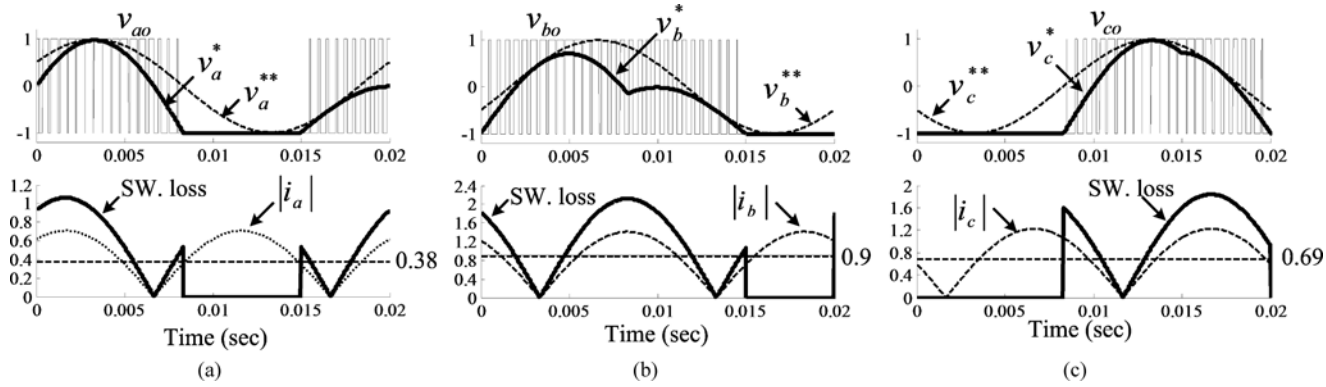

Fig. 16. Normalized switching losses of unbalanced output voltage of DSVPWM type 1.

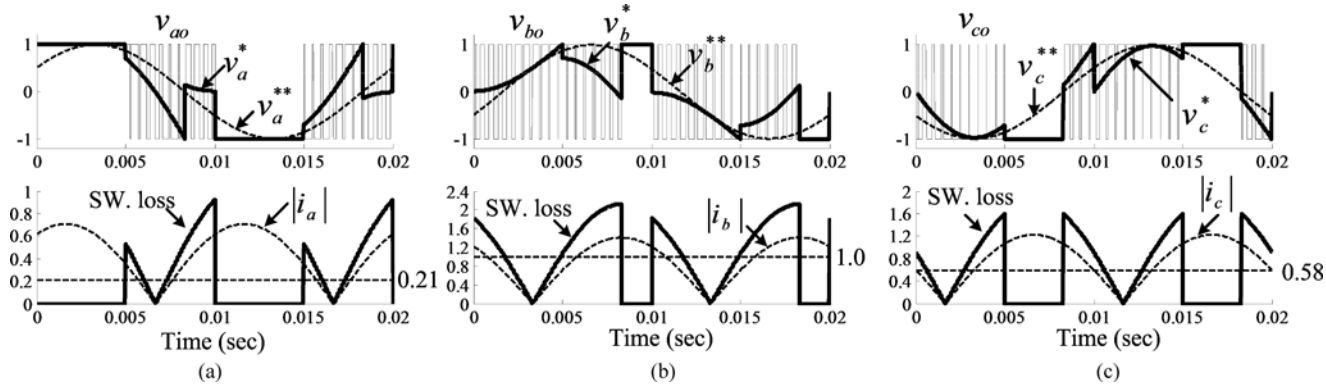

Fig. 17. Normalized switching losses of unbalanced output voltage of DSVPWM type 2.

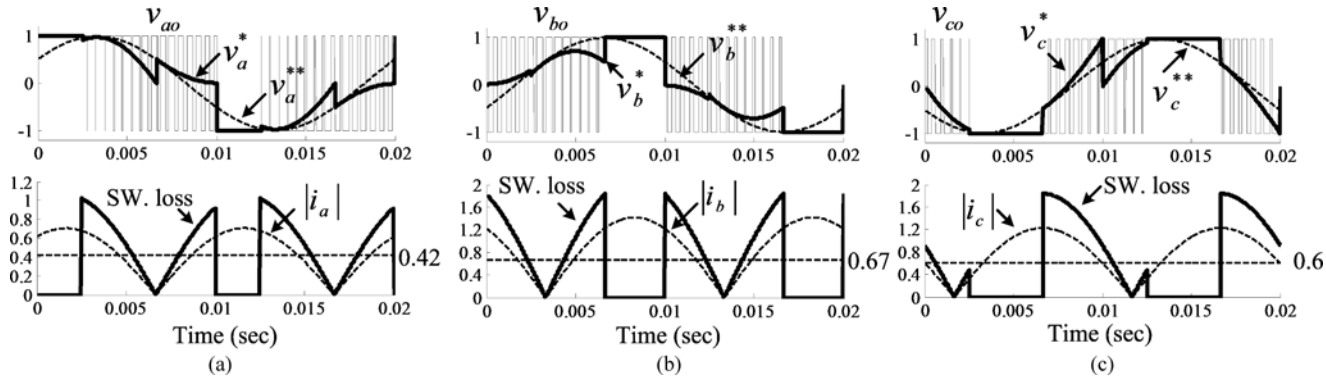

Fig. 18. Normalized switching losses of unbalanced output voltage of DSVPWM type 3.

and

$$v_{\mathrm{SW}}(t) = 2V_{\mathrm{dc}} - 2V_{\mathrm{dc}}\frac{t}{t_{\mathrm{ON}}} \tag{13}$$

where t_{ON} is turn-on time.

T_{SW} is a period of switching. Using (12) and (13), instantaneous switching power loss for a turn-on process is expressed as

$$P_{\mathrm{ON}}(t) = i_{\mathrm{SW}}\, v_{\mathrm{SW}} = \left(I_{\mathrm{SW}}\frac{t}{t_{\mathrm{ON}}}\right)\left(2V_{\mathrm{dc}} - 2V_{\mathrm{dc}}\frac{t}{t_{\mathrm{ON}}}\right). \tag{14}$$

The average switching power loss is

$$P_{\mathrm{ON,avg}} = \frac{1}{T_{\mathrm{SW}}}\int_0^{t_{\mathrm{ON}}} P_{\mathrm{ON}}(t)\mathrm{d}t = f_{\mathrm{SW}} I_{\mathrm{SW}} t_{\mathrm{ON}}\frac{V_{\mathrm{dc}}}{3}. \tag{15}$$

For turn-off time, instantaneous power loss can be expressed as

$$P_{\mathrm{OFF}}(t) = i_{\mathrm{SW}}\, v_{\mathrm{SW}} = 2V_{\mathrm{dc}} I_{\mathrm{SW}}\left(1 - \frac{t}{t_{\mathrm{OFF}}}\right)\frac{t}{t_{\mathrm{OFF}}}. \tag{16}$$

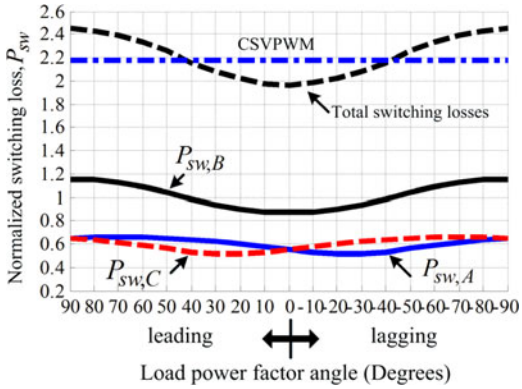

Fig. 19. Normalized switching losses of DSVPWM type 1 in balanced output voltage condition.

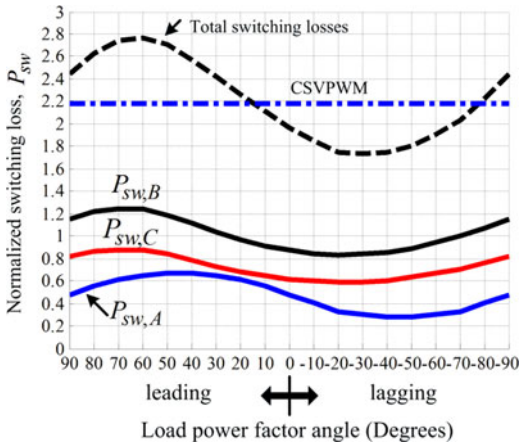

Fig. 20. Normalized switching losses of DSVPWM type 2 in balanced output voltage condition.

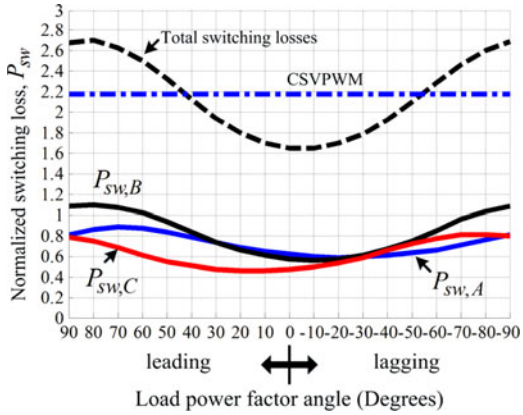

Fig. 21. Normalized switching losses of DSVPWM type 3 in balanced output voltage condition.

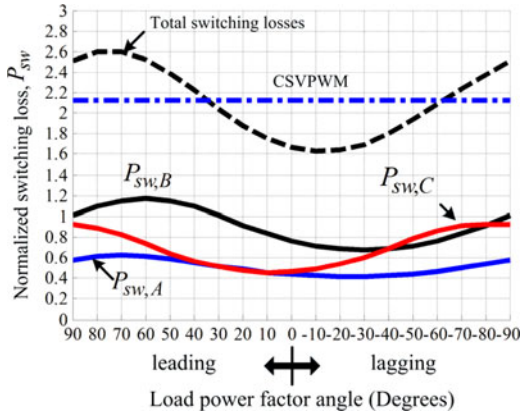

Fig. 22. Normalized switching losses of DSVPWM type 3 in unbalanced output voltage condition.

Then, the average switching power loss during turn-off is

$$P_{\mathrm{OFF,avg}} = \frac{1}{T_{SW}} \int_0^{t_{\mathrm{OFF}}} P_{\mathrm{OFF}}\,(t)dt = f_{SW}\, I_{SW}\, t_{\mathrm{OFF}}\, \frac{V_{\mathrm{dc}}}{3}. \tag{17}$$

Total average switching loss in a switching period is

$$P_{\mathrm{SW}} = P_{\mathrm{ON,avg}} + P_{\mathrm{OFF,avg}} = f_{\mathrm{SW}}\, I_{\mathrm{SW}}\, (t_{\mathrm{ON}} + t_{\mathrm{OFF}})\, \frac{V_{\mathrm{dc}}}{3}. \tag{18}$$

Note that I_{SW} in Fig. 14 for any switching period is assumed constant for determining average switching losses during such interval. For over fundamental period, magnitude of I_{SW} varies with time and relates to the load current. Therefore, I_{SW} can be expressed as

$$I_{\mathrm{SW}} = \begin{cases} 0 & : \text{unmodulated time} \\ |i_a| & : \text{modulated time} \end{cases} \tag{19}$$

where i_a is the load current of phase-leg a. Note that I_{SW} is assigned to be zero during clamping time or unmodulated time since there is no switching of devices in the same leg. As a consequence switching power loss P_{SW} is zero in accordance with (18).

For the proposed DSVPWM method, switching frequency (f_{SW}) is 1.5 times the switching frequency of CSVPWM method [2], [5], [10]. When considering voltage and current of switching devices as shown in Fig. 15, Fig. 15(a) illustrates carrier and modulating signals for a comparison in order to generate PWM signals for upper and lower switching devices in phase-leg a (i.e., S_1 and S_4) of the main power circuit in Fig. 1. Waveforms of voltage across S_1, current of S_1 and current of S_4 are shown in Fig. 15(b), (c), and (d), respectively. For the time interval between t_4 and t_5, S_4 is ON resulting in continuous switch current. Therefore, conduction loss occurs in S_4 which is neglected for considering the switching loss in phase-leg a devices. The time variant average switching loss waveform over a switching period which is dependent of current value I_{SW} and the dotted line representing an average of switching losses over a fundamental period are shown in Fig. 15(e). The switching loss during clamping is zero. Clearly, in order to reduce switching losses, clamping zone can be made at peak value of the load current.

Advantage of DSVPWM strategy is a reduction in switching losses considering the load current as a main point since the switching loss of a switch depends on not only a modulating function but also current and load power factor angle. From (19),

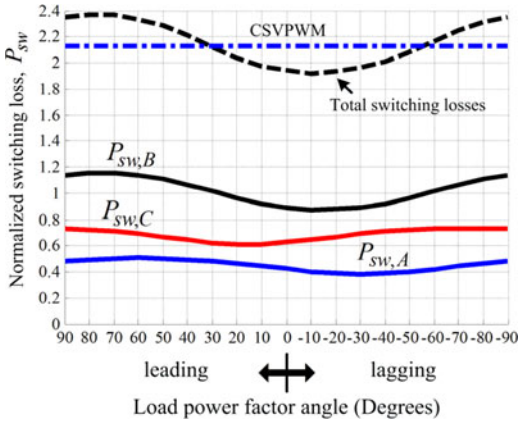

Fig. 23. Normalized switching losses of DSVPWM type 1 in unbalanced output voltage condition.

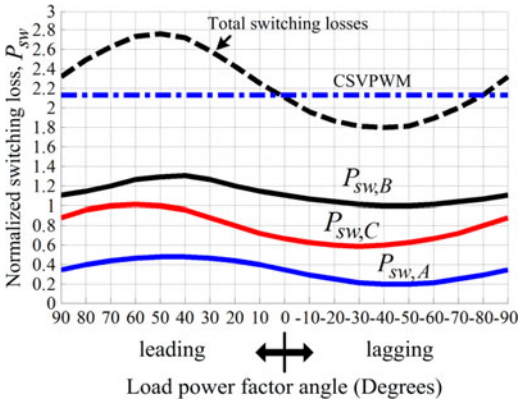

Fig. 24. Normalized switching losses of DSVPWM type 2 in unbalanced output voltage condition.

$I_{\rm SW}$ is the absolute value of load current during modulated time or switching times for both switching devices in the same leg, while at clamping time $I_{\rm SW}$ is zero. The proposed DSVPWM type 1, 2, and 3 techniques with power factor angle of 30° for unbalanced output voltages are illustrated in Figs. 16–18, respectively, in terms of normalized phase-leg voltages v_a^*, v_b^*, and v_c^*; fundamentals of normalized phase-leg voltages v_a^{**}, v_b^{**}, and v_c^{**}; and absolute load current and normalized switching loss. From these figures, one can see, clearly, that normalized power switching loss is zero at clamping zone resulting in a reduction in switching losses. The switching loss waveforms are similar to the absolute load current waveforms with 1.5 times the value due to the switching frequency according to (18). Time intervals of clamping for each phase-leg are not equal resulting in unequal switching losses for each leg. Clearly, the average of switching losses is unequal due to the sector time according to Figs. 4, 9, and 12.

When considering DSVPWM mentioned earlier, the power factor angle varies between 0°–90° lagging and 0°–90° leading. It is found that type 1 gives unequal switching losses for each phase due to unequal clamping intervals for each sector. From Fig. 19, the sum of normalized switching losses of each phase-leg ($P_{{\rm sw},A}, P_{{\rm sw},B}$, and $P_{{\rm sw},C}$) for DSVPWM type 1 is minimum at 1.97 with unity power factor while the sum of switching losses of each phase-leg for the conventional balanced SVPWM (CSVPWM) is 2.18. The proposed DSVPWM gives 9.6% reduction of switching losses. DSVPWM type 2 gives a minimum switching loss at 1.734 with a power angle of 30° lagging as shown in Fig. 20. The reduction of switching losses is 20.46% when compared to CSVPWM.

From the analysis of DSVPWM type 1–3 as mentioned earlier, DSVPWM is focused on switching losses of the RL load. Generally, at full load operation, a two-phase induction motor has a lagging power factor of 0.866° or 30° power angle. Although DSVPWM type 2 gives minimum switching losses at 30° lagging power factor angle, switching losses of each phase-leg are unequal. Therefore, in order to balance switching losses for each phase-leg, the proposed DSVPWM technique divides

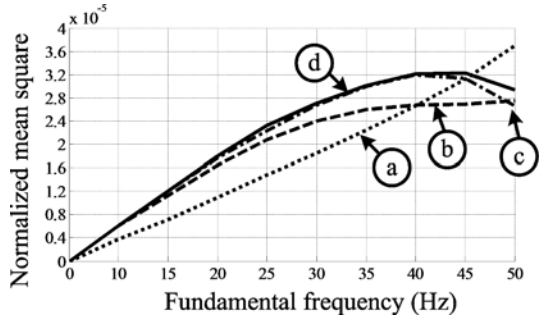

Fig. 25. Normalized mean square current ripple in unbalanced output voltage condition ($\delta = 30°$). (a) CSVPWM. (b) DSVPWM type 1. (c) DSVPWM type 2. (d) DSVPWM type 3.

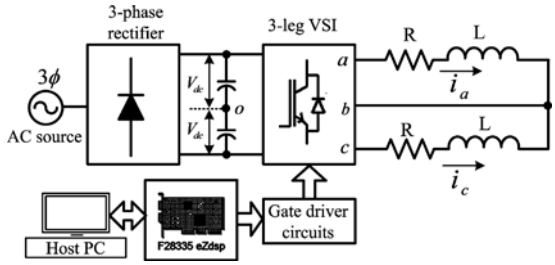

Fig. 26. Overall proposed system.

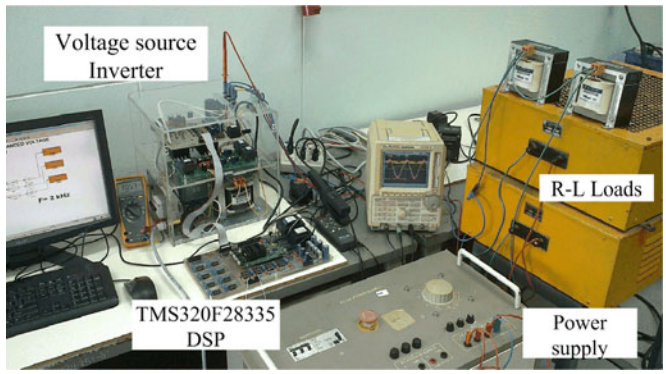

Fig. 27. Photograph of the experimental setup.

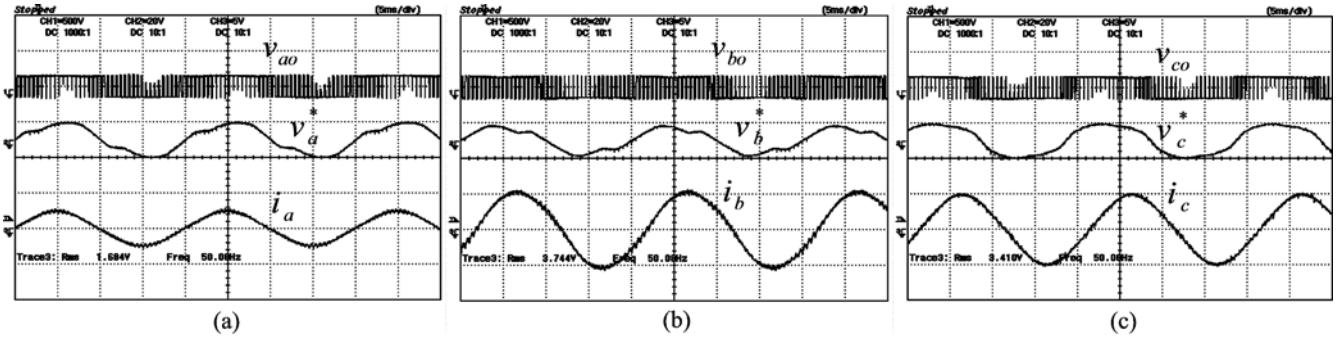

Fig. 28. Unbalanced output voltage CSVPWM.

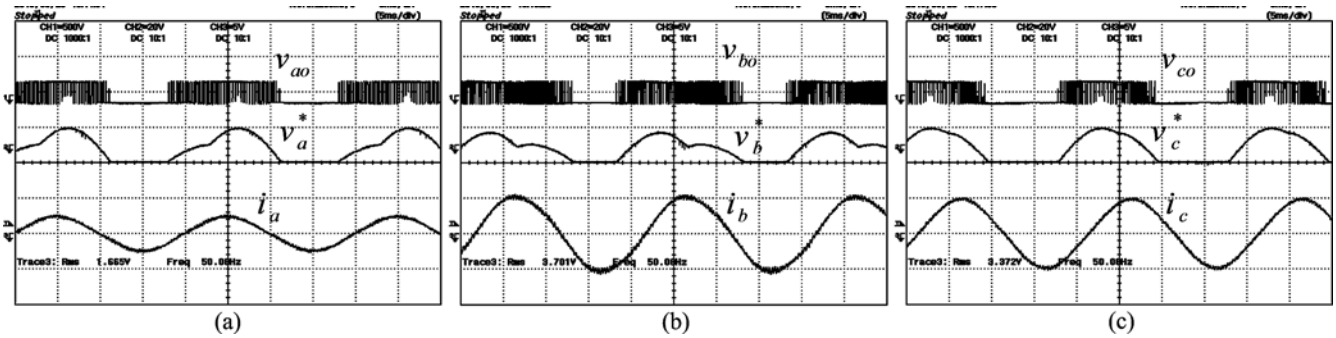

Fig. 29. Unbalanced output voltage DSVPWM type 1.

the zone for clamping at peak current zone of the load current for the 30° lagging power factor angle as shown in Fig. 12. The zone is divided into ten subzones so that the clamp occurs at peak current zone which has equal clamping time. As a result, switching losses for each phase-leg are equal for both balanced and unbalanced phase voltage cases as illustrated in Figs. 21 and 22, respectively.

Figs. 16–18 illustrated normalized switching losses for each leg under unbalanced output voltages with the unbalanced voltage angle (δ) of 30° for all proposed DSVPWM types. According to Fig. 16, DSVPWM type 1 for phase-leg a gives normalized switching losses of 0.38, 0.9, and 0.69 for phase-leg a, b, and c, respectively.Total normalized switching loss is 1.97 in accordance with Fig. 23 at 30° load lagging power factor angle. With the same load power factor angle, DSVPWM type 2 gives a total normalized switching losses of 1.79 in accordance with Fig. 24. Also, for DSVPWM type 3, the total normalized switching loss is 1.69 in accordance with Fig. 22. When comparing total normalized switching losses for the VSI with the RL load of 0.866 lagging power factor for three types, it is concluded that DSVPWM type 3 gives the lowest normalized switching losses. Although the proposed techniques are effective in producing equal switching losses under the balanced voltage condition, for the unbalanced case, the proposed technique (type 3) produces only equal switching losses for two legs at 30° power factor angle. The switching loss of another leg is slightly different from those of the others. Clearly, switching losses for each leg at any power factor are significantly different for types 1 and 2 as shown in Figs. 22–24.

B. Output Current Ripple

Output current ripple for the two-phase three-leg VSI using CSVPWM and DSVPWM can be calculated. Output voltage across an inductor load consists of fundamental output voltage and ripple voltage at ripple frequency depending on harmonic frequency [19], [20]. Ripple voltage can be expressed as

$$v_{\text{ripple}}(t) = v_{\text{line}} - v_{\text{line},1}. \tag{20}$$

From the basic inductor voltage equation $v_L = L\frac{\mathrm{d}i}{\mathrm{d}t}$, the inductor current is

$$i_L(t) = \frac{1}{L}\int v_L \mathrm{d}(t). \tag{21}$$

Similarly, ripple current is

$$i_{\text{ripple}}(t) = \frac{1}{L}\int v_{\text{ripple}}(t)\mathrm{d}(t). \tag{22}$$

The mean square value of the output current ripple over one fundamental frequency can be obtained by

$$i_{\text{ripple,avg}} = \frac{1}{2\pi}\int_0^{2\pi} i_{\text{ripple}}^2(t)\,\mathrm{d}(t). \tag{23}$$

According to (23), the results of the output current ripple obtained from the simulation of the proposed DSVPWM with MATLAB/SIMULINK are illustrated in Fig. 25 where normalized mean square current ripple occurs under unbalanced output voltage conditions with unbalanced voltage angle of 30° and constant V/F in accordance with scalar control induction motor applications. It is found that the proposed technique

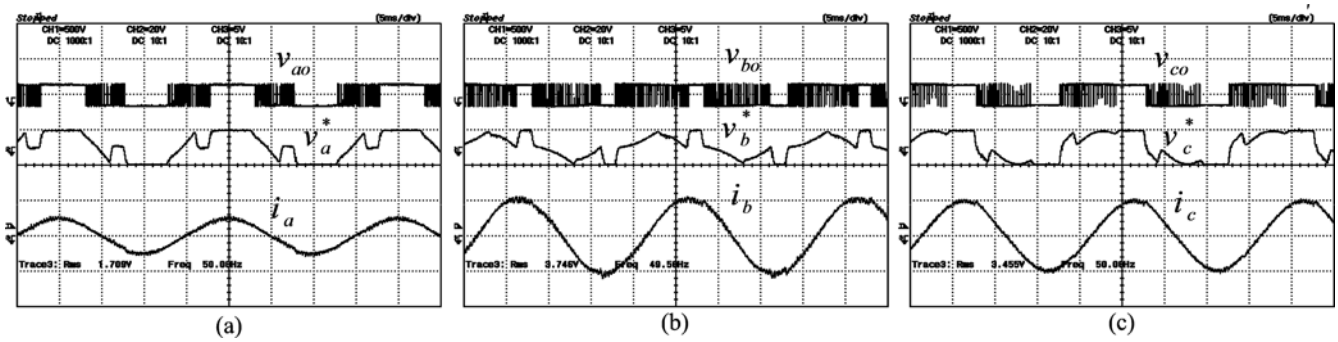

Fig. 30. Unbalanced output voltage DSVPWM type 2.

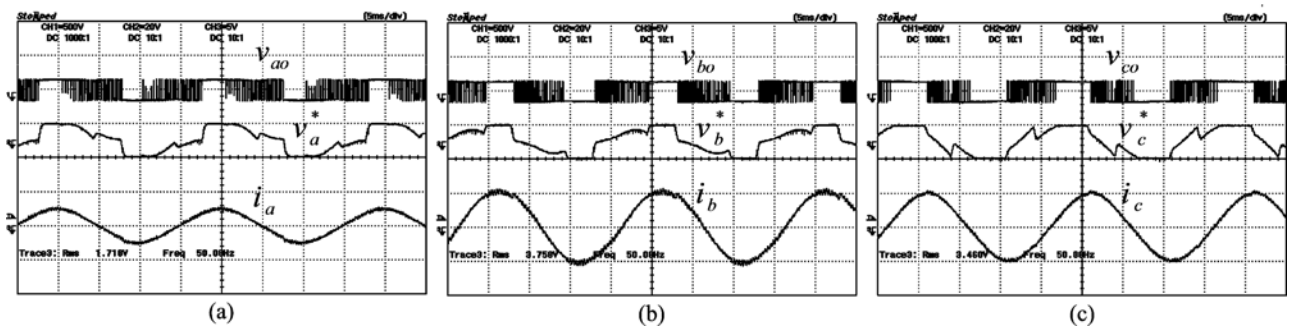

Fig. 31. Unbalanced output voltage DSVPWM type 3.

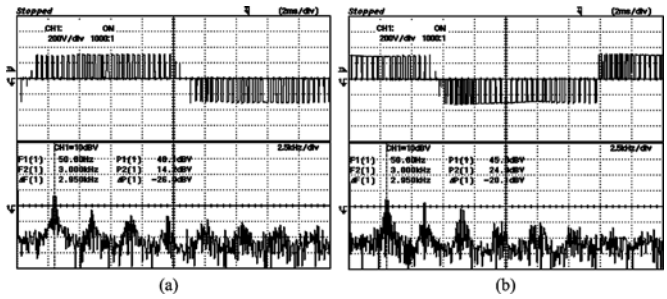

Fig. 32. Output voltages spectrum of DSVPWM type 3. (a) v_{ab}. (b) v_{cb}.

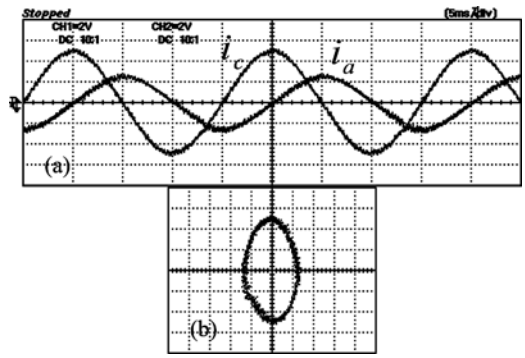

Fig. 33. Output currents of DSVPWM type 3 (a) i_a and i_c and (b) locus of output currents.

offers lower current ripple than the conventional one in a range between 45 and 50 Hz.

V. Experimental Results

The overall system for verifying the DSVPWM method is shown in Figs. 26 and 27. It consists of a three-phase diode bridge rectifier with filter capacitors providing smooth dc-link voltage, a three-leg VSI (VSI) converting dc voltage into adjustable voltage frequency of ac, resistors and inductors connected in series acting as a two-phase load set. The VSI employs IGBTs as semiconductor switches. Modulated signals for driving all IGBTs are generated by Digital signal processor TMS320F28335 EZDSP board [18] together with MATLAB/SIMULINK as shown in Fig. 27. DC bus voltage is 300 V resulting in voltage across each capacitor of 150 V. Each RL load has resistance of 35 Ω and inductance of 50 mH to obtain 0.866 lagging load power factor (i.e., 30° power factor angle). The load current lags 30° with respect to the fundamental voltage. This condition is required for testing of minimum switching losses. The experimental setup is shown in Fig. 27. The testing conditions are divided into two parts for comparative purposes for unbalanced output voltage DSVPWM:

1) comparison of switching losses for each condition of CSVPWM, type 1, type 2, and type 3;
2) comparison of output load current ripple i_a and i_c for each condition of CSVPWM, type 1, type 2, and type 3.

The unbalanced angle (δ) is set at 30°, and the modulation index is kept at 1.414. Figs. 28–31 show waveforms of reference voltage, phase-leg voltage with respect to the midpoint of

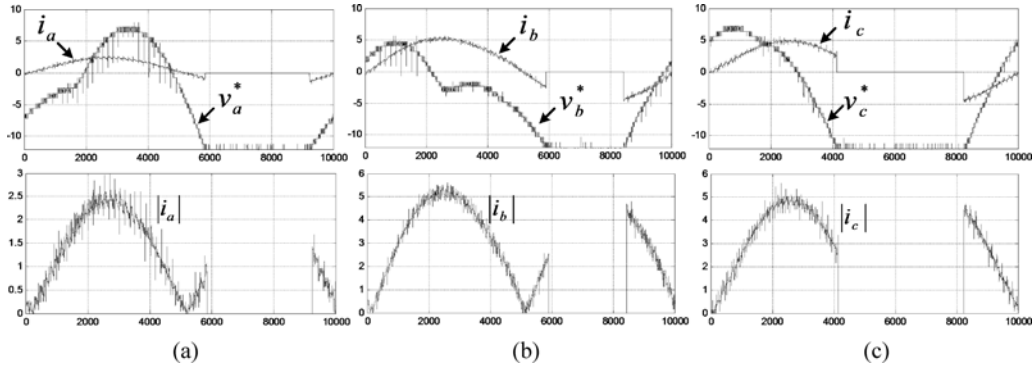

Fig. 34. Switching losses of unbalanced output voltage (type 1).

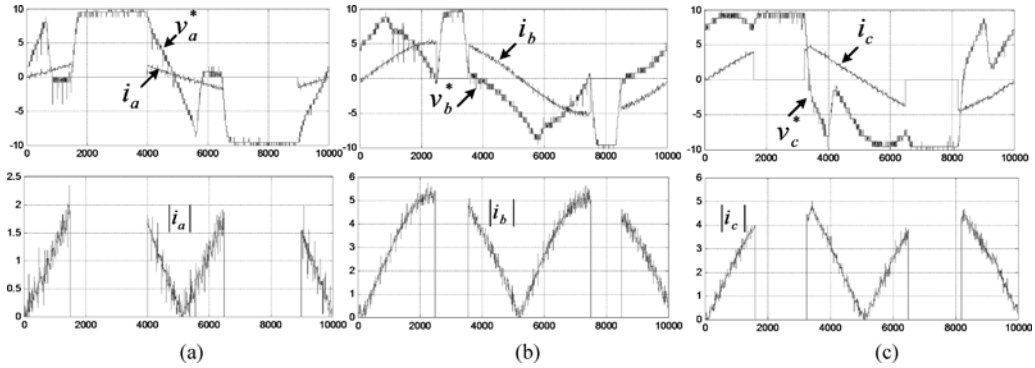

Fig. 35. Switching losses of unbalanced output voltage (type 2).

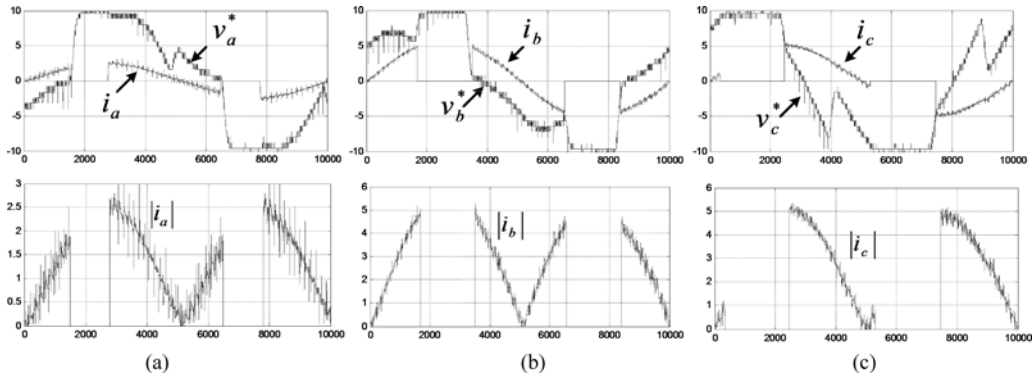

Fig. 36. Switching losses of unbalanced output voltage (type 3).

dc bus, output phase current for each phase having 0.866 load power factor as mentioned earlier. As can be seen, magnitude of phase a current i_a is lower than that of phase c current i_c due to unbalanced fundamental phase voltages. In order to confirm this, harmonic voltage spectrum is shown in Fig. 32 which is for type 3. First harmonic sidebands are around at 3 kHz. Fundamental voltage magnitudes of v_{ab} and v_{cb} are 40.1 dB (143 V) and 45.0 dB (254.4 V),respectively which are in accordance with (7) and (8). Fig. 33 illustrates waveforms of i_a and i_c. Phase difference angle between these currents is 90°. Due to unbalanced output voltages for the two-phase load, the magnitude of i_a is lower than that of i_c. The locus of currents is elliptical due to unbalanced magnitudes and 90° phase difference.

TABLE III
NORMALIZED POWER SWITCHING LOSSES FOR UNBALANCED VOLTAGE CASE

Method	Phase a	Phase b	Phase c	Total
CSVPWM	2.20	3.31	2.50	8.01
Type 1	1.26	3.29	2.75	7.30
Type 2	0.64	3.55	2.32	6.51
Type 3	1.42	2.44	2.41	6.27

Figs. 34–36 represent the analysis of the normalized power switching loss for each phase of type 1, type 2, and type 3. The

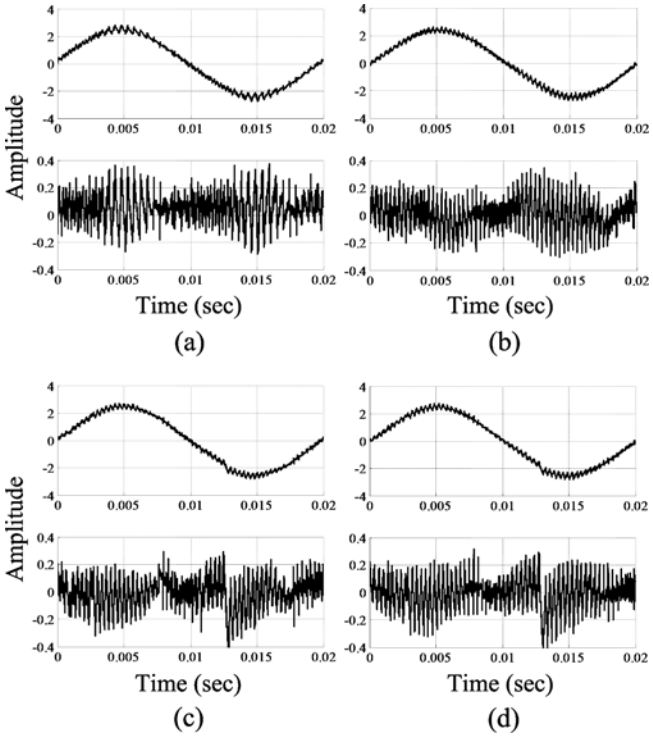

Fig. 37. Measured load current ripple of phase-leg a (i_a) in each type at modulation index = 1.414, $F_1 = 50$ Hz, $f_{\rm SW} = 2$ kHz for CSVPWM and $f_{\rm SW} = 3$ kHz for DSVPWM (a) CSVPWM, (b) type 1, (c) type 2, and (d) type 3. The measured mean square of load current (i_a) of (a) 0.0125, (b) 0.0094, (c) 0.01142, and (d) 0.0109.

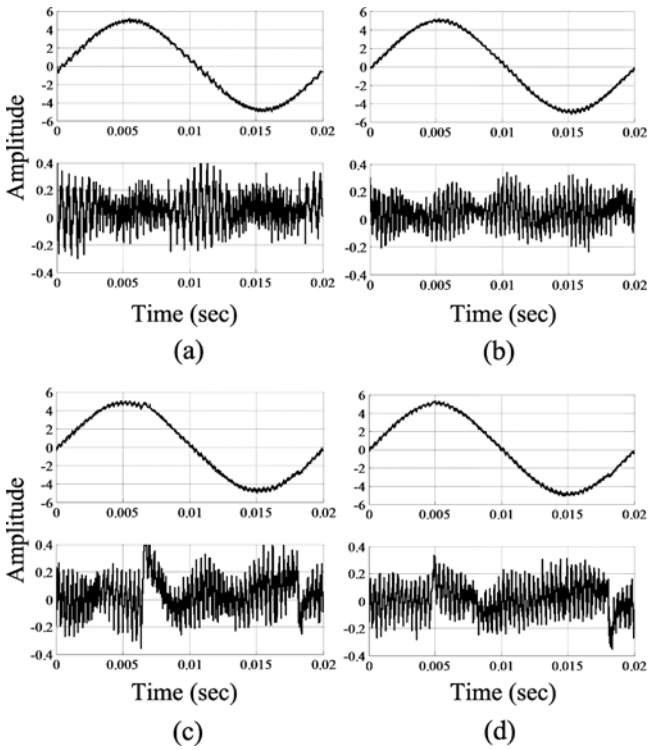

Fig. 38. Measured load current ripple of phase-leg a (i_c) in each type at modulation index = 1.414, $F_1 = 50$ Hz, $f_{\rm SW} = 2$ kHz for CSVPWM and $f_{\rm SW} = 3$ kHz for DSVPWM (a) CSVPWM, (b) type 1, (c) type 2, and (d) type 3. The measured mean square of load current (i_c) of (a) 0.01275, (b) 0.01037, (c) 0.01541, and (d) 0.01099.

measured data of voltages and currents for each phase is used for mathematical calculations by using MATLAB/SIMULINK. The data were collected at fundamental frequency of 50 Hz or 2 ms/div and sampling rate of 500 kHz. Ten thousand sampled data were captured. After that phase-leg currents were performed to be absolute values: $|i_a|$, $|i_b|$, and $|i_c|$. Absolute current value is zero when the clamp occurs at positive and negative reference voltage. Average absolute current was used as the normalized power switching losses for the analysis of switching losses for each type.

Table III illustrates the normalized power switching losses derived from the average of $|i_a|$, $|i_b|$, and $|i_c|$. According to Table III, the average of switching losses for type 3 of phase-leg b and c are approximately equal. Also, the sum of switching losses for type 3 is minimum. This means that type 3 DSVPWM gives minimum switching losses at load power factor of 0.866.

Testing of the current ripple was conducted to consider the comparison between CSVPWM and DSVPWM. Current waveforms of i_a and i_c, and ripple are shown in Figs. 37 and 38. The ripple currents are extracted from currents excluding fundamental components using MATLAB/SIMULINK. All types give current ripple in lower level than the conventional technique. Note that for type 2, as shown in Fig. 38(c), it implies that i_c has higher mean square of the ripple current in a fundamental period due to the transition between sectors 5 and 6. The reason is that this error arises from the implementation. The types 2 and 3 provide the ripple current in the same level.

VI. Conclusion

A discontinuous space vector PWM technique for a three-leg VSI supplying balanced two-phase loads has been proposed. The principle of the proposed DSVPWM has been described. Three types of the proposed DSVPWM are investigated in order to improve performance for balancing switching losses for each phase-leg. The proposed DSVPWM offers reductions of switching losses and load current ripple. The proposed DSVPWM type 1 suits a pure restive load. The proposed DSVPWM types 2 and 3 are suitable for RL Loads with 30° lagging power factor angle. Especially, the proposed DSVPWM type 3 which has ten zone divisions is capable of balanced losses for each leg with adjustment of an increase in unbalanced voltage angle. From the testing results, the current ripple for the proposed technique is lower than for the CSVPWM. The validity of the proposed technique are verified by simulation and experimental results in terms of voltage spectrum, current waveforms, reductions in switching losses and output current ripple at high modulation index when compared to a CSVPWM technique.

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