# Buck-Derived Converters Based on Gallium Nitride Devices for Envelope Tracking Applications

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***Abstract*—Envelope tracking (ET) is a technique designed to enhance the efficiency of radio frequency power amplifiers (RF PA). It is based on providing the voltage to the RF PA with variations that mimic the shape of the envelope of the communication signal that the RF PA is processing. As the bandwidth of these signals can be around several megahertz, the switching frequency of the switching mode power supply designed for ET applications has to be very high. The good switching characteristics of Gallium Nitride devices makes them suitable for this application. This paper presents two multiphase converters to be used as envelope modulators in envelope tracking applications.**

***Index Terms*—DC-DC power conversion, gallium compounds, microwave power amplifiers.**

## I. Introduction

THE simultaneous phase and envelope variations, typical of spectrally efficient wireless communication standards, require using back-off linear RF PAs, which are unavoidably power inefficient. In order to increase the efficiency of these systems, a technique called envelope tracking (ET), can be applied. Different implementations and theoretical analyses of this technique can be found in the literature [1]–[3].

In order to explain how the envelope tracking works, a brief introduction will be presented here. Fig. 1 shows the basic architecture of this technique. The dc/dc converter that provides power to the RF PA is often known as envelope modulator.

The key point is that the voltage provided to the RF PA varies trying to match the envelope of the communication signal. As the voltage in the drain of the main transistor of the RF PA is varying along the envelope signal by means of the output voltage of the envelope modulator, the voltage across the power transistor of the RF PA is lower than in the case of having a constant voltage and, therefore, the efficiency increases. In RF terminology, the RF PA operates always near compression, which is where it presents its highest efficiency.

Regarding the overall efficiency, one of the most critical parts is the envelope amplifier or envelope modulator. In order to keep its efficiency high, a switching mode dc/dc converter is often used [4]–[9]. However, the bandwidth and slew rate requirements imposed by the communication signals usually surpass the capabilities of standard switching mode dc/dc converters. In order to solve that, combination of switching mode dc/dc converters with linear stages have been proposed [10]–[13]. The use of linear stages can be avoided or minimized if higher switching frequencies are used in dc/dc converters. Here, gallium nitride devices for power supplies are an enabling technology. Their low values of on-state resistance and parasitic capacitances make them a good option to act as the controlled switching devices of dc/dc converters. One example of the utilization of such devices in envelope tracking applications can be found in [14].

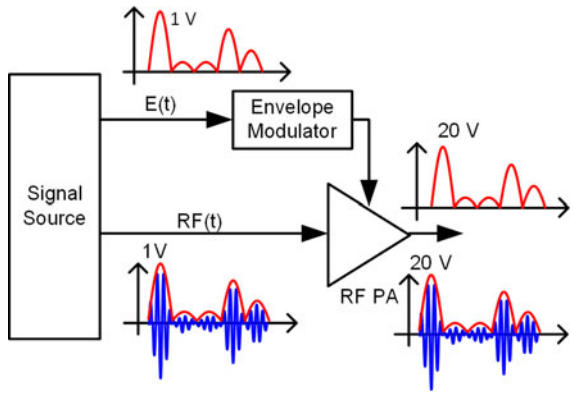


Fig. 1. Envelope tracking architecture.

In this paper, a 8-MHz Buck converter cell using a GaN HEMT (*High Electron Mobility Transitor*) is presented. This cell is made up of the transistor itself and the freewheeling diode, along with an isolator and the driver for the transistor. Bypass capacitors are added to stabilize the input voltage to the cell converter. This cell can be combined with more similar cells, different output filters and voltage selection networks to build different dc/dc converters. Two of them, a two-phase buck and a floating two-phase buck are presented here along experimental results showing communication waveforms.

This paper is organized as follows. Section II shows the basic design of the buck cell. Two different dc/dc converter topologies obtained with this cell are shown in Section III. The control system for both converters will be explained in Section IV. Experimental results are shown in Section V. Finally, conclusions are addressed in Section VI.

## II. Buck Cell Design

The cornerstone of the dc/dc converters presented in this paper is the switching cell shown in Fig. 2. It is formed by the active switch, a normally-off GaN HEMT, its driving circuitry, the freewheeling diode, which is a Si Schottky diode with very low parasitic capacitances, and a set of bypass capacitors $C_{\mathrm{bypass}}$.

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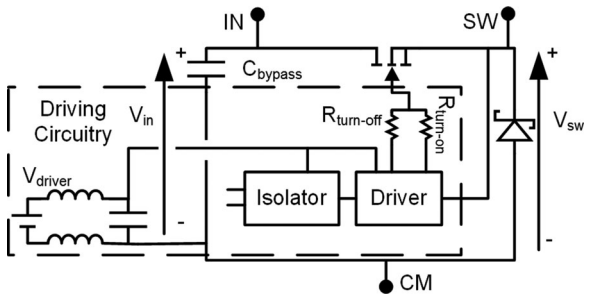


Fig. 2. Schematic of the buck cell.

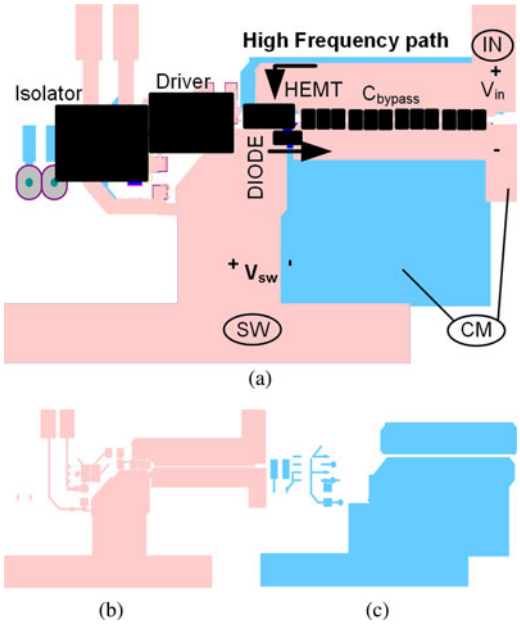


Fig. 3. (a) Layout of the buck cell. (b) Top layer. (c) Bottom layer.

In order to achieve a switching frequency of 8 MHz, a careful layout of the switching cell circuit board has to be designed. Special attention should be paid to the path between the transistor, the diode, and the common node, labeled CM in Fig. 2. The path from the driver to the gate of the transistor and its return paths must be carefully routed. As the selected driver is the LM5114 from Texas instruments, different resistors for the turn off and turn on of the transistor can be used. The purpose of this resistor is to damp the oscillations on the gate of the transistor. Advice for using these devices at high frequencies can be found in [15]. The power supply to the driver is provided through a common mode choke and bypass capacitors to provide good decoupling.

The actual layout of the cell can be seen in Fig. 3(a). It is a two layer PCB, where the top layer is shown in Fig. 3(b) and the bottom layer in Fig. 3(c). Most of the components described in Fig. 2 can be seen over the layout. It can be seen how the high-frequency paths are extremely short. This high-frequency path connects the switching node (SW) to the input node (IN) through the HEMT and to the node CM through the freewheeling diode. It is important to note that the copper areas to which CM is connected extends on the top layer [see Fig. 3(b)] and the bottom layer [see Fig. 3(c)]. The switching node, labeled SW in Fig. 2, can be connected to an *LC* filter to easily form a buck converter, the path to the output filter being less critical than in the case of the aforementioned paths.

A freewheeling diode was used instead a synchronous rectifier to ease both the design of the PCB and the control stage. If two HEMTs were used, one acting as the main switch and the other as a synchronous rectifier a careful control of the dead-times between the gate signal of both devices should be addressed to minimize losses. This kind of transistors (enhancement mode HEMT) lack a body diode, however the reverse conduction can be achieved with a gate to source voltage equal to 0. In these conditions, as the drain voltages decreases, the gate will be set to a voltage above drain's voltage (which is negative now). When the gate-to-drain voltage reaches the threshold voltage, the device starts conducting (in some way the drain and the source terminals interchange their roles). A detailed explanation of this process can be found in[15] and[16]. In this situation, the voltage drop in the device is higher than in a comparable Si diode (or even in the body diode of a Si MOSFET), and a careful timing of the gate signals (even superposing them) is important to minimize losses in the device [15]. With a freewheeling Si Schottky diode the necessity of these careful control is avoided and good efficiency can be achieved.

## III. Converter Topologies

This basic cell can be combined in several ways to improve the bandwidth achieved and the efficiency of the system. Fig. 4 shows the different ways in that the cells are combined. The first one is a two-phase buck converter, represented in Fig. 4(a). General theory about filter design for Buck-type converters can be found in [17]. The extension of the aforementioned filter design process to multiphase buck converters can be found in [18]. Multiphase operation introduces a notch at the switching frequency which improves the rejection ratio of the filter used.

A variation of the two-phase buck converter is shown in Fig. 4(b). As in the previous case, both terminals $CM_1$ and $CM_2$ have been connected together. However, this common point has not been connected to ground in this case, but to a offset voltage selected by the MOSFET transistors labeled $MOSFET_2$, $MOSFET_1$, and $MOSFET_0$ in Fig. 4(b). Fig. 5 shows the main voltages in this converter. The offset voltage, labeled $V_{\mathrm{offset}}$, is the voltage between terminals $CM_1 = CM_2$ and ground. The voltage between CM and the output is labeled $V_{\mathrm{o\_CM}}$ Finally, the output voltage referred to ground is labeled $V_o$. The offset voltage can take values $V_{g2}$, $V_{g1}$ or 0, depending on what MOSFET is ON. The selection of the offset voltage depends on the desired output voltage, in such a way that the offset voltage is always lower than the output voltage $V_o$. The difference between the output voltage and the offset voltage $V_{\mathrm{o\_CM}}$ will be provided by the two-phase buck converter based on GaN devices, which is switching at high constant frequency. On the other hand, the MOSFETs are standard Si devices which select the proper offset voltage at low variable frequency, depending on the waveform to be reproduced, just as in [13]. The

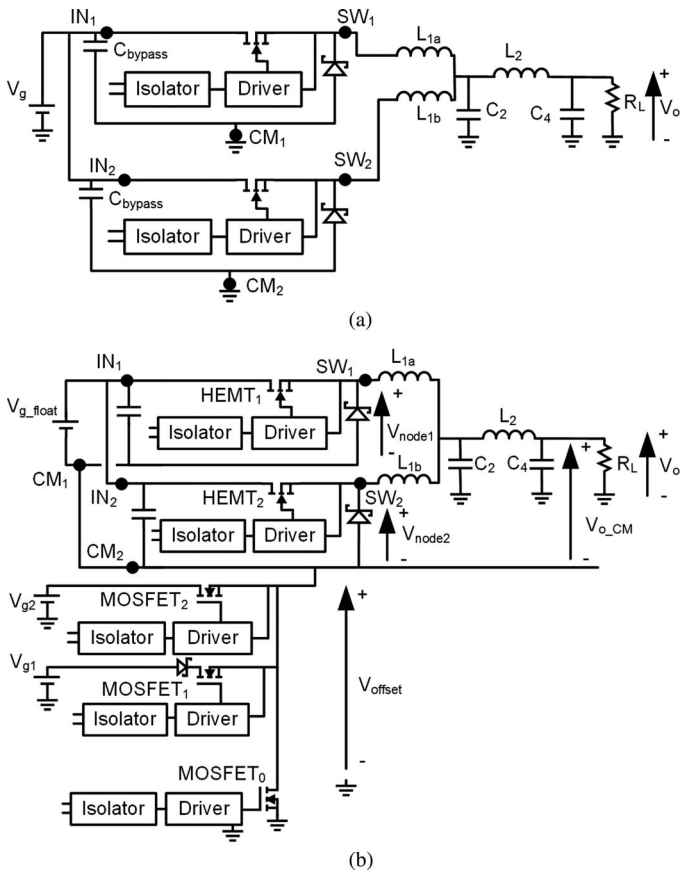


Fig. 4. Combinations with the switch cell: (a) Two-phase buck with fourth-order filter. (b) Floating two-phase buck with fourth-order filter.

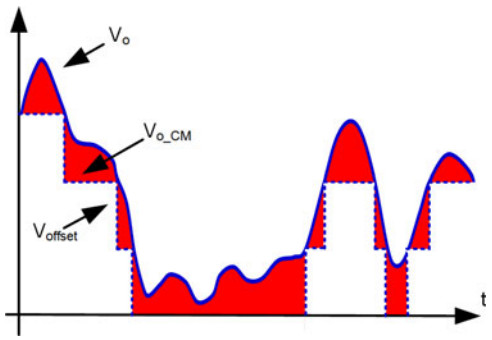


Fig. 5. Explanation of voltages in the floating two-phase buck converter.

voltage waveforms at the input of the filter are the same as in the multiple input buck converter, formerly presented in [8]. In summary, the offset voltage provides a coarse representation of the waveform to be reproduced, while the high-frequency switching cell provides a fine adjustment of that waveform. This allows the high-frequency switching cells not to process all the power, thus increasing the overall efficiency. This implementation can be called floating two-phase buck. It is important to note that the input voltage source to the switching stage $V_{\mathrm{g\_float}}$ must be isolated from the other voltage sources. The principal advantage of the floating two-phase buck over the multiple input buck, which is a multilevel converter, is that instead of having several high-frequency transistors, switching between close voltages at high frequency, there are only two high-frequency switching cells forming a two-phase buck converter. The input voltage to these cells is also low, minimizing switching losses, while a wide output voltage range is obtained with the combination of the high-frequency cells with the low frequency offset selection network.

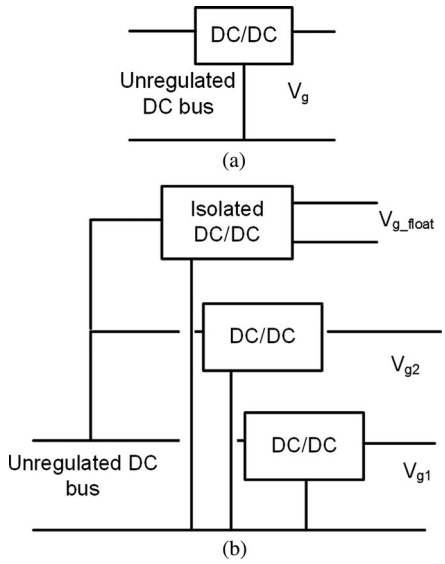


Fig. 6. (a) Power supply architecture for the two-phase buck. (b) Power supply architecture for the floating two-phase buck.

The two-phase buck converter with high-order output filter, formerly presented in [18], and the new floating two-phase buck converter, also with a high-order output filter, benefit from the ripple cancellation typical of multiphase buck converters [18], [19]. The output filter demands (i.e., good rejection of the switching frequency, little distortion in the passband and good step response) will be similar in both cases. Although the floating two-phase buck seems more promising than the two-phase buck, the control system is more complex. The description of the control system of both converters can be found in Section IV. Moreover, the need of more voltage supplies is a limitation of this topology. The power architecture needed for both converters is shown in Fig. 6. For the two-phase buck converter [see Fig. 6(a)], an unregulated dc bus voltage (maybe the output voltage of a PFC converter) is regulated, by means of another dc/dc converter, to voltage $V_g$, which is the only voltage needed by the two-phase buck converter. The architecture needed by the floating two-phase buck converter is more complicated, as can be seen in Fig. 6(b). The same unregulated bus is used to generate the voltages for the offset levels $V_{g1}$ and $V_{g2}$. From the same bus, and isolated from the other ones, the input voltage to the switching stage, $V_{\mathrm{g\_float}}$ is also generated. All these voltages are regulated through the use of different dc/dc converters.

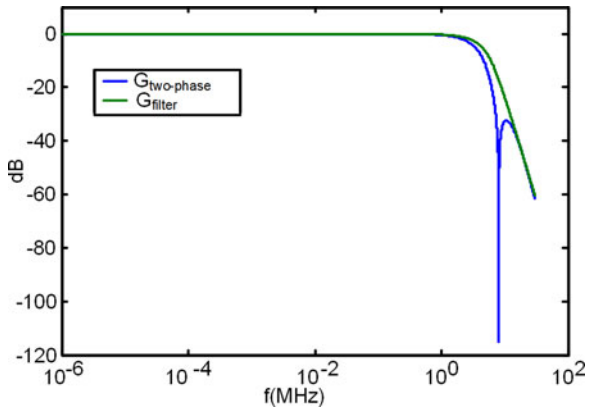


Fig. 7. Bode plot of a fourth-order Bessel filter with 3.5-MHz cutoff frequency.

## IV. Control

### A. Filter Design

The process used to design the filter for a two-phase buck converter can be found in [18] for limited bandwidth envelopes. However, the criteria used here is the step response instead of the bandwidth of the signal to reproduce. This approach can be found in [17], where several types of filters were compared. In order to obtain a step response with no overshoot, a fourth-order Bessel–Thomson filter is used. The rejection of the switching frequency components is obtained by the notch effect due to the multiphase operation, as described in [18].

In this paper, a fourth-order Bessel–Thomson filter with a cutoff frequency of 3.5 MHz has been selected after some experimental tries. This cutoff frequency is enough to reproduce some complex waveforms such as the OFDM envelope shown in Section V. The switching frequency is 8 MHz. Therefore, the ratio between the switching frequency and the cutoff frequency of the filter is 2.28. As can be found in [17] for a single-phase Buck converter any value of the ratio between the switching frequency and the cutoff frequency above 2 guarantees the operation in continuous conduction mode (CCM). In the case of a two-phase buck converter, a similar condition can be found in [18]. Operation in CCM enables the linearity between the output voltage and the duty cycle. So, in order to reproduce a waveform, such as those shown in Section V, it is enough to encode the waveform in the duty cycle. The response of the function $G_{\mathrm{two-phase}}(s)$ which represent the effect of the filter and the two-phase operation, can be seen in Fig. 7. In the same figure, the response of the filter $G_{\mathrm{filter}}(s)$ is represented to see the notch effect due to the two-phase operation. $G_{\mathrm{two-phase}}(s)$ provides 7 dB of rejection at 4 MHz, which can be enough to reject the harmonics corresponding to the lower side band produced by the PWM modulation.

### B. Considerations About the Floating Two-Phase Buck

When using the floating two-phase buck, it is important to maintain the linearity between the duty cycle and the output voltage while the offset voltage changes between different values. In order to study that, let us call $\Delta D$ the minimum change in duty cycle corresponding to the HEMTs. When the converter is forced to change its output voltage without changing the offset level, then the minimum output voltage change $\Delta V_{\mathrm{out}}$ will be

$$\Delta V_{\mathrm{out}} = \Delta D \cdot V_{\mathrm{g\_float}} \tag{1}$$

where $V_{\mathrm{g\_float}}$ is the floating input voltage, which always is the input voltage of the high-frequency switching stage [see Fig. 4(b)].

The practical duty cycle range that can be achieved taking into account the actual DPWM resolution and the driver characteristics is narrower than the theoretical one (0% to 100%). This duty cycle range will extend from $D_{\min}$ to $D_{\max}$. So, if an increase of $\Delta D$ takes place when the duty cycle is already $D_{\max}$ and $\mathrm{MOSFET}_0$ is ON (thus no offset level is applied), then the control circuitry must modify the duty cycle corresponding to the HEMTs and modify the state of the MOSFETs (turning off $\mathrm{MOSFET}_0$ and turning on $\mathrm{MOSFET}_1$). Therefore

$$(D_{\max} + \Delta D) \cdot V_{\mathrm{g\_float}} = V_{g1} + D_{\min} \cdot V_{\mathrm{g\_float}} \tag{2}$$

If the change in $\Delta D$ takes place when the offset level is $V_{g1}$, then the offset voltage will change by turning OFF $\mathrm{MOSFET}_1$ and turning ON $\mathrm{MOSFET}_2$. The duty cycle to the HEMTs will also change. Therefore

$$V_{g1} + (D_{\max} + \Delta D) \cdot V_{\mathrm{g\_float}} = V_{g2} + D_{\min} \cdot V_{\mathrm{g\_float}}. \tag{3}$$

Rearranging terms in (2) and (3) yield

$$D_{\max} \cdot V_{\mathrm{g\_float}} = V_{g1} + (D_{\min} - \Delta D) \cdot V_{\mathrm{g\_float}} \tag{4}$$

and

$$V_{g1} + D_{\max} \cdot V_{\mathrm{g\_float}} = V_{g2} + (D_{\min} - \Delta D) \cdot V_{\mathrm{g\_float}}. \tag{5}$$

It should be noted that if (4) and (5) are satisfied, the full range of the output voltage can be achieved. This range goes from $D_{\min} \cdot V_{\mathrm{g\_float}}$ to $V_{g2} + D_{\max} \cdot V_{\mathrm{g\_float}}$.

As the duty cycle resolution is very fine, the variation in the output voltage due to $\Delta D$ is very small and a good approximation of (4) and (5) is

$$D_{\max} \cdot V_{\mathrm{g\_float}} \approx V_{g1} + D_{\min} \cdot V_{\mathrm{g\_float}}, \tag{6}$$

and

$$V_{g1} + D_{\max} \cdot V_{\mathrm{g\_float}} \approx V_{g2} + D_{\min} \cdot V_{\mathrm{g\_float}}. \tag{7}$$

The duty cycle modifications necessary to perform the transition described by (2) and (3) are easily carried out in a digital way and they are described in Section IV-C. Fig. 8 shows how the transition works. The voltage produced by the high-frequency switching cells are shown in this figure (labeled $V_{\mathrm{node1}}$ and $V_{\mathrm{node2}}$ as in Fig. 4(b), this waveforms represent the voltage across the freewheeling diodes), along with the offset voltage ($V_{\mathrm{offset}}$) and the output voltage $V_{\mathrm{out}}$. It can be seen how waveforms $V_{\mathrm{node1}}$ an $V_{\mathrm{node2}}$ are square wave waveforms as in conventional buck converters. Due to the multiphase operation, $V_{\mathrm{node2}}$ is delayed half a switching period from $V_{\mathrm{node1}}$. When the transition occurs, the duty cycle changes from the maximum achievable to the minimum one. At the same time, the offset level $V_{\mathrm{offset}}$ increases. This change in offset is synchronized in such a way that both switching voltages $V_{\mathrm{node1}}$ and $V_{\mathrm{node2}}$ are

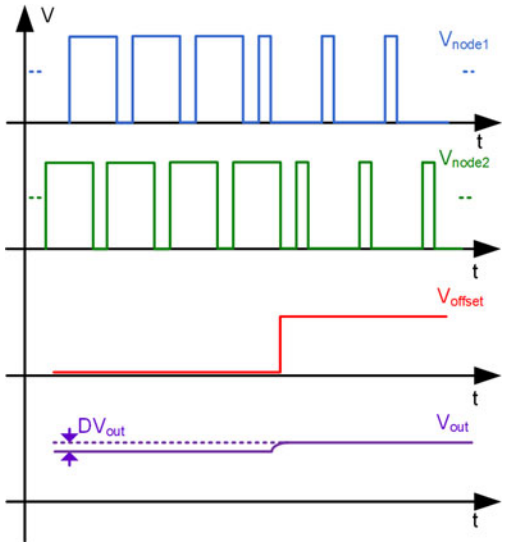


Fig. 8. Ideal transition between levels in the floating two-phase buck.

zero at the moment of the transition. This minimizes the distortion in the output voltage. The output voltage is also shown, it can be seen how the increase in the voltage is very low (ideally the same as an increase in the duty cycle).

Regarding the dynamic of the filter is important to note that two different situations are present when the converter is demanded to change its output voltage. Fig. 9 shows an equivalent model for this transitions using voltage sources that generate the offset and the switching waveforms. Fig. 9(b) represents the equivalent for a change only in the duty cycle, taking into account that $V_{\mathrm{node2}}$ is a delayed version of $V_{\mathrm{node1}}$. Therefore, $G_{\mathrm{two-phase}}$ models the evolution of the output voltage in response to changes in the duty cycle. In Fig. 9(c), the equivalent circuit for a change only in the offset is shown. There is no delay between the inductors and therefore the transfer function is only determined by the filter $G_{\mathrm{filter}}$. Fig. 10 shows the theoretical step response steps for the implemented filters, one of them taking into account the delay and the other one only the response of the filter. It can be seen how the filter is faster than the filter plus the delay. This means that a change in the output voltage that implies a change in the level must be faster than a change in the output voltage due to only a change in the duty cycle. It is important to note that during a transition the variations of the duty cycle have an opposite direction to the variations on the offset voltage. However, the synchronization process makes the whole system behaves as a normal multiphase converter as it will be seen in the experimental results (see Section V).

### C. Digital Pulsewidth Modulator

In order to achieve a good duty cycle resolution and high switching frequency (8 MHz), a digital pulsewidth modulator (DPWM) is employed. This DPWM is a hybrid DPWM with a delay line based in the carry-chain lines of the FPGAs. This kind of DPWM is described in [20]. The design is a 8 MHz, 10-bit resolution DPWM. A brief scheme of the DPWM is shown

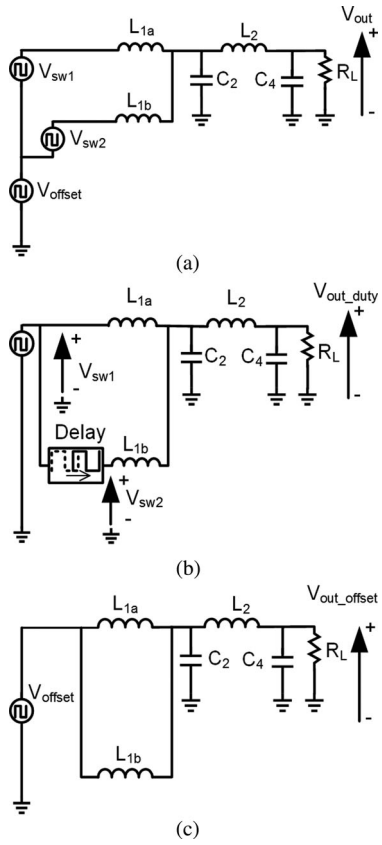


Fig. 9. Equivalent circuits to study the transitions: (a) Equivalent circuit. (b) Equivalent circuit for transients only in the duty cycle. (c) Equivalent circuit for transients only in the offset voltage.

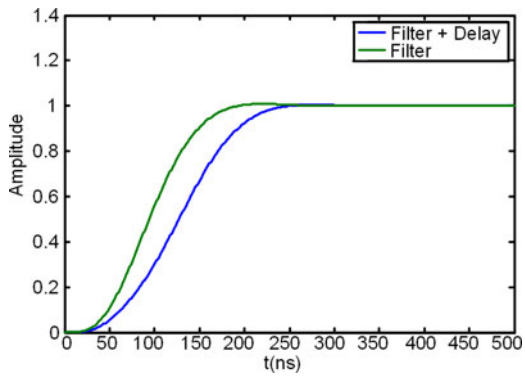


Fig. 10. Step responses of the combination of the delay and $G_{\mathrm{filter}}$ ($G_{\mathrm{two-phases}}$) and only $G_{\mathrm{filter}}$.

in Fig. 11, $N$ being the number of bits used to control the DPWM. The FPGA clock is used to generate four clocks at the switching frequency, each with 90° outphasing. The first one, labeled with 0 in Fig. 11, activates a set/reset flip-flop which drives the PWM signal. The duty cycle modulation is controlled by the reset signal of this flip-flop, which is a delayed version of the activation signal. This delay is controlled by the duty cycle command with two mechanisms. The first one is a coarse adjustment with steps of the 25% of the switching period. This

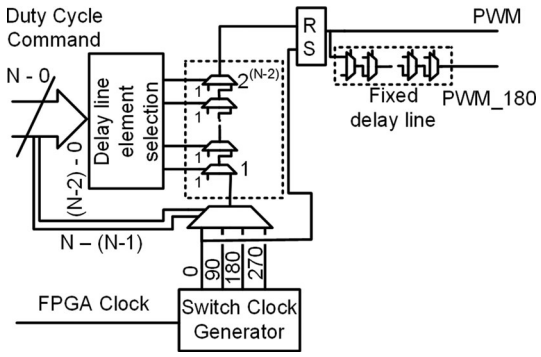


Fig. 11. Scheme of the PWM modulator.

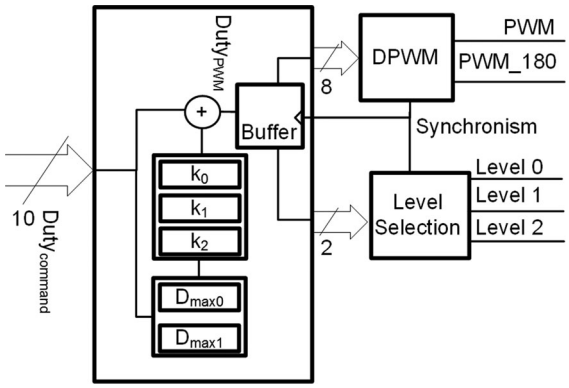


Fig. 12. Scheme of the control system of the floating-two phase.

delay is generated by the outphased switching frequency clocks and it is selected by the two most significant bits of the duty cycle command. The fine adjustment, controlled by the lower bits of the duty cycle command, is achieved by selecting how many delay cells the reset signal must pass through. The maximum delay achieved by this delay line is 25% of the switching period. The selection is done with a look up table stored in the FPGA memory. The cells are implemented using the inner multiplexers of the FPGA which are connected through the inner carry-chain lines, as in [20], without any manual routing. The PWM signal to control the other phase signal is generated by delaying the PWM signal with a fixed delay line, which delays the PWM signal by half switching period (then it is labeled in Fig. 11 as $\mathrm{PWM}_{180}$). This delay line is based on the same delay cells as the one used in the DPWM. The current design implements a 8 MHz, 10 bit resolution DPWM. The duty command is buffered in every switching cycle, that is, when the set signal turns ON.

In the case of the floating two-phase buck, the resolution is lowered to 8 bit because the two more significant bits will select the offset voltage of the switching stage. If the offset voltage change takes place when the duty cycle is above 50%, then the offset selection signal must be synchronized so the offset voltage occurs when signal $\mathrm{PWM}_{180}$ (see Figs. 11 and 12) is low. This allows a better transition between levels, since the offset does not change when one of the high-frequency switches is in on state. This problem only occurs with duty cycles above 50% because the delayed signal is ON when the next cycle of the leading signal starts a new cycle.

The way the offset voltage level changes is quite simple. The two most significant bits control the offset voltage level. When the duty cycle command reaches the duty cycle limit, a constant value is added to the duty cycle command so the lower bits change to the minimum duty cycle safely achievable while the two most significant bits changes to the next offset voltage level. For example, when the offset voltage level is set to 0 and the duty cycle command reaches the limit $D_{\max 0}$, then constant $k_1$ is added. Equation (8) describes this behavior

$$Duty_{PWM} = \begin{cases} Duty_{command} \\ \text{if } Duty_{command} \leq D_{\max 0} \\ Duty_{command} + k_1 \\ \text{if } D_{\max 0} < Duty_{command} \leq D_{\max 1} \end{cases} \tag{8}$$

Following the same process, when the duty cycle command reaches $D_{\max 1}$, a constant $k_2$ should be added to change to the highest offset level. Equation (9) extends (8) to this general case

$$Duty_{PWM} = \begin{cases} Duty_{command} \\ \text{if } Duty_{command} \leq D_{\max 0} \\ Duty_{command} + k_1 \\ \text{if } D_{\max 0} < Duty_{command} \leq D_{\max 1} \\ Duty_{command} + k_2 \\ \text{if } Duty_{command} > D_{\max 1} \end{cases} \tag{9}$$

Values $D_{\max 0}$, $D_{\max 1}$, $k_1$, and $k_2$ are selected in such a way that $Duty_{PWM}$ changes from the maximum value to the minimum one. In order to clarify this, let us suppose that the offset voltage is zero and the duty cycle command is the maximum one. The duty cycle command is described by the following equation:

$$Duty_{command} = [\text{“00”} D_{\max 1}] \tag{10}$$

“00” being the most significant bits of $Duty_{command}$. In this situation, no modification has to be done and $Duty_{PWM}$, which controls the actual switching signal of the HEMTs and the MOSFETs (see Fig. 12), is

$$Duty_{PWM} = Duty_{command} = [\text{“00”} D_{\max 1}]. \tag{11}$$

Suppose that the $Duty_{command}$ is increased in one unity

$$Duty_{command} = [\text{“00”} D_{\max 1}] + 1 \tag{12}$$

then constant $k_1$ must be added in such a way that the duty applied to the HEMTs $Duty_{PWM}$ is equal to the minimum duty cycle $D_{\min}$ and the offset voltage selection changes to $V_{g1}$

$$Duty_{PWM} = [\text{“00”} D_{\max 1}] + 1 + k_1 = [\text{“01”} D_{\min}]. \tag{13}$$

Then, the two most significant bits of $Duty_{PWM}$ control the offset level and the lower bits control the PWM modulator so a switching signal with the minimum duty cycle is generated. This allows the correct operation of the driver.

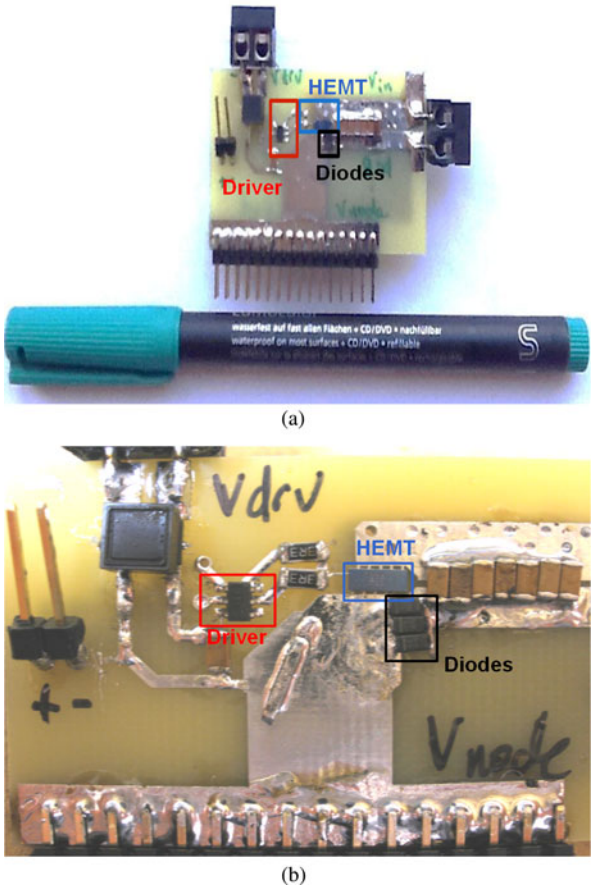


Fig. 13. (a) Picture of the switching cell, (b) Close Up.

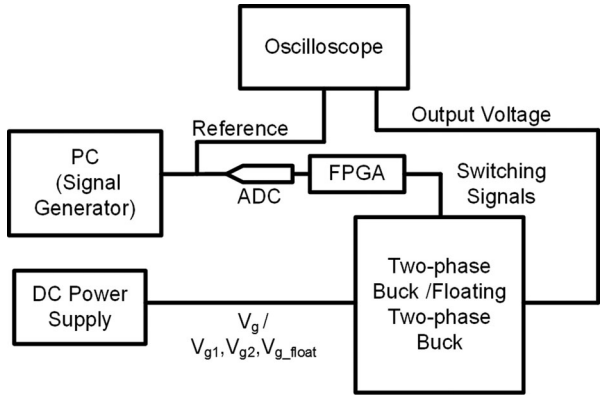


Fig. 14. Scheme of the experimental setup.

## V. Experimental Results

### A. Hardware Description

A prototype of the switching cells has been built using EPC2015 GaN HEMTs from Efficient Power Conversion Corporation. This is a normally off device. Three MSS1P3L from Vishay were placed in parallel acting as the freewheeling diode. The GaN transistor is driven by the LM5114 IC from Texas Instruments. The turn-off resistor is $1.8\ \Omega$ while the turn-on resistor has been removed and replaced with a short circuit. The gate of the transistor is driven using a 5-V square signal. The aforementioned resistor is placed to avoid overshoot and ringing, since the maximum gate voltage is 6 V. The control signals from the FPGA are translated to the driver using a IL610 digital isolator. The switching frequency is 8 MHz. Fig. 13(a) shows a picture of the switching cell with its main devices labeled (the HEMT, the driver, and the freewheeling diodes). A detailed closeup of the different elements of the switching cell can be seen in Fig. 13(b).

The offset voltage selection network is based around IPD135 MOSFETs driven with EL7156 drivers and IL610 digital isolators. These drivers use 12 V to drive the transistors of the voltage selection network.

The control is built using a Virtex-4 FPGA from Xilinx. The reference signal is taken with a THS1030 analog to digital converter. The FPGA will apply the switching signals with the correct duty cycle and outphasing to the two-phase buck converter. It also generates the control signals to the offset voltage selection network. The reference signal is generated by a PC with a digital to analog conversion card. The reference signal is generated in MATLAB and loaded to the card. Output voltage is sensed with a digital oscilloscope. The data sensed by the oscilloscope will be used to assess the quality of the signals as will be presented in Section V-D2. A schematic of the experimental setup can be seen in Fig. 14.

The output filter of both converters is a Bessel filter with a cutoff frequency of 3.5 MHz, adapted to a 5.2 $\Omega$ load. This is the resistive load that was used throughout the tests. The filter uses iron powder cores and Litz wire for the inductors, while the capacitors are a combination of low ESR ceramic capacitors. The values are the following: $L_{1a} = L_{1b} = 703$ nH, $C_2 = 8.6$ nF, $L_3 = 143.5$ nH and $C_4 = 1.86$ nF.

### B. Operation of the Two-Phase Buck

Two switching cell are combined with the filter to form a two-phase buck converter. The input voltage is 19 V and the switching frequency is set to 8 MHz. The adequate software is loaded in the FPGA so the duty cycles are generated following the signal sensed by the ADC. One of the main characteristics which are desirable for Envelope Modulators is a high slew rate. Fig. 15 shows a 10-V output voltage step performed by the two-phase buck. The slew rate achieved is around 100 $\mathrm{V}/\mu\mathrm{s}$. In Fig. 16, the two-phase buck converter is commanded to reproduce the envelope of a OFDM wireless communication standard. A dc offset has been added to it so that the output voltage does not reach zero. This offset does not affect the bandwidth of the signal that, according to Fig. 25, it is around 1.5 MHz. It can be seen how the output voltage mimics almost without error of the reference signal. The converter reaches an efficiency of around 79% while reproducing this waveform. The average output power in this situation is 13 W. This efficiency was obtained without taking into account the driver losses.

Defining the output voltage ripple in a dc/dc converter whose output voltage changes is a difficult task. However, it can be measured by demanding the converter to operate at a constant

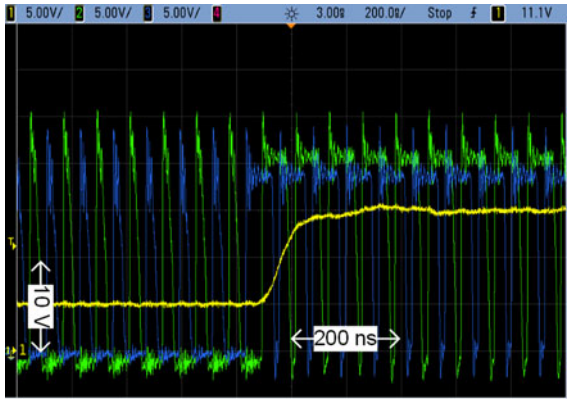


Fig. 15. Step response of the two-phase buck converter.

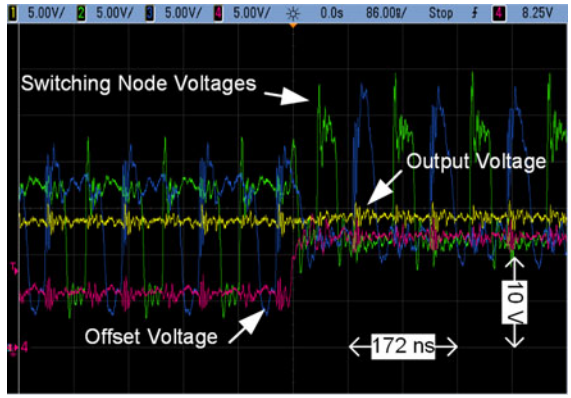


Fig. 18. Real offset level transition.

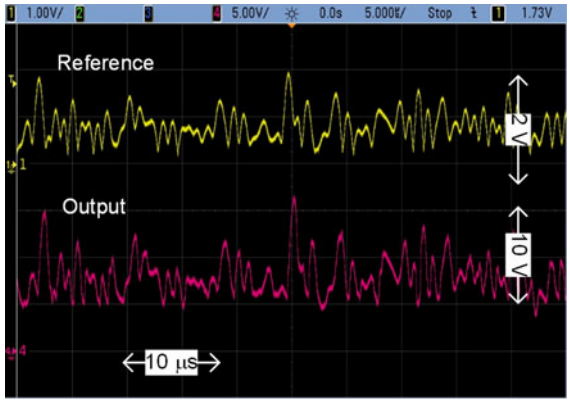


Fig. 16. Two-phase buck converter reproducing a OFDM standard envelope.

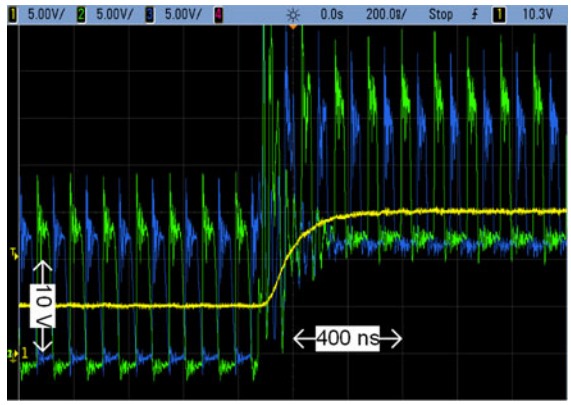


Fig. 19. Step response of the floating two-phase converter.

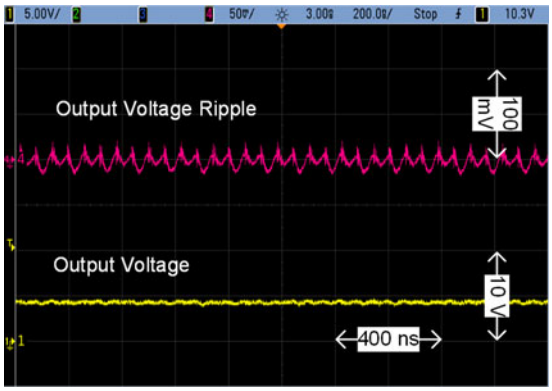


Fig. 17. Output voltage ripple at a 5-V dc output.

dc voltage. Results can be seen in Fig. 17 for an output voltage of 5 V. Measurements were carried out minimizing the ground loop of the probes of the oscilloscope, so very little electromagnetic noise was captured. The oscilloscope channel that senses the ripple was ac coupled so it removes the dc voltage. Results show a ripple with a peak amplitude around 20 mV. This value means a relative ripple around 0.4%. Such a low value is possible due to the fourth-order output filter and the multiphase operation. This measurement is taken far from the ripple cancellation points of the multiphase converter, which take place with a duty cycle equal to 0.5 for a two-phase converter [19].

### C. *Operation of the Floating Two-Phase Buck*

The same two switching cells were combined with the same filter and a Si MOSFET-based voltage selection network to build a floating two-phase converter. The software loaded to the FPGA will generate the proper duty cycle and voltage selection signals to track the voltage sensed by the ADC. The input voltage to the switching stage $V_{g\_\mathrm{float}}$ was set to 12.5 V, the other voltage levels were set to $V_{g1} = 6.5$ V and $V_{g1} = 12$ V. A detailed closeup of the transition between the offset voltages $V_{g1}$ to $V_{g2}$ can be seen in Fig. 18. The offset voltage, the switching voltages $V_{\mathrm{SW}1}$ and $V_{\mathrm{SW}2}$, and the output voltage are represented in it. As can be seen, it is very similar to the ideal waveforms represented in Fig. 8, although the noisy aspect is due to the connection of the oscilloscope probes. It can be seen how the offset voltage changes when all the switching voltages are low. Due to these transitions between levels, the converter can reproduce all the possible output voltages smoothly.

Fig. 19 shows the step response of the floating two-phase converter controlled to give an output voltage step of 10 V like in Section V-B. The slew rate achieved is also around 100 V/$\mu$s because it is mostly determined by the output filter which is the

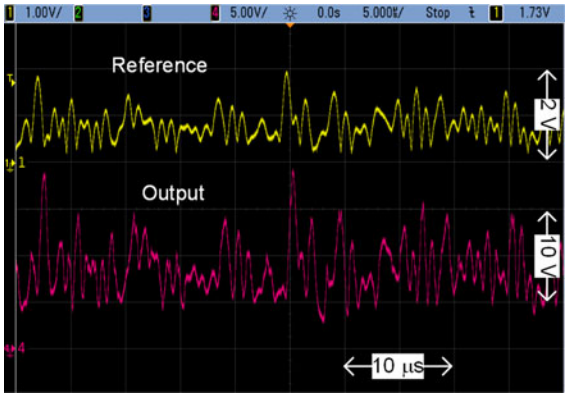


Fig. 20. Floating two-phase buck converter reproducing a OFDM envelope.

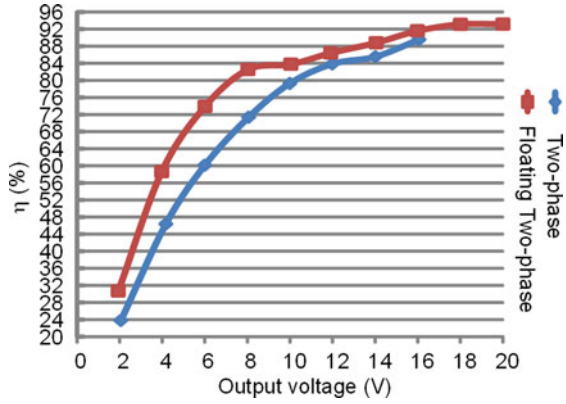


Fig. 22. Efficiency of the converters against output voltage.

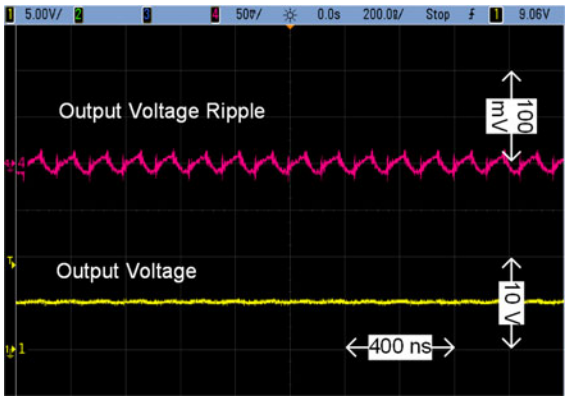


Fig. 21. Output voltage ripple at a 5-V dc output.

same in both converters. This step response involves a change in the offset level. It can be seen how the change in the offset is fast enough to reproduce the step.

The converter was commanded to track the same OFDM waveform described in Section V-B. Results can be seen in Fig. 20. The reproduction is very similar to the case of the two-phase buck converter. On the other hand, the efficiency in this case is higher, around 85%, with an average output power of 16 W. This measurements were also carried out without taking into account the drivers and the auxiliary circuitry. The efficiency measurement was carried out taking into account the power provided by the voltage sources $V_{\mathrm{g\_float}}$, $V_{g2}$, and $V_{g1}$.

Finally, the ripple was measured in the same dc point and with the same setup described in Section V-B. Results are shown in Fig. 21, in this case the ripple is lower, around 0.2%, due to the fact that the switching stage switches with lower input voltage ($V_{\mathrm{g\_float}} = 12.5$ V instead of $V_g = 19$).

### D. Comparison of the Two-Phase Buck and the Floating Two-Phase Buck

*1) Efficiency Comparative:* As has been explained in Sections V-B and V-C, both converters have almost the same dynamic characteristics, can reproduce the same waveforms and have very little output voltage ripple. In summary, both converters have desirable characteristics for the operation as envelope modulators. The main difference between them in terms of performance is their efficiency.

As in the case of the output voltage ripple, it is difficult to measure the efficiency using high speed varying waveforms as the ones used in the OFDM envelope test. Here, efficiency was measured at different constant dc points. Both converters were commanded to generate approximately the same dc voltage. The results are shown in Fig. 22. It can be seen how a higher output voltage means a higher efficiency in both cases. This is due to the fact that the low on resistance of the transistors plays a major role as long as the duty cycle becomes larger. The peak efficiency is achieved by the floating two-phase buck converter with an output voltage of 20 V, thus processing an output power of 77.7 W. In this case, the efficiency reaches around 93%. The two-phase converter maximum output voltage is 16 V (with an output power of 50 W), with an efficiency around 89%. It should be noted that the floating two-phase converter reaches 91% at this same point. Therefore, the floating-two phase buck converter is slightly more efficient than the two-phase buck, and can reach easily higher voltages. At low voltages, the efficiency of the floating two-phase converter is way higher than the two-phase buck. This is important since the most common value in an envelope will not be near the peak. If the output voltage of the converter remains near the low values most of the time the average efficiency will be lower with the two-phase buck converter than with the floating two-phase buck converter. However, the need of multiple power supplies, with $V_{\mathrm{g\_float}}$ isolated from the other ones, and a more complex control system are the main drawbacks of the latter one.

*2) Accuracy Comparative:* In order to compare how well does the output voltage match with the reference both converters were commanded to follow some communication envelopes. The experimental setup shown in Fig. 14 is used for this task. The reference signal sent to the converter is also displayed in the oscilloscope, as in Figs. 16 and 20. The oscilloscope was set to capture the data and then exported to MATLAB. Therefore, the sequences $r[n]$, which contains the samples of the reference, and $o[n]$, which are samples of the output voltage, are available for analysis. Once in MATLAB sequences were normalized, so

TABLE I
ERRORS MEASURED

| Converter | Signal | Mean of NMSE(%) | Standard Deviation of NMSE(%) |
|---|---|---|---|
| Two-phase buck | EDGE | 1 | 0.3 |
| | WCDMA+DC | 6.4 | 1.6 |
| | OFDM+DC | 3.8 | 0.41 |
| | OFDM | 8.2 | 0.7 |
| Floating two-phase buck | EDGE | 0.6 | 0.2 |
| | WCDMA+DC | 4.6 | 2.6 |
| | OFDM+DC | 1.7 | 0.13 |
| | OFDM | 4.9 | 1.5 |

the peak value in each one equals 1, obtaining the normalized sequences $r_n[n] = r[n]/\max(r[n])$ and $o_n[n] = o[n]/\max(o[n])$. Then, both sequences were aligned. Alignment is performed by means of finding how many samples is the output voltage signal $o_n[n]$ delayed from the reference signal $r_n[n]$. This is done by estimating the cross correlation $R_{r_n,o_n}[m]$

$$R_{r_n,o_n}[m] = \frac{1}{N}\begin{cases} \sum_{n=0}^{N-m-1} r_n[n+m]\cdot o_n^*[n] & \text{if } m \geq 0 \\ \sum_{n=0}^{N+m-1} r_n[n-m]\cdot o_n^*[n] & \text{if } m < 0 \end{cases} \quad (14)$$

where $N$ is the length of sequences $r_n[n]$ and $o_n[n]$ and $^*$ denotes the complex conjugate. (In MATLAB, (14) is computed using the instruction $xcorr(r\_n, o\_n, \text{'}biased\text{'})$). The delay between them is the sample $n_d$, where the cross correlation has a maximum. Therefore, the delayed version of the reference will be $r_{nd}[n] = r_n[n+n_d]$. Now, sequences $o_n[n]$ and $r_{nd}[n]$ have the same peak amplitude and are aligned, and therefore, they can be fairly compared. In order to do so, the energy of the error sequence $e[n] = o_n[n] - r_{nd}[n]$ is estimated and compared to the energy of the reference sequence $r_{nd}[n]$, thus obtaining the normalized mean square error (NMSE)

$$\text{NMSE} = \frac{\sum_{n=0}^{N} e^2[n]}{\sum_{n=0}^{N} r_{nd}^2[n]}. \quad (15)$$

The aforementioned process was carried out with both converters using the envelope of a OFDM signal with a 1.5-MHz RF bandwidth (the envelope has a higher frequency components), the same envelope of the OFDM signal but with a dc component (called OFDM+DC) to avoid the converter reaching 0 V, the envelope of a WCDMA signal used in 3G mobile communication standard with a dc offset (this signal will be called WCDMA+DC). Signals OFDM+DC and WCDMA+DC have the same minimum value. Finally, the envelope of the EDGE mobile communications standard is also used. The EDGE signal has the lowest bandwidth among the ones used in the test, thus the influence of the filter bandwidth should be smaller in this case. No dc component has been added to it since the EDGE envelope does not go near 0. The addition of a dc offset does not influence the bandwidth of the signals to reproduce.

The oscilloscope captures 1000 samples per screen, so a 5 $\mu$s/div time scale was selected for the OFDM signals, 2 $\mu$s/div for the WCDMA+DC test, and 20 $\mu$s/div for the EDGE. Time scale was selected to capture several transitions in the envelope waveform. Several screens were captured with different traces of the EDGE, WCDMA+DC, OFDM+DC, and OFDM signals. Results of evaluation of (15) were stored and then the mean and the standard deviation of the NMSEs calculated were obtained. These results can be found in Table I. Fig. 23 shows $r_{nd}[n]$ and $o_n[n]$ for a OFDM+DC example with the floating two-phase buck converter. It can be seen how similar are both sequences. The same sequences with the waveform WCDMA+DC are

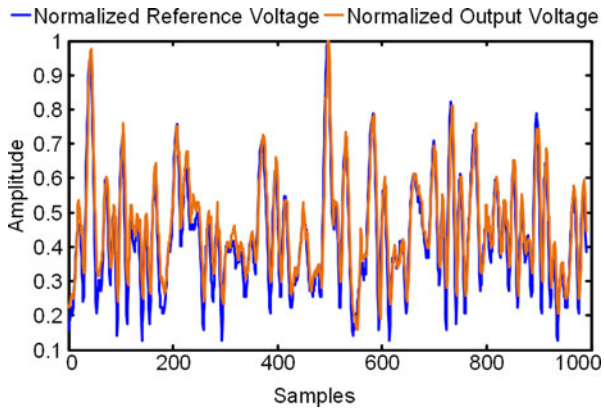


Fig. 23. Sequences $r_{nd}[n]$ and $o_n[n]$ for a OFDM example with the floating two-phase buck converter.

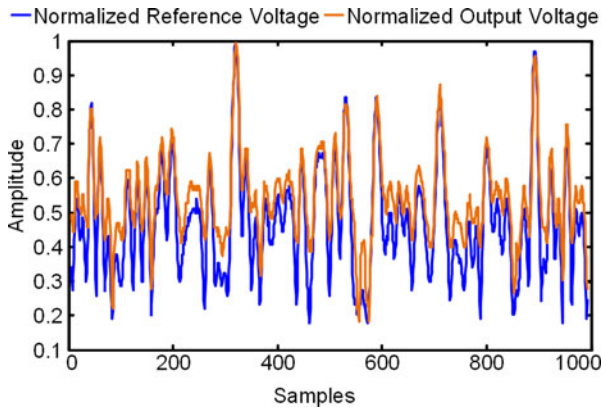


Fig. 24. Sequences $r_{nd}[n]$ and $o_n[n]$ for a WCDMA+DC example with the floating buck converter.

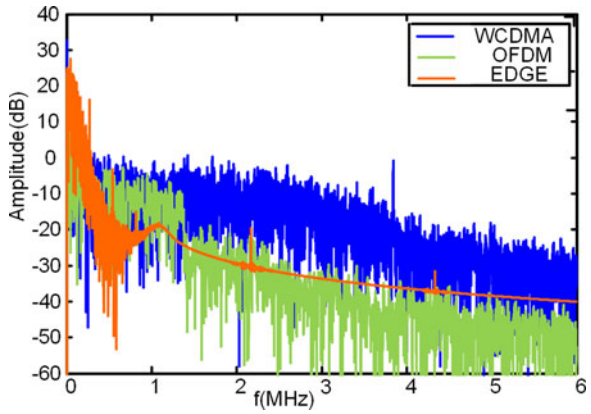


Fig. 25. Power spectral density of the envelopes used.

represented in Fig. 24. It can be seen how there are more differences than in the example represented in Fig. 23.

According to Table I, both converters show an average error well below 10% which means that they can track the signals very accurately. In the case of the two-phase buck, it is apparent how the error with the OFDM, OFDM+DC, and WCDMA+DC signals are higher than with the EDGE revealing that the signal bandwidth may be close to the cutoff frequency of the filter. Fig. 25 shows a power spectral density (estimated via periodogram) of the signals used in this test. It is apparent how a power drop appears around 500 kHz for the EDGE signal and 1.5 MHz in the OFDM case. For frequencies higher than this drop, the components carry little power and therefore they can be deprecated without contributing very much to the error measurements. There is no such a sharp transition for the WCDMA signal, but around 4 MHz for the WCDMA case there is a drop in the PSD. The highest NMSE appears with the WCDMA revealing that there are significant components above the cutoff frequency of the filter. However, due to its low power, the rejected components do not introduce a great error. Fig. 24 shows the normalized reference and output voltage with a WCDMA+DC waveform. Although they are very similar it is apparent that there is an error between them. In spite of this error, a good NMSE has been obtained.

By inspecting the mean NMSE, it is apparent how the lowest errors take place when the converter does not reach 0. This has two main reasons. The first one is that the converter does not work well with very small duty cycles. The second one is that a small error is more important when the output voltage is low than when the output voltage is high. Therefore, the NMSE is much more higher with the OFDM than with the OFDM+DC component, having both waveforms of the same bandwidth. For either waveform (OFDM and OFDM+DC), the error is smaller in the floating two-phase converter. This can be because the switched voltage is lower than in the two-phase buck. This means that an error in the PWM modulation means less error in the output voltage. The lower NMSE obtained with the floating two-phase converter also means that the error that the offset level transition may cause have little importance in the overall error performance.

It is important to note that no predistortion of the reference signal has been applied to any of the converters. The duty cycle fed to the PWM modulator is just the amplitude of the reference signal. What has been analyzed in this section is how well the converters are capable to reproduce a complex waveform. Results of these test show that both converters perform really well in this task with a very little error. However, the influence of this error in the final RF waveform is a question that must be answered by the designers of the whole envelope tracking system.

## VI. Conclusion

This paper shows different implementations of dc/dc converters to be used as envelope modulators in envelope tracking applications. These dc/dc converters derived from the buck converter and use the high frequency switching capabilities that are enabled by the use of GaN transistors. This allows to achieve a wide bandwidth with good efficiency, so the use of them as envelope modulators, alone or in combination with linear stages, can be feasible.

Between the two topologies presented here, the floating two-phase buck converter presents higher efficiency at the cost of a slightly more complex hardware and control. Its main drawback is the necessity of multiple power supplies to generate the offset levels. On the other hand, the two-phase buck converter is more simple from the hardware and software point of view.

In summary, these converters are capable to deal with the envelope of a OFDM signal with a good efficiency. Results presented in Section V-D2) show that both converters can reproduce real complex signals used in communications (OFDM, EDGE, WCDMA) with very little error.

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