Letters

An Enhanced SVM Method to Drive Matrix Converters for Zero Common-Mode Voltage

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***Abstract*—This paper presents an enhanced space vector modulation (SVM) method to drive matrix converters (MCs) with zero common-mode voltage by using the rotating vectors, which are not used in the traditional SVM for MCs. The reference output voltage vector is generated by a combination of the closer rotating vectors in order to minimize the output distortion. Explicit equations are used to develop the switching patterns so that the proposed SVM method can achieve full control of the output voltage vector and input current phase angle with good performance of the input/output current waveforms. Together with the theoretical analysis, the experimental results are provided to validate the feasibility of the proposed method.**

***Index Terms*—Common-mode voltage, matrix converter, rotating vector, space vector modulation.**

I. Introduction

In recent years, the matrix converter (MC) has been attracting considerable attention from many researchers due to its significant advantages such as its bidirectional power flow capability, sinusoidal input/output waveforms, a controllable input power factor, lightweight design, and long life compared to the back-to-back converter with the equivalent power ratings [1]. In spite of the MC's outstanding features, it has problems to be solved such as its input filter, complicated commutation, control algorithm under unbalanced input voltages, and common-mode voltage (CMV) [2]. Among those problems, the CMV with a high dv/dt and high switching frequency, which is known as the main source of the shaft voltage, leakage current, and bearing current damage, not only harms the motor lifetime, but also degrades the reliability of the electrical system [3]. According to a number of surveys, bearing current damage causes 30% of all motor failures [4]. Furthermore, the leakage current creates a noise problem and electromagnetic interference (EMI), which affect the other electronic equipment near the power converter [5]. Therefore, it is important to develop techniques to mitigate the CMV in the MC.

Fig. 1 shows a common topology of the MC. There are 27 possible switching configurations (SCs) to satisfy the two main rules in MC: 1) the input phases should never be short-circuited, and 2) the output phases should not be unconnected. These SCs are categorized into three groups as listed in Table I. Many researchers have focused on modulation methods as well as CMV reduction methods for the MC by using the first 21 SCs in Table I. The peak value of CMV has been reduced to 42% with direct space vector modulation (SVM) method by replacing the zero space vectors with active vectors [6] or rotating vectors [7], and by using lower input line-to-line voltages [8]. On the other hand, an indirect SVM method was proposed to reduce the CMV peak value to 34% by placing the zero vectors in the center of the sampling period [9], while a predictive current control strategy has suppressed the rms value of the CMV to 70% by adding a new quality function [10]. Until now, all modulation methods in the MC can mitigate the CMV peak value to 34%, 42% or the rms value to 70%.

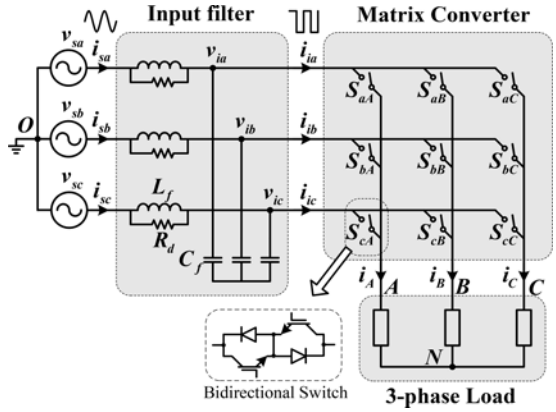

Fig. 1. Common three-phase to three-phase MC configuration.

In order to achieve the zero CMV, this paper proposes a new SVM method by using only rotating vectors. It is not easy to create a repetitive pattern from the rotating vectors in Group III of Table I since their angular positions change according to the input voltage. Due to this difficulty, the rotating vectors are not usually used in modulation methods [7]. This paper focuses on how to apply the rotating vectors to drive the MC and suggests a repetitive switching pattern for a new SVM method that uses only these rotating vectors. With this repetitive pattern, the new SVM method can achieve full control of output voltage vector and input current phase angle which determines the input power factor of the MC. The proposed SVM method can generate good performance in terms of the input/output current waveforms and

Manuscript received June 14, 2014; revised July 19, 2014; accepted August 2, 2014. Date of publication August 15, 2014; date of current version November 3, 2014. This work was supported by the National Foundation of Korea under Grant 2013R1A2A2A01016398.

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Digital Object Identifier 10.1109/TPEL.2014.2348019

TABLE I
POSSIBLE SCS IN MC

	Switching Configuration		Output Voltage		Input Current		CMV (peak)
	No	A B C	V_o	α_o	I_i	β_i	V_{cm}
Group I	$+1$	a b b	$2v_{ab}/3$	0	$2i_A/\sqrt{3}$	$-\pi/6$	$V_i/\sqrt{3}$
	-1	b a a	$-2v_{ab}/3$	0	$-2i_A/\sqrt{3}$	$-\pi/6$	
	$+2$	b c c	$2v_{bc}/3$	0	$2i_A/\sqrt{3}$	$\pi/2$	
	-2	c b b	$-2v_{bc}/3$	0	$-2i_A/\sqrt{3}$	$\pi/2$	
	$+3$	c a a	$2v_{ca}/3$	0	$2i_A/\sqrt{3}$	$7\pi/6$	
	-3	a c c	$-2v_{ca}/3$	0	$-2i_A/\sqrt{3}$	$7\pi/6$	
	$+4$	b a b	$2v_{ab}/3$	$2\pi/3$	$2i_B/\sqrt{3}$	$-\pi/6$	
	-4	a b a	$-2v_{ab}/3$	$2\pi/3$	$-2i_B/\sqrt{3}$	$-\pi/6$	
	$+5$	c b c	$2v_{bc}/3$	$2\pi/3$	$2i_B/\sqrt{3}$	$\pi/2$	
	-5	b c b	$-2v_{bc}/3$	$2\pi/3$	$-2i_B/\sqrt{3}$	$\pi/2$	
	$+6$	a c a	$2v_{ca}/3$	$2\pi/3$	$2i_B/\sqrt{3}$	$7\pi/6$	
	-6	c a c	$-2v_{ca}/3$	$2\pi/3$	$-2i_B/\sqrt{3}$	$7\pi/6$	
	$+7$	b b a	$2v_{ab}/3$	$4\pi/3$	$2i_C/\sqrt{3}$	$-\pi/6$	
	-7	a a b	$-2v_{ab}/3$	$4\pi/3$	$-2i_C/\sqrt{3}$	$-\pi/6$	
	$+8$	c c b	$2v_{bc}/3$	$4\pi/3$	$2i_C/\sqrt{3}$	$\pi/2$	
	-8	b b c	$-2v_{bc}/3$	$4\pi/3$	$-2i_C/\sqrt{3}$	$\pi/2$	
	$+9$	a a c	$2v_{ca}/3$	$4\pi/3$	$2i_C/\sqrt{3}$	$7\pi/6$	
	-9	c c a	$-2v_{ca}/3$	$4\pi/3$	$-2i_C/\sqrt{3}$	$7\pi/6$	
Group II	0_a	a a a	0	x	0	x	V_i
	0_b	b b b	0	x	0	x	
	0_c	c c c	0	x	0	x	
Group III	r_1	a b c	V_i	α_i	I_o	β_o	0
	r_2	a c b	V_i	$-\alpha_i$	I_o	$-\beta_o$	
	r_3	c a b	V_i	$2\pi/3+\alpha_i$	I_o	$-2\pi/3+\beta_o$	
	r_4	b a c	V_i	$2\pi/3-\alpha_i$	I_o	$2\pi/3-\beta_o$	
	r_5	b c a	V_i	$-2\pi/3+\alpha_i$	I_o	$2\pi/3+\beta_o$	
	r_6	c b a	V_i	$-2\pi/3-\alpha_i$	I_o	$-2\pi/3-\beta_o$	

solves the CMV problem in the MCs. The feasibility of the proposed SVM method is experimentally verified.

II. PROPOSED SVM METHOD

In balanced operation, the instantaneous source voltages are defined as follows:

$$\mathbf{v_s} = \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} = V_s \begin{bmatrix} \cos(\omega_i t) \\ \cos(\omega_i t - 2\pi/3) \\ \cos(\omega_i t + 2\pi/3) \end{bmatrix} \quad (1)$$

where V_s and ω_i are the amplitude and the angular frequency of the source voltage, respectively.

With the relevant symbols shown in Fig. 1, the space vector of the input and output voltages, the input and output currents can be defined, respectively, by the following equations:

$$\vec{v}_i = 2(v_{ia} + v_{ib}e^{j2\pi/3} + v_{ic}e^{j4\pi/3})/3 = V_i e^{j\alpha_i} \quad (2)$$

$$\vec{v}_o = 2(v_A + v_B e^{j2\pi/3} + v_C e^{j4\pi/3})/3 = V_o e^{j\alpha_o} \quad (3)$$

$$\vec{i}_i = 2(i_{ia} + i_{ib}e^{j2\pi/3} + i_{ic}e^{j4\pi/3})/3 = I_i e^{j\beta_i} \quad (4)$$

$$\vec{i}_o = 2(i_A + i_B e^{j2\pi/3} + i_C e^{j4\pi/3})/3 = I_o e^{j\beta_o}. \quad (5)$$

As shown in Table I, the SCs in Group III always generate zero CMV. In order to eliminate the CMV for the MC, a novel SVM method to drive the MC is developed by using only the SCs in Group III.

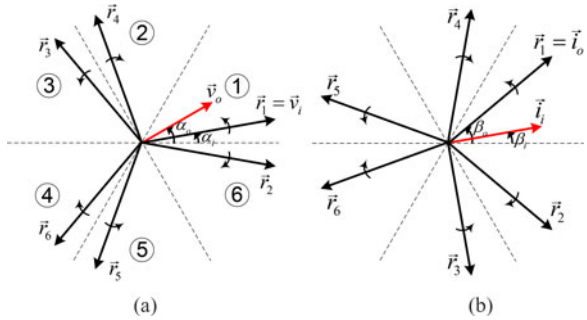

Fig. 2. (a) Rotating voltage vectors. (b) Rotating current vectors in MC.

A. Selection of SCs

The rotating vectors are classified into anticlockwise-rotating (i.e., $\vec{r}_1$, $\vec{r}_3$, $\vec{r}_5$) and clockwise-rotating (i.e., $\vec{r}_2$, $\vec{r}_4$, $\vec{r}_6$) vector groups as shown in Fig. 2(a) and (b). The $\alpha\beta$ plane is divided into six sectors for the input and output voltage vectors. The following analysis presumes that five rotating vectors are utilized to control output voltage and input current vectors at the same time. Five vectors are selected among six rotating vectors, but the farthest one from the reference output voltage vector is excluded in order to minimize the output distortion. For example, if the input voltage vector and output voltage vector are both lying in sector 1, the five SCs r_1, r_2, r_3,r_4, and r_5 are chosen in this case. This selection does not depend on the relation between the input voltage phase angle α_i and the output voltage phase angle α_o as long as both the input voltage vector and the

TABLE II
SELECTED SCS FOR EACH COMBINATION OF OUTPUT VOLTAGE AND INPUT VOLTAGE SECTORS IN THE PROPOSED SVM METHOD

		Input Voltage Vector Sector					
		1	2	3	4	5	6
Output	1	$r_1\ r_2\ r_3\ r_4\ r_5$	$r_4\ r_5\ r_6\ r_1\ r_2$	$r_5\ r_4\ r_1\ r_6\ r_3$	$r_6\ r_3\ r_2\ r_5\ r_4$	$r_3\ r_6\ r_5\ r_2\ r_1$	$r_2\ r_1\ r_4\ r_3\ r_6$
Voltage	2	$r_4\ r_3\ r_2\ r_1\ r_6$	$r_1\ r_6\ r_5\ r_4\ r_3$	$r_6\ r_1\ r_4\ r_5\ r_2$	$r_5\ r_2\ r_3\ r_6\ r_1$	$r_2\ r_5\ r_6\ r_3\ r_4$	$r_3\ r_4\ r_1\ r_2\ r_5$
Vector	3	$r_3\ r_4\ r_5\ r_6\ r_1$	$r_6\ r_1\ r_2\ r_3\ r_4$	$r_1\ r_6\ r_3\ r_2\ r_5$	$r_2\ r_5\ r_4\ r_1\ r_6$	$r_5\ r_2\ r_1\ r_4\ r_3$	$r_4\ r_3\ r_6\ r_5\ r_2$
Sector	4	$r_6\ r_5\ r_4\ r_3\ r_2$	$r_3\ r_2\ r_1\ r_6\ r_5$	$r_2\ r_3\ r_6\ r_1\ r_4$	$r_1\ r_4\ r_5\ r_2\ r_3$	$r_4\ r_1\ r_2\ r_5\ r_6$	$r_5\ r_6\ r_3\ r_4\ r_1$
	5	$r_5\ r_6\ r_1\ r_2\ r_3$	$r_2\ r_3\ r_4\ r_5\ r_6$	$r_3\ r_2\ r_5\ r_4\ r_1$	$r_4\ r_1\ r_6\ r_3\ r_2$	$r_1\ r_4\ r_3\ r_6\ r_5$	$r_6\ r_5\ r_2\ r_1\ r_4$
	6	$r_2\ r_1\ r_6\ r_5\ r_4$	$r_5\ r_4\ r_3 r_2\ r_1$	$r_4\ r_5\ r_2\ r_3\ r_6$	$r_3\ r_6\ r_1\ r_4\ r_5$	$r_6\ r_3\ r_4\ r_1\ r_2$	$r_1\ r_2\ r_5\ r_6\ r_3$
Duty cycles		$d_I\ d_{II}\ d_{III}\ d_{IV}\ d_V$	$d_I\ d_{II}\ d_{III}\ d_{IV}\ d_V$	$d_I\ d_{II}\ d_{III}\ d_{IV}\ d_V$	$d_I\ d_{II}\ d_{III}\ d_{IV}\ d_V$	$d_I\ d_{II}\ d_{III}\ d_{IV}\ d_V$	$d_I\ d_{II}\ d_{III}\ d_{IV}\ d_V$

output voltage vector are located in sector 1. In a similar way, the selected rotating vectors and the corresponding duty cycles are summarized in Table II for any combination of input voltage and output voltage sectors.

B. Calculation of Duty Cycles

In order to select the SCs to generate the desired output voltage vector, the input voltage and output voltage sectors should be known, where the symbols k_i ($k_i = 1, \ldots, 6$) and k_o ($k_o = 1, \ldots, 6$) represent the input voltage sector and the output voltage sector, respectively. For the case in which $k_i = 1$, $k_o = 1$ ($0 \le \alpha_i < \pi/3$ and $0 \le \alpha_o < \pi/3$), the selected SCs are r_1, r_2, r_3, r_4, and r_5, and their duty cycles are sequentially assigned one by one to each switching vector as d_I, d_{II}, d_{III}, d_{IV}, and d_V as shown in Table II. In order to find the duty cycles, the following five constraint equations are used:

$$d_I + d_{II} + d_{III} + d_{IV} + d_V = 1 \tag{6}$$

$$\begin{aligned} &d_I \cos(\alpha_i - \alpha_o) + d_{II} \cos(-\alpha_i - \alpha_o) \\ &\quad + d_{III} \cos(2\pi/3 + \alpha_i - \alpha_o) \\ &\quad + d_{IV} \cos(2\pi/3 - \alpha_i - \alpha_o) \\ &\quad + d_V \cos(-2\pi/3 + \alpha_i - \alpha_o) = q \end{aligned} \tag{7}$$

$$\begin{aligned} &d_I \sin(\alpha_i - \alpha_o) + d_{II} \sin(-\alpha_i - \alpha_o) \\ &\quad + d_{III} \sin(2\pi/3 + \alpha_i - \alpha_o) \\ &\quad + d_{IV} \sin(2\pi/3 - \alpha_i - \alpha_o) \\ &\quad + d_V \sin(-2\pi/3 + \alpha_i - \alpha_o) = 0 \end{aligned} \tag{8}$$

$$\begin{aligned} &d_I \cos\beta_i - d_{II} \cos(-\beta_i) + d_{III} \cos(2\pi/3 + \beta_i) \\ &\quad - d_{IV} \cos(2\pi/3 - \beta_i) + d_V \cos(-2\pi/3 + \beta_i) = 0 \end{aligned} \tag{9}$$

$$\begin{aligned} &d_I \sin\beta_i - d_{II} \sin(-\beta_i) + d_{III} \sin(2\pi/3 + \beta_i) \\ &\quad - d_{IV} \sin(2\pi/3 - \beta_i) + d_V \sin(-2\pi/3 + \beta_i) = 0 \end{aligned} \tag{10}$$

where $q = V_o/V_i$ is the voltage transfer ratio.

Equation (6) is clearly related to the completion of the sampling period. Equations (7) and (8) are required to control the reference output voltage vector in its direction and the perpendicular direction, respectively. Equations (9) and (10) are written so as to control the input power factor, and are explained in the Appendix.

From (6) to (10), the duty cycles are obtained as follows:

$$\begin{aligned} d_I = \frac{1}{3}\Big[1 - 2q\frac{\cos(\pi/3 - \alpha_o)\cos\beta_i}{\cos\delta_i} \\ + \sqrt{3}q\frac{\sin(2\pi/3 - \alpha_o + \beta_i)}{\cos\delta_i}\Big] \end{aligned} \tag{11}$$

$$d_{II} = \frac{q}{\sqrt{3}} \times \frac{\sin(2\pi/3 - \alpha_o - \beta_i)}{\cos\delta_i} \tag{12}$$

$$\begin{aligned} d_{III} = \frac{1}{3}\Big[1 - 2q\frac{\cos(\pi/3 - \alpha_o)\cos\beta_i}{\cos\delta_i} \\ + \sqrt{3}q\frac{\sin(\alpha_o - \beta_i)}{\cos\delta_i}\Big] \end{aligned} \tag{13}$$

$$d_{IV} = \frac{q}{\sqrt{3}} \times \frac{\sin(\alpha_o + \beta_i)}{\cos\delta_i} \tag{14}$$

$$d_V = \frac{1}{3}\left[1 - 2q\frac{\cos(\pi/3 - \alpha_o)\cos\beta_i}{\cos\delta_i}\right] \tag{15}$$

where $\delta_i = \alpha_i - \beta_i$ is the input current displacement angle.

In order to minimize the number of commutations in each sampling period and the output distortion, the SCs in the proposed SVM method are arranged symmetrically as shown in Fig. 3.

Considering all 36 possible combinations of input voltage and output voltage sectors, the duty cycles in Table II are expressed generally as follows:

$$\begin{aligned} d_I = \frac{1}{3}\Big[1 - 2q\frac{\cos(\pi/3 - \tilde{\alpha}_o)\cos\tilde{\beta}_i}{\cos\delta_i} \\ + \sqrt{3}q\frac{\sin(2\pi/3 - \tilde{\alpha}_o + \tilde{\beta}_i)}{\cos\delta_i}\Big] \end{aligned} \tag{16}$$

$$d_{II} = \frac{q}{\sqrt{3}} \times \frac{\sin(2\pi/3 - \tilde{\alpha}_o - \tilde{\beta}_i)}{\cos\delta_i} \tag{17}$$

$$\begin{aligned} d_{III} = \frac{1}{3}\Big[1 - 2q\frac{\cos(\pi/3 - \tilde{\alpha}_o)\cos\tilde{\beta}_i}{\cos\delta_i} \\ + \sqrt{3}q\frac{\sin(\tilde{\alpha}_o - \tilde{\beta}_i)}{\cos\delta_i}\Big] \end{aligned} \tag{18}$$

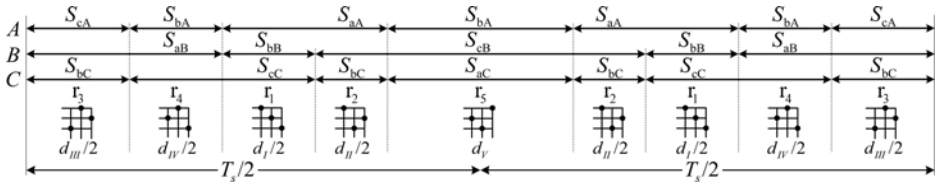

Fig. 3. Switching pattern for input voltage sector 1 and output voltage sector 1 of the proposed SVM method.

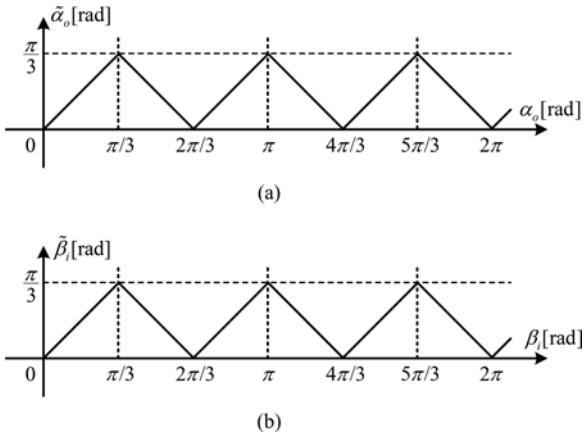

Fig. 4. (a) Relation between $\tilde{\alpha}_o$ and α_o. (b) Relation between $\tilde{\beta}_i$ and β_i in the proposed SVM method.

$$d_{IV} = \frac{q}{\sqrt{3}} \times \frac{\sin(\tilde{\alpha}_o + \tilde{\beta}_i)}{\cos\delta_i} \tag{19}$$

$$d_V = \frac{1}{3}\left[1 - 2q\frac{\cos(\pi/3 - \tilde{\alpha}_o)\cos\tilde{\beta}_i}{\cos\delta_i}\right] \tag{20}$$

where $\tilde{\alpha}_o$ and $\tilde{\beta}_i$ are defined by (21) and (22), respectively

$$k_1 = (\text{int})(k_o \times 0.5);\ \tilde{\alpha}_o = (-1)^{k_o}(k_1 \times 2\pi/3 - \alpha_o) \tag{21}$$

$$k_2 = (\text{int})(k_i \times 0.5);\ \tilde{\beta}_i = (-1)^{k_i}(k_2 \times 2\pi/3 - \beta_i) \tag{22}$$

where the (int) function rounds down a number to the nearest integer.

From (21) and (22), the patterns of $\tilde{\alpha}_o$ and $\tilde{\beta}_i$ in the proposed SVM method are plotted in Fig. 4(a) and (b), respectively. The proposed SVM method can provide a repetitive pattern to drive the MCs by using the rotating vectors shown in Table II.

All duty cycles must be positive and lower than unity:

$$0 \le d_N \le 1, \quad N = I, \ldots, V. \tag{23}$$

Therefore, the limit of the voltage transfer ratio q is obtained from all of the duty cycles in (16)–(20) to satisfy (23)

$$q \le \frac{1}{2}\cos\delta_i. \tag{24}$$

III. Experimental Results

In order to evaluate the control strategy of the proposed modulation method, a prototype of a three-phase to three-phase MC with a passive RL load is considered. The power stage is developed by using eighteen discrete IGBTs (IRG4PF50WD). The digital control system is implemented with fixed-point digital signal processors (TMS320F2812) and a complex programmable logic device (EPM7128SLC84-15). The control scheme of the proposed SVM method is the same as the general control scheme in [11] except the modulation method. The parameters in the experiment are as follows:

1) three-phase power supply: 100 V/60 Hz (phase-to-neutral);
2) input filter: $L_f = 1.4$ mH, $C_f = 22$ μF, $R_d = 30$ Ω;
3) three-phase load: $R = 25$ Ω, $L = 20$ mH;
4) output frequency: $f_o = 50$ Hz;
5) voltage transfer ratio: $q = 0.45$;
6) input power factor of MC: $\cos\delta_i = 1$;
7) PWM sampling frequency: $f_s = 10$ kHz ($T_s = 100$ μs).

Figs. 5 and 6 show the input voltage/input current and output line-to-line voltage/three-phase output current waveforms, respectively, at $f_o = 50$ Hz, $q = 0.45$ with the proposed SVM method. The filtered input current has a small ripple due to the small damping resistance in the input filter circuit. The input current leads the supply phase voltage due to the LC input filter.

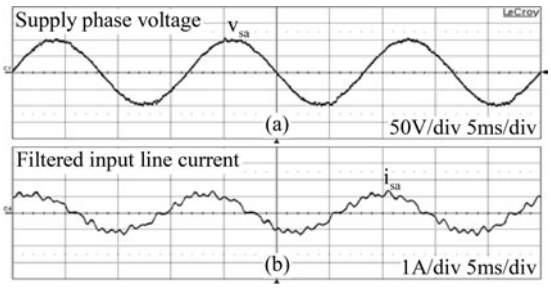

Fig. 5. (a) Supply phase voltage. (b) Filtered input line current with the proposed SVM method at $f_o = 50$ Hz, $q = 0.45$.

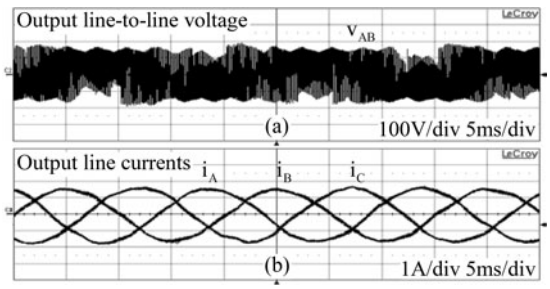

Fig. 6. (a) Output line-to-line voltage. (b) Three-phase output line current with the proposed SVM method at $f_o = 50$ Hz, $q = 0.45$.

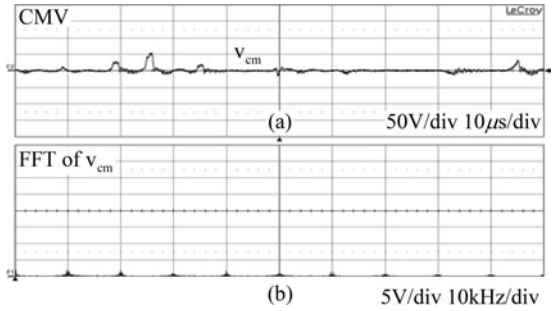

Fig. 7. (a) Waveform of CMV in one sampling period. (b) FFT of CMV with the proposed SVM method at $f_o = 50$ Hz, $q = 0.45$.

With the duty cycles in (16)–(20) for the rotating vectors, the proposed SVM can overcome the nonlinear regulator problem which appears in the conventional SVM method [12].

As can be seen in Fig. 7, the CMV is nearly zero, except for some noise resulting from the commutation. Therefore, the proposed SVM can help to effectively reduce the bearing current damage, leakage current, and the resultant EMI caused by the CMV.

IV. Conclusion

We have developed an enhanced SVM method to drive MCs with zero CMV by using rotating vectors to synthesize the reference output voltage vector and to control the input current phase angle. The explicit equations to calculate the duty cycles of the rotating vectors and the repetitive switching pattern for a new SVM method have been provided. The feasibility of the proposed SVM for zero CMV is experimentally demonstrated with good performance of the input/output waveforms.

Besides the well-known advantages of the MC such as the bidirectional power flow capability, compact design, and long life due to the lack of a bulky storage capacitor, we have added one more advantage, i.e., zero CMV for the MCs without any additional hardware, which is not achieved in the back-to-back converter, multilevel inverter, or even an indirect MC due to the dc-link voltage. Since the proposed SVM method in this paper uses only the rotating vectors to control the MCs, the voltage transfer ratio is limited from 0 to 0.5. However, the combination of all SCs in Table I promises new SVM methods with more advantages in the near future.

Appendix

Basically, the input voltage phase angle is obtained by measuring the source voltages. Hence, the control of the input power factor can be achieved by controlling the phase angle β_i of the input current vector. In order to control the input current phase angle, the following equation should be satisfied:

$$\begin{aligned} &d_I \sin(\beta_o - \beta_i) + d_{II} \sin(-\beta_o - \beta_i) \\ &\quad + d_{III} \sin(-2\pi/3 + \beta_o - \beta_i) \\ &\quad + d_{IV} \sin(2\pi/3 - \beta_o - \beta_i) \\ &\quad + d_V \sin(2\pi/3 + \beta_o - \beta_i) = 0. \end{aligned} \tag{A1}$$

After some manipulation, it is possible to obtain the following equation:

$$\sin\beta_o . M_1(\beta_i) - \cos\beta_o . M_2(\beta_i) = 0 \tag{A2}$$

where

$$\begin{aligned} M_1(\beta_i) = \; &[d_I \cos\beta_i - d_{II} \cos(-\beta_i) \\ &+ d_{III} \cos(2\pi/3 + \beta_i) \\ &- d_{IV} \cos(2\pi/3 - \beta_i) \\ &+ d_V \cos(-2\pi/3 + \beta_i)] \end{aligned} \tag{A3}$$

$$\begin{aligned} M_2(\beta_i) = \; &[d_I \sin\beta_i - d_{II} \sin(-\beta_i) \\ &+ d_{III} \sin(2\pi/3 + \beta_i) - d_{IV} \sin(2\pi/3 - \beta_i) \\ &+ d_V \sin(-2\pi/3 + \beta_i)]. \end{aligned} \tag{A4}$$

Since the phase angle of the input current vector β_i is independent of the phase angle of the output current vector β_o, (A5) and (A6) should be satisfied to hold (A2) true for any value of β_o

$$M_1(\beta_i) = 0 \tag{A5}$$

$$M_2(\beta_i) = 0. \tag{A6}$$

Thus, we can say that (A5) and (A6) prove (9) and (10), respectively.

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