Letters

A Novel Accurate Primary-Side Control (PSC) Method for Half-Bridge (HB) *LLC* Converter

Jae-Bum Lee, Chong-Eun Kim, Jae-Kuk Kim, Jae-Hyun Kim, Sang-Cheol Moon, and Gun-Woo Moon

***Abstract*—Recently, several researches have been progressed on the primary-side control (PSC) methods which decrease the size and cost of the control stage. However, most of the researches have been applied to the flyback converter, and they have some challenges in applying them to the half-bridge (HB) *LLC* converter due to the large voltage across the secondary leakage inductor of the transformer. In this letter, a new PSC method for the HB *LLC* converter is proposed to obtain accurate output voltage. In the proposed method, the output voltage is regulated by obtaining the voltage across the primary side of the transformer when the external resonant inductor voltage becomes 0 V. At this time, since the voltage across the transformer secondary leakage inductor is small, the proposed method can accurately regulate the output voltage. A 400 V input and 20 V/85 W output laboratory prototype is built and tested to verify the effectiveness of the proposed PSC method.**

***Index Terms*—Half-bridge (HB) *LLC* converter, high-power adaptor applications, primary-side control (PSC).**

I. Introduction

RECENTLY, as the portable data-processing equipment such as the mobile phones, tablet PCs, and laptop computers has grown explosively and their energy consumption has also been increased, the energy saving has been an essential issue. Meanwhile, since the consumers tend to prefer a compact device, the manufacturers make an effort to minimize its size. For these reasons, the power systems for those devices have been required to be small size and achieve a high efficiency. Among the power systems, the adaptors for the laptop computers are strongly required to have a high power density in excess of 5 W/in^3 and average efficiency above 85% because of the energy efficiency standards like the energy star program.

At a high power level above 70 W for the laptop computers, the conventional adaptors have been developed based on two-stage structure in Fig. 1 to comply with the IEC 1000-3-2 harmonic standards and obtain a high efficiency [1], [2]. This two-stage configuration consists of the power factor correction (PFC) stage and dc/dc stage. Since the boost converter has many advantages such as a direct control of the line current and low input current ripple, it has been widely utilized in the PFC stage [3], [4]. For the dc/dc stage, the flyback converter is one of the suitable candidates due to simple PWM control method and low component count. However, high voltage stress on the primary switch and hard switching cause low efficiency. Moreover, a large transformer dc-offset current increases the converter size. To overcome these drawbacks, the conventional half-bridge (HB) *LLC* converter can be a good solution because of its simple structure and low voltage stresses on the primary switches [5]–[7]. Additionally, since the zero-voltage switching (ZVS) of the primary switches and zero-current switching of the secondary switches can be achieved under the entire load conditions, the switching loss can be decreased. Therefore, it can operate at a high switching frequency, and the size of reactive components can be reduced [8].

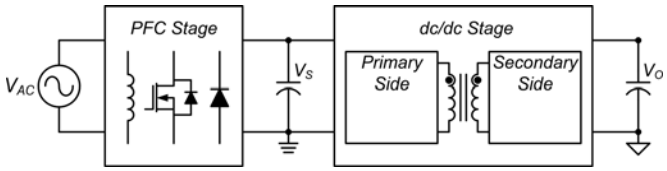

Fig. 1. Block diagram of two-stage structure for high-power applications.

The HB *LLC* converter is generally implemented by the secondary-side control (SSC), using a HB *LLC* controller in the primary side, operational amplifier in the secondary side, and photocoupler in between the primary and secondary sides to regulate the output voltage as shown in Fig. 2. However, since the SSC method requires at least three ICs with different grounds, it is difficult to integrate them into a single-chip, which increases the size and cost of the control stage. Moreover, the current transfer ratio of the photocoupler often changes with the temperature, which degrades the reliability on the control [9], [10].

To overcome these problems of the SSC method, several researches on the primary side control (PSC) methods have been proceeded [9]–[16]. By eliminating the photocoupler and secondary feedback circuitry, the PSC methods can decrease the size and cost of the control stage compared with the SSC method. In [11] and [12], the PSC methods for contactless resonant

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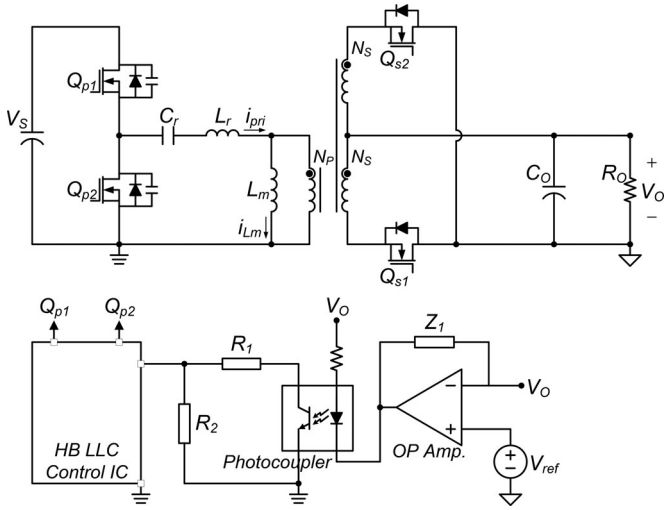

Fig. 2. Schematic of HB *LLC* converter with the conventional SSC method.

converters are proposed. In [11], complex calculations should be required to estimate the output voltage. Moreover, it is limited to the *LCL* resonant converter. In [12], the PSC method is applied to the HB *LLC* converter for the battery charging system. However, due to the additional circuits such as the phase detector circuit and state determiner circuit, the control stage becomes complex and the size and cost increase. Moreover, since it controls not the output voltage of the converter but battery voltage, the output voltage of the converter cannot be accurately regulated. In [9], [10], [13]–[16], the PSC methods for the flyback converter are proposed. They commonly have simple control stage compared with the PSC methods for contactless resonant converters. However, they have some challenges in applying them to the HB *LLC* converter because of the following reasons. Fig. 3(a) and (b) shows the simplified block diagram and operational key waveforms of the HB *LLC* converter with the conventional PSC methods applied to the flyback converter, respectively. As shown in Fig. 3(a), the center-tapped rectifier was adopted for high-power adaptor applications with low output voltage. In addition, the secondary switches are used to decrease the secondary conduction losses. Moreover, to prevent a high voltage oscillation across the secondary switches, the transformer should have a small leakage inductor L_{lkg} and the required resonant inductor should be adjusted by an external inductor L_r in the primary side.

In the conventional PSC methods applied to the flyback converter, when the secondary current $i_{\rm sec1}(t)$ reaches 0 A at time t_1, the auxiliary winding voltage $v_{NA}(t_1)$ is obtained by the sample-and-hold (S/H) circuit, and the voltage control loop enables $v_{NA}(t_1)$ to follow a reference value $V_{\rm ref}$, i.e., $V_{\rm ref} = N_A V_O / N_S$. At time t_1 when the primary and secondary switches Q_{p1} and Q_{s1} are turned off, $v_{NA}(t_1)$ becomes $N_A(V_O + v_{lkgs1}(t_1))/N_S$. Assuming that the transformer secondary leakage inductor L_{lkgs1} is neglected, $v_{NA}(t_1)$ becomes $N_A V_O / N_S$, and the output voltage can be accurately regulated. However, in practice, L_{lkgs1} surely exists due to L_{lkg} in the primary side. Therefore, in the HB *LLC* converter, the voltage $v_{lkgs1}(t_1)$ across L_{lkgs1} becomes large due to steep slope of

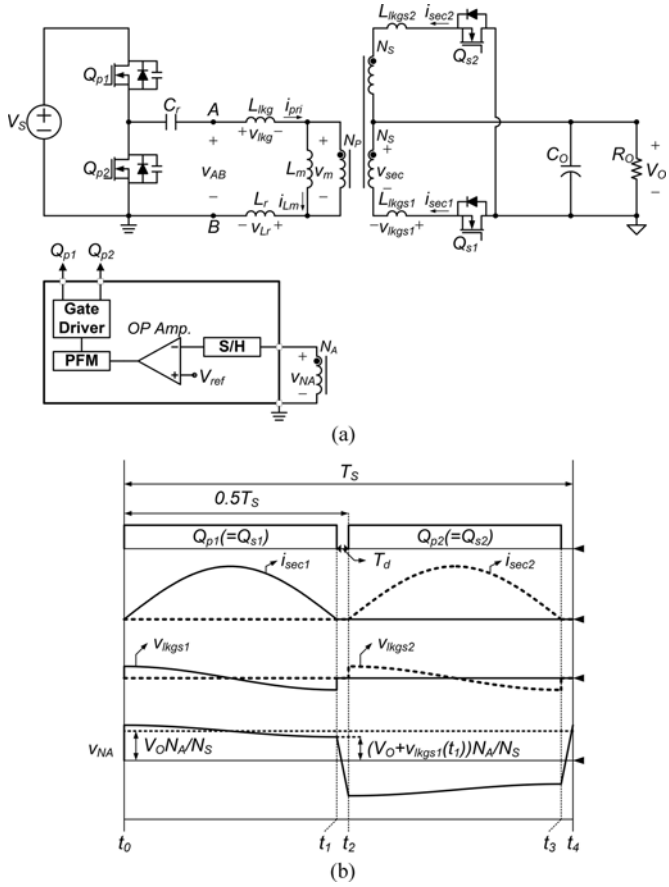

Fig. 3. Conventional PSC method for HB *LLC* converter. (a) Simplified block diagram. (b) Operational key waveforms.

$i_{\rm sec1}(t)$ at time t_1 caused by sinusoidal secondary current as shown in Fig. 3(b), while the secondary current in the flyback converter has a gentle slope resulting from large L_m. Since $v_{NA}(t_1)$ follows $V_{\rm ref}$, i.e., $V_{\rm ref} = N_A V_O / N_S$, the output voltage cannot be accurately regulated. Therefore, it has the limitation in applying the conventional PSC methods to the HB *LLC* converter due to large $v_{lkgs1}(t_1)$.

In this letter, a new PSC method for the HB *LLC* converter is proposed to improve the regulation accuracy of the conventional PSC methods applied to the flyback converter, maintaining simple control stage as shown in Fig. 4. In the proposed PSC method, the output voltage is regulated by obtaining $v_{\rm sen}(t)$ when the external resonant inductor voltage $v_{Lr}(t)$ becomes 0 V. At this time, since the voltage across the transformer secondary leakage inductor is small, the proposed method can accurately regulate the output voltage.

II. Proposed Method

A. Principle of the Proposed PSC Method

Figs. 4 and 5, respectively, show the simplified block diagram and operational key waveforms of the HB *LLC* converter with the proposed PSC method under the following assumptions:

1) all parasitic components except for those specified in Fig. 4 are ignored;

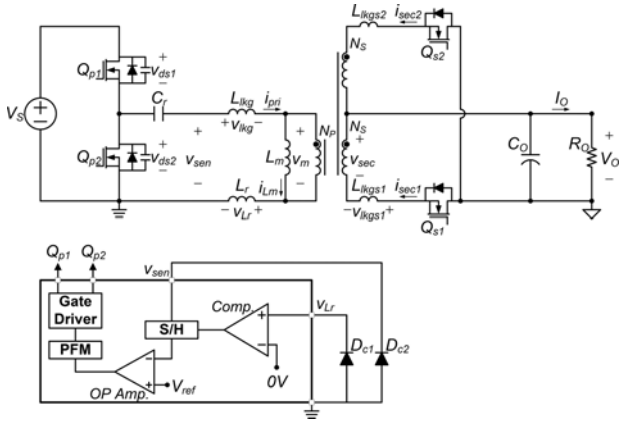

Fig. 4. Simplified block diagram of HB *LLC* converter with the PSC method.

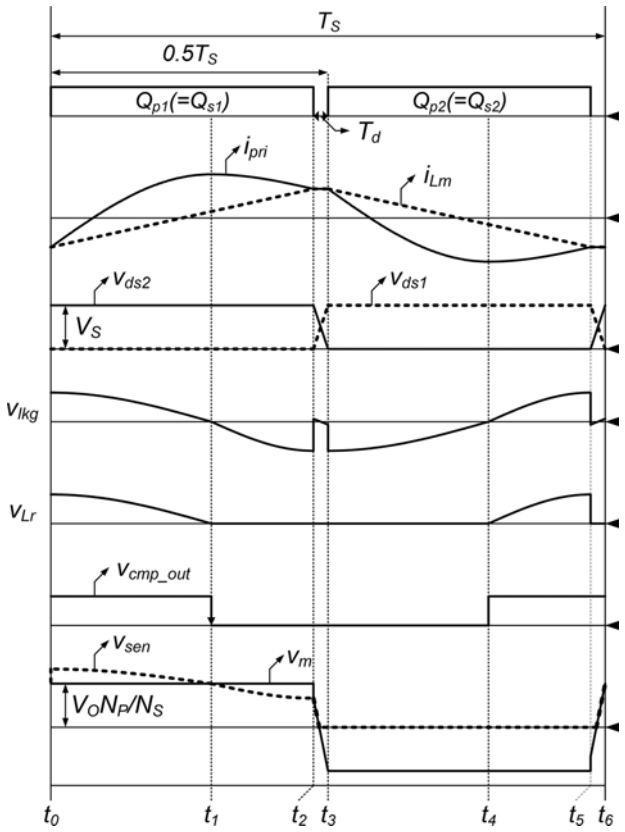

Fig. 5. Operational key waveforms of the HB *LLC* converter with the PSC method.

2) the transformer secondary leakage inductors L_{lkgs1} and L_{lkgs2} are ignored, the analysis including L_{lkgs1} and L_{lkgs2} is discussed in Section II-B;
3) the turn-on resistance $R_{ds,\mathrm{on}}$ of the secondary switches Q_{s1} and Q_{s2} is small enough to be ignored;
4) the forward voltage drops of two Schottky diodes D_{c1} and D_{c2} are zero;
5) the output voltage V_O is constant.

As shown in Fig. 4, the external resonant inductor L_r is located beside the primary ground to easily sense $v_{Lr}(t)$, and two Schottky diodes D_{c1} and D_{c2} are used to enable two sensing voltages $v_{Lr}(t)$ and $v_{\mathrm{sen}}(t)$ to have positive value that is appropriate for the controller IC. As shown in Fig. 5, the HB *LLC* converter operates near the resonant frequency in order to obtain maximized efficiency, and its operation can be divided into two half-cycles t_0–t_3 and t_3–t_6. Since two half-cycles have symmetric operation, the first half-cycle is only explained.

1) Mode 1 [t_0–t_2]: The primary switch Q_{p1} is turned on at time t_0. Since the secondary switch Q_{s1} is turned on, the magnetizing inductor current $i_{Lm}(t)$ is linearly increased with a slope of $N_P V_O/N_S/L_m$, and the transformer leakage inductor L_{lkg}, external resonant inductor L_r, and resonant capacitor C_r begin to resonate. Thus, the primary current $i_{\mathrm{pri}}(t)$ has sinusoidal shape. The voltages $v_{lkg}(t)$ and $v_{Lr}(t)$ across L_{lkg} and L_r can be expressed as follows:

$$v_{\mathrm{lkg}}(t) = L_{\mathrm{lkg}} \frac{di_{\mathrm{pri}}(t)}{dt} \tag{1}$$

$$v_{Lr}(t) = L_r \frac{di_{\mathrm{pri}}(t)}{dt}. \tag{2}$$

Based on (1) and (2), it can be seen from Fig. 5 that $v_{lkg}(t_1)$ and $v_{Lr}(t_1)$ become 0 V when $i_{\mathrm{pri}}(t)$ reaches its peak value at time t_1. Since $v_{lkg}(t_1)$ and $v_{Lr}(t_1)$ become 0 V, $v_{\mathrm{sen}}(t_1)$ becomes $N_P V_O/N_S$, i.e., $v_{\mathrm{sen}}(t) = N_P V_O/N_S + v_{lkg}(t) + v_{Lr}(t)$. As shown in Fig. 4, $v_{Lr}(t)$ is compared with 0 V. When $v_{Lr}(t)$ decreases and reaches 0 V at time t_1, the output $v_{\mathrm{cmp_{out}}}(t_1)$ of the comparator is changed from high value to low value. By using the S/H circuit, $v_{\mathrm{sen}}(t_1)$ can be obtained at only falling edge of $v_{\mathrm{cmp_{out}}}(t)$ [12], and the voltage control loop enables $v_{\mathrm{sen}}(t_1)$ to follow V_{ref}, i.e., $V_{\mathrm{ref}} = N_P V_O/N_S$. Therefore, the output voltage can be accurately regulated by obtaining $v_{\mathrm{sen}}(t_1)$ since $v_{lkg}(t_1)$ and $v_{Lr}(t_1)$ become 0 V. When $v_{Lr}(t)$ and $v_{\mathrm{sen}}(t)$ go to negative, D_{c1} and D_{c2} clamp the voltages to 0 V.

2) Mode 2 [t_2–t_3]: At time t_2, $i_{\mathrm{pri}}(t)$ becomes equal to $i_{Lm}(t)$, and Q_{p1} is turned off. The peak magnetizing inductor current $i_{Lm}(t_2)$, considered as a current source, discharges the output capacitor of Q_{p2}. Thus, $v_{ds2}(t)$ is linearly decreased and reaches zero. At this time, Q_{p2} is turned on, and the ZVS of Q_{p2} can be achieved.

B. Effect of the Transformer Secondary Leakage Inductor

In this section, since the transformer secondary leakage inductors L_{lkgs1} and L_{lkgs2} have a strong influence on the regulation accuracy, the analysis considering L_{lkgs1} and L_{lkgs2} is discussed. Fig. 6(a) and (b) shows the current and voltage waveforms according to L_m, considering L_{lkgs1} and L_{lkgs2}. During mode 1, $i_{Lm}(t)$ is linearly increased with a slope of $N_P V_O/N_S/L_m$, and L_{lkg}, L_r, and C_r resonate. Therefore, $i_{Lm}(t)$ and $i_{\mathrm{pri}}(t)$ can be expressed as follows:

$$i_{Lm}(t) = \frac{N_P V_O}{N_S L_m}(t - t_0) - \frac{N_P V_O}{4 N_S L_m f_s} \tag{3}$$

$$i_{\mathrm{pri}}(t) = i_{\mathrm{pri}}(t_0)\cos(\omega_O(t - t_0)) + \left(\frac{V_S - v_{Cr}(t_0) - N_P V_O/N_S}{Z}\right)\sin(\omega_O(t - t_0)) \tag{4}$$

where $v_{Cr}(t_0)$ and $i_{\mathrm{pri}}(t_0)$ are the initial values of the resonant capacitor voltage $v_{Cr}(t)$ and primary current $i_{\mathrm{pri}}(t)$, f_s is the

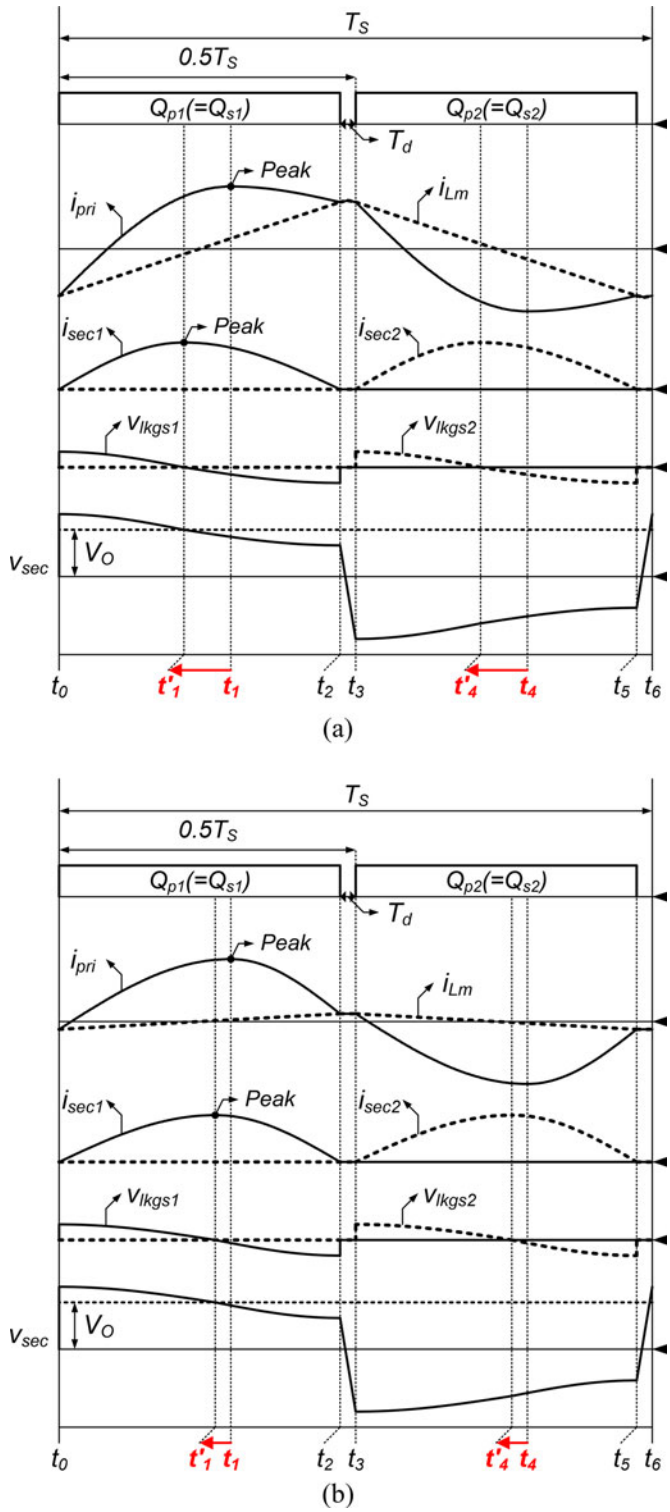

Fig. 6. Current and voltage waveforms of i_{Lm}, $i_{\rm pri}$, $i_{\rm sec1}$, $i_{\rm sec2}$, v_{lkgs1}, v_{lkgs2}, and $v_{\rm sec}$ according to L_m. (a) Small L_m. (b) Large L_m.

switching frequency, and the characteristic impedance Z and resonant angular frequency ω_O are defined as $[(L_{lkg}+L_r)/C_r]^{0.5}$ and $1/[(L_{lkg}+L_r)C_r]^{0.5}$.

Based on (1) and (2), when $i_{\rm pri}(t)$ reaches its peak value at time t_1, both $v_{lkg}(t)$ and $v_{Lr}(t)$ become 0 V, and t_1 can be

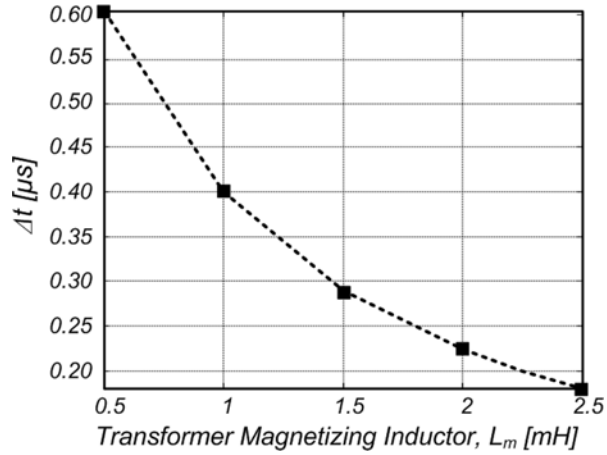

Fig. 7. Δt according to L_m under full-load conditions.

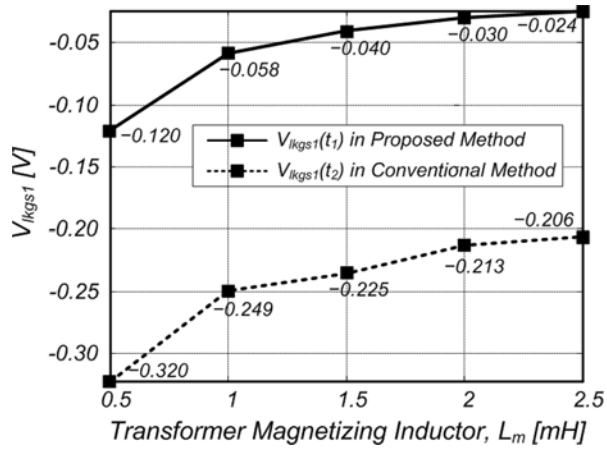

Fig. 8. $v_{lkgs1}(t_1)$ and $v_{lkgs1}(t_2)$ according to L_m under full-load conditions.

expressed as follows:

$$t_1 = t_0 + \frac{1}{\omega_O}\left[\pi + \tan^{-1}\left(\frac{V_S - v_{Cr}(t_0) - N_P V_O/N_S}{i_{\rm pri}(t_0)Z}\right)\right]. \tag{5}$$

Meanwhile, the secondary current $i_{\rm sec1}(t)$ during mode 1 is the difference between $i_{\rm pri}(t)$ and $i_{Lm}(t)$, and $i_{\rm sec1}(t)$ can be expressed as follows:

$$i_{\rm sec\,1}(t) = \frac{N_P}{N_S}(i_{\rm pri}(t) - i_{Lm}(t)). \tag{6}$$

As shown in Fig. 6(a) and (b), since $i_{\rm sec1}(t)$ reaches its peak value at time not t_1 but t'_1, the voltage $v_{lkgs1}(t_1)$ across L_{lkgs1} becomes negative, and t'_1 can be expressed as follows:

$$t'_1 = t_1 - \frac{1}{\omega_O}\sin^{-1} \times \left[\frac{N_P V_O}{N_S L_m \omega_O \sqrt{i^2_{\rm pri}(t_0) + \left(\frac{V_S - v_{Cr}(t_0) - N_P V_O/N_S}{Z}\right)^2}}\right]. \tag{7}$$

TABLE I
CIRCUIT PARAMETERS OF THE HB *LLC* CONVERTER WITH PSC METHODS

Rated power	85 W	Input voltage V_S	400 V
		Output voltage V_O	20 V
Main switches (Q_{p1}, Q_{p2})		IPP60R600CP	
External resonant inductor (L_r)		31.05 μH	
Resonant capacitor (C_r)		47 nF	
Main transformer	Core	PQ2620	
		$N_P : N_S : N_S = 20 : 2 : 2$	
		L_m: 2.25 mH, L_{lkg}: 5.5 μH	
Secondary switches		BSC077N12NS3G	
(Q_{s1}, Q_{s2})		(120 V, 98 A, $R_{ds,on:7.7}$ m Ω)	

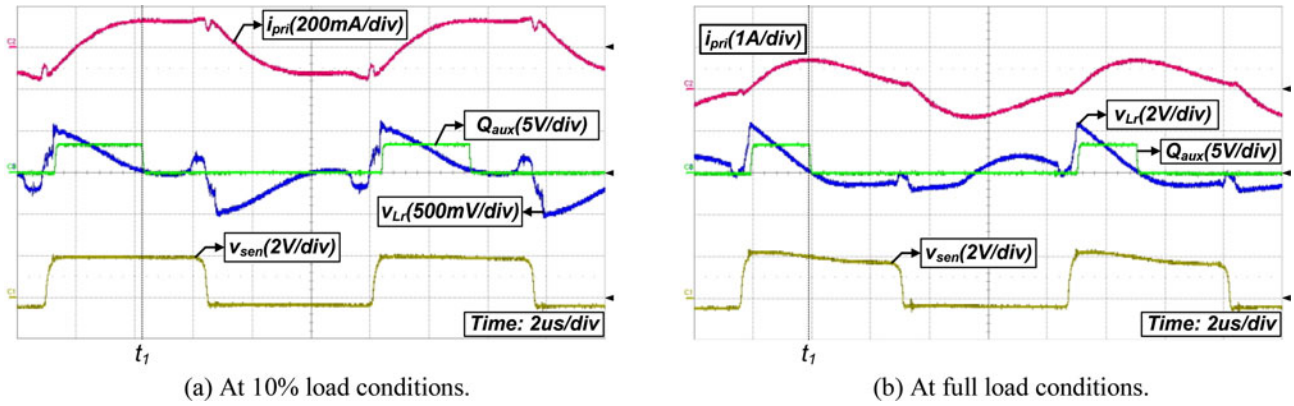

Fig. 9. Experimental key waveforms of $i_{\rm pri}$, v_{Lr}, $v_{\rm aux}$, and $v_{\rm sen}$ under 10% and full-load conditions. (a) Under 10% load conditions. (b) Under full-load conditions.

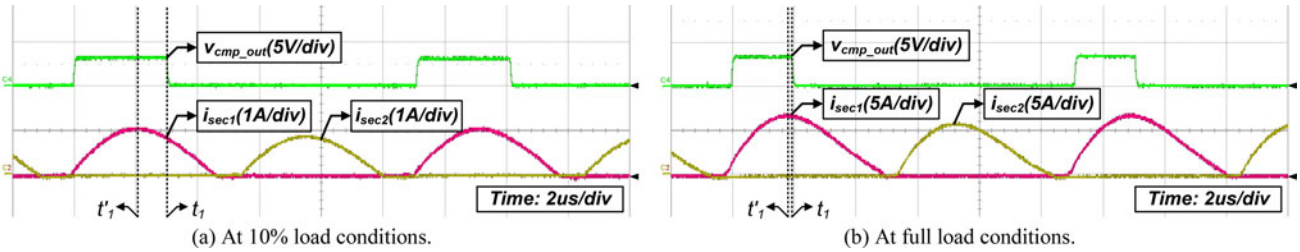

Fig. 10. Experimental key waveforms of $v_{\rm aux}$, $i_{\rm sec1}$, and $i_{\rm sec2}$ under 10% and full-load conditions. (a) Under 10% load conditions. (b) Under full-load conditions.

From (7), as the transformer magnetizing inductor L_m is decreased, it can be seen from Fig. 6(a) that t_1' deviates farther from t_1 and $v_{lkgs1}(t_1)$ becomes more negative due to steep slope of $i_{\rm sec1}(t)$ at time t_1. For example, let us $V_S = 400\ V$, $V_O = 20\ V$, $N_P/N_S = 10$, and $f_s = 100\ kHz$, which are used in the experiment, and it is assumed that $L_{lkgs1} = 30\ nH$. Fig. 7 shows Δt according to L_m under full-load conditions, i.e., $\Delta t = t_1 - t_1'$. From Fig. 7, as L_m is decreased, it can be seen that t'_1 deviates farther from t_1. As a result, as L_m is decreased, $v_{lkgs1}(t_1)$ becomes more negative as shown in Fig. 8. However, since the variation of Δt is small according to L_m, $v_{lkgs1}(t_1)$ is not large even despite small L_m. In the proposed method, since $v_{\rm sen}(t_1)$ becomes $N_P(V_O + v_{lkgs1}(t_1))/N_S$, designing larger L_m indicates that $v_{lkgs1}(t_1)$ is smaller and more accurate output voltage is obtained.

Meanwhile, in the HB *LLC* converter with the conventional PSC methods, when $i_{\rm sec1}(t)$ reaches 0 A at time t_2 as shown in Fig. 6(a) and (b), $v_{NA}(t_2)$ is obtained, i.e., $v_{NA}(t_2) = N_A(V_O + v_{lkgs1}(t_2))/N_S$. Since $v_{lkgs1}(t_2)$ is much larger than $v_{lkgs1}(t_1)$ at the same L_m, as shown in Fig. 8, the output voltage in the conventional PSC methods can be less accurately regulated than that in the proposed PSC method.

III. EXPERIMENTAL RESULTS

To verify the validity of the proposed PSC method for the HB *LLC* converter, an 85 W prototype converter with the specification of $V_S = 400\ V$ and $V_O = 20\ V$ has been built, and a PIC33FJ16GS502 microcontrol unit (MCU) is utilized. The design parameters utilized in this experiment are presented in

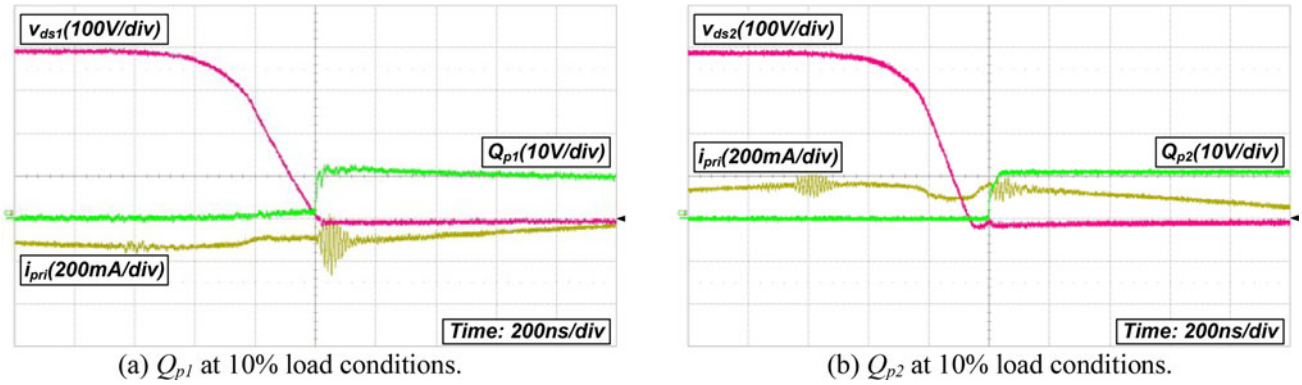

Fig. 11. ZVS waveforms. (a) Q_{p1} under 10% load conditions. (b) Q_{p2} under 10% load conditions.

TABLE II
MEASURED SWITCHING FREQUENCY AND EFFICIENCY OF THE PROPOSED METHOD

Output load	Switching frequency	Efficiency	Output load	Switching frequency	Efficiency
10%	91 kHz	91.38%	60%	86 kHz	95.11%
20%	89 kHz	92.75%	70%	85 kHz	95.21%
30%	88 kHz	93.92%	80%	85 kHz	95.31%
40%	87 kHz	94.83%	90%	83 kHz	95.48%
50%	87 kHz	94.98%	100%	82 kHz	95.61%

TABLE III
MEASURED OUTPUT VOLTAGE OF PSC METHODS ACCORDING TO OUTPUT LOAD

Output load	Output voltage		Output load	Output voltage	
	Conventional PSC method	Proposed PSC method		Conventional PSC method	Proposed PSC method
10%	20.235 V	20.141 V	60%	20.501 V	20.105 V
20%	20.291 V	20.135 V	70%	20.554 V	20.097 V
30%	20.342 V	20.130 V	80%	20.607 V	20.091 V
40%	20.394 V	20.121 V	90%	20.660 V	20.085 V
50%	20.448 V	20.112 V	100%	20.714 V	20.077 V

Table I. The *S/H* to obtain $v_{\rm sen}(t_1)$ is implemented by using the functions provided by the MCU. An auxiliary gate signal $v_{\rm aux}(t)$ is turned on at the instant Q_{p1} is turned on. When $v_{\rm cmp\_out}(t)$ becomes low, $v_{\rm aux}(t)$ can be turned off. At this instant, $v_{\rm sen}(t)$ can be sampled, which is provided by the MCU.

Fig. 9(a) and (b) shows the experimental key waveforms of the HB *LLC* converter with the proposed PSC method under 10% and full-load conditions. As can be seen from $i_{\rm pri}(t)$ and $v_{Lr}(t)$ in Fig. 9(a) and (b), $v_{Lr}(t_1)$ becomes 0 V when $i_{\rm pri}(t)$ reaches its peak value at time t_1. Due to a gentle slope of $i_{\rm pri}(t)$ under 10% load conditions, $v_{Lr}(t)$ is not clamped to the forward voltage drop during t_2–t_3, as shown in Fig. 9(a). In addition, from $v_{\rm aux}(t)$ in Fig. 9(a) and (b), it can be seen that $v_{\rm aux}(t_1)$ is changed from high value to low value. From $i_{\rm sec1}(t)$ in Fig. 10(a) and (b), it can be seen that $i_{\rm sec1}(t)$ reaches its peak value at time not t_1 but t_1'. However, since L_m is large enough, the slope of $i_{\rm sec1}(t)$ is gradual at time t_1, and $v_{lkgs1}(t_1)$ is small. Fig. 11(a) and (b) shows the ZVS waveforms of Q_{p1} and Q_{p2} under 10% load conditions, respectively. Since the ZVS of the primary switches is achieved by sufficient energy stored in L_m, it can be seen that the ZVS of Q_{p1} and Q_{p2} is achieved under 10% load conditions. Furthermore, the HB *LLC* converter with the proposed PSC method achieves a high efficiency over the entire load conditions, as shown in Table II. Table III shows the measured output voltage of the conventional and proposed PSC methods according to the output load conditions. As shown in this table, it can be seen that the proposed method has the improved output voltage regulation capability within 0.71% by minimizing $v_{lkgs1}(t_1)$ compared the output voltage regulation capability of the conventional method within 3.57%.

IV. CONCLUSION

This paper introduces a new PSC method for the HB *LLC* converter. The proposed method has the output voltage regulation capability within 0.71% by minimizing the voltage across the transformer secondary leakage inductor. The validity of this study is confirmed by the experimental results. It is suitable for

high-power adaptor applications employing the HB *LLC* converter for the tablet PCs and laptop computers.

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