Time-Shift Current Balance Technique in Four-Phase Voltage Regulator Module with 90% Efficiency for Cloud Computing

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***Abstract*—Four power stages for voltage regulator module (VRM) are adopted to provide high current driving capability and low output ripple in cloud computing. Thus, the time-shift current balance (TSCB) technique is proposed to achieve high performance power supply for servers. In addition, the power request, which includes the number of active phases and voltage identification, is acknowledged by servers for high driving capability during high throughput and high efficiency during standby mode. Furthermore, to equally distribute the current in each phase, the proposed TSCB technique in either voltage-mode or peak current-mode control improves the current balance performance and solves the stability problem. In the scale-down clouding computing prototype, the efficiency can be kept higher than 90% over a wide load current range of 2 A. In addition, the performance and operating frequency of the servers in stable operation are not limited by the VRM with the TSCB technique.**

***Index Terms*—Cloud computing, ramp-amplitude adjustable current balance technique, time-shift current balance (TSCB), voltage identification (VID), voltage regulator module (VRM).**

I. Introduction

CLOUD computing allows for using remote servers to store and process data rather than a local machine. It reduces information technology (IT) expenditures, increases network flexibility and streamlines communication infrastructure. Besides, cloud computing servers permit end users to take advantage of a large network of computers without having to maintain hardware [1]–[3]. However, an effective power solution is needed for delivering high power consumption and high performance servers. The power request is decided by the voltage identification (VID), which is a digital signal containing several bits and generated by servers to adjust the reference voltage. Thus, the switch-mode converters can scale the output voltage dynamically according to this adjustable reference voltage. Power consumption of servers is able to decrease during idle periods by lowering the supply voltage. On the other hand, computing performance can be improved if the supply voltage is scaled up accordingly. To achieve the demands for servers, several power stages in parallel can provide large current driving capability. Using interleaving operation can improve load transient response and reduce output ripple without increasing switching loss because the switching frequency is equivalently increased [4]–[6]. Moreover, the number of active power stages is decided by the cloud computing system for high efficiency and better thermal management.

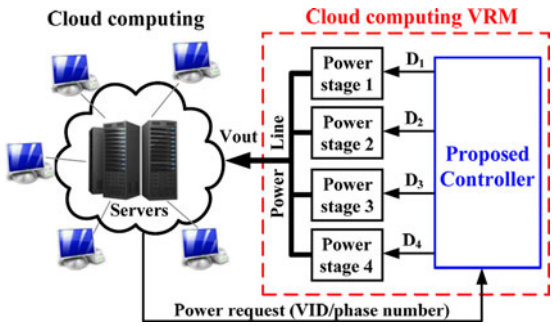

Fig. 1. Simplified schematic diagram of the cloud computing power solution by the proposed VRM.

Fig. 1 illustrates simplified schematic diagram of the cloud computing power solution using the proposed voltage regulator module (VRM). Four power stages are adopted with an interleaving operation. The currents provided by four phases are collected on the power line, $V_{\rm OUT}$, and sent to the cloud computing servers. The four phases are manipulated by the proposed controller. Additionally, the power request including active-phase number and VID find the tradeoff between performance and efficiency. Nevertheless, even though the duty cycles, D_1–D_4, are exactly the same, equal current distribution in each phase is unable to be confirmed if mismatches exist among the phases. Therefore, the current balance mechanism is necessary to ensure high efficiency and thermal management.

Fig. 2(a) shows current distribution of four phases without adopting any current balance mechanism. As load current increases, current unbalance circumstance becomes more serious. Especially at heavy load, the current of each channel is unequal extremely and thus deteriorates the total efficiency. Taking $I_{\rm L1}$ as an example, the duty cycle, D_1, is required to decrease and thus suppress I_{L1} (current in channel 1) since I_{L1} is much larger than I_{L2}–I_{L4} (currents of the other phases). D_2–D_4 are also modulated according to the difference between I_{L2}–I_{L4}

Manuscript received April 1, 2014; revised April 22, 2014; accepted April 22, 2014. Date of publication April 30, 2014; date of current version October 15, 2014. Recommended for publication by Associate Editor J. A. Cobos.

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Digital Object Identifier 10.1109/TPEL.2014.2321177

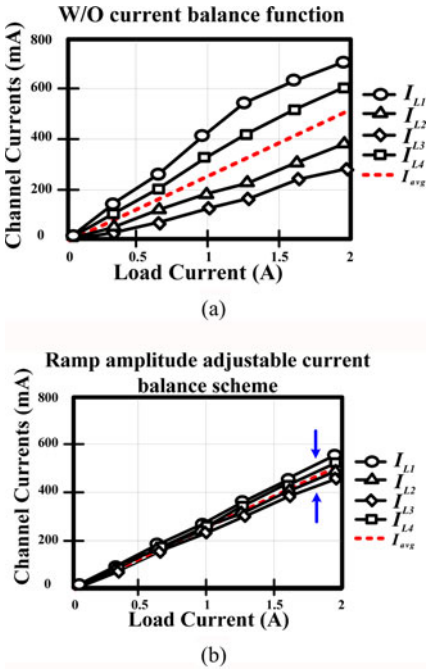

Fig. 2. Current distribution and ramp signal waveforms (a) without adopting current balance function and (b) with adopting conventional RACB technique.

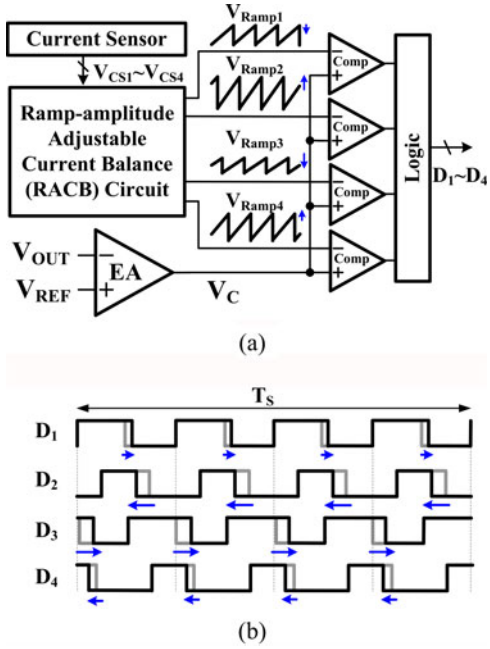

Fig. 3. Conventional RACB technique. (a) Block diagram. (b) Waveforms of duty cycle adjustment.

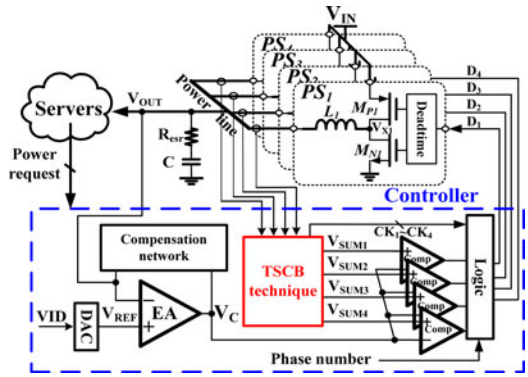

Fig. 4. Architecture of the proposed cloud computing VRM with the TSCB technique in both voltage- and current-mode controls.

and the average current, $I_{\rm avg}$. By employing current balance technique to properly adjust duty cycles, I_{L1}–I_{L4}, are balanced to approach to $I_{\rm avg}$, as shown in Fig. 2(b).

The simplest current balance mechanism is the droop method which does not require any communication between the parallel modules [7]. It relies on the output resistance of the parallel modules to maintain a relatively equal current distribution among the modules. However, the tradeoff must be made between load regulation and output voltage set point. For high performance cloud computing VRM, the passive current balance is not adequate. On the other hand, there are several current balance mechanisms with closed-loop control to conquer the drawbacks of poor regulation [8]. Current unbalance levels are estimated in each phase to adjust the error signal for duty cycle adjustment accordingly. However, it results in complicated current balance control, which integrates the output voltage dependent information and the channel current dependent information. In some of the applications, feedforward technique is widely used to include line voltage information by adjusting the amplitude of ramp signal [9]–[13]. Generally speaking, duty cycle can be easily adjusted by the ramp-amplitude adjustable (RACB) technique, which is similar to the techniques used in feedforward control. Combining the channel current control with ramp signal adjustment of each phase is a better choice for silicon implementation owing to the simple architecture [14], [15].

Fig. 3(a) illustrates the block diagram of conventional ramp-amplitude adjustable current balance (RACB) technique which combines the channel current control and ramp signals, $V_{\rm Ramp1}$–$V_{\rm Ramp4}$. Ideally, $V_{\rm Ramp1}$–$V_{\rm Ramp4}$ are identical but interleaving. Comparing $V_{\rm Ramp1}$–$V_{\rm Ramp4}$ with the error signal, V_C, four interleaving duty cycles, D_1–D_4, all of which have the same on-time, are generated to control four power stages. If perfectly matching is assumed, the current to servers is equally provided by four phases. Nevertheless, inevitable mismatches existing in four power stages and printed circuit board result in the four channel currents unequal. Thus, unbalanced inductor current of each phase is sensed by the current sensor and sent to the RACB control circuit to adjust the amplitude of $V_{\rm Ramp1}$–$V_{\rm Ramp4}$ accordingly. In other words, by slightly adjusting the amplitude of $V_{\rm Ramp1}$–$V_{\rm Ramp4}$, D_1–D_4 can be adjusted individually to compensate the unbalanced current. The waveforms of D_1–D_4 are illustrated in Fig. 3(b), gray lines represent the original duty cycle without any adjustment. With current balance function, D_1–D_4 are modulated to balance the driving capability fairly according to I_{L1}–I_{L4}.

Even though current balance function is able to be achieved by the RACB technique, system stability still cannot be assured. Since the modulation gain is inversely proportional to the slope of ramp signal [16], the loop gain varies with different current unbalance circumstances. Lower loop gain can

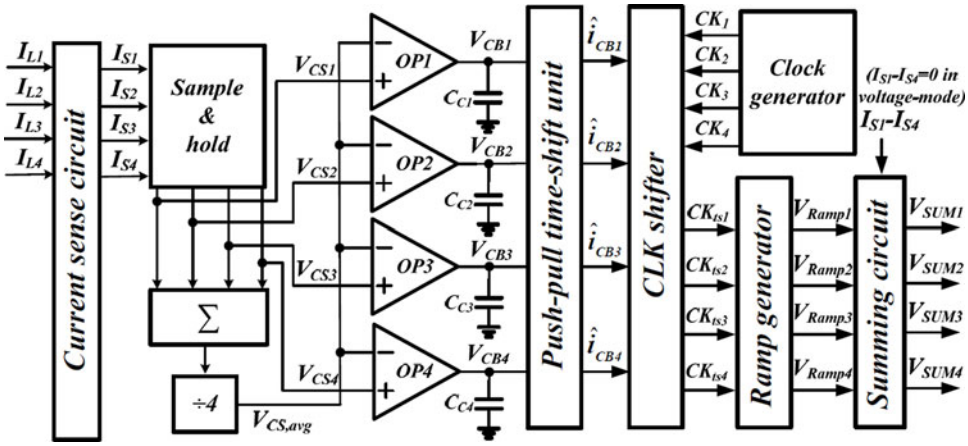

Fig. 5. Block diagram of the proposed TSCB technique.

increase the stability but sacrifice current balance performance. Moreover, applying ramp amplitude current balance technique to peak current-mode controlled VRM is a challenge. The adjusted ramp signals achieve current balance function and slope compensation concurrently. If the amplitude of ramp is largely decreased for current balance, the subharmonic phenomenon may occur owing to insufficient slope compensation [17]. Although the system stability can be ensured by overcompensation, system bandwidth, and transient response are decreased [18].

The proposed time-shift current balance (TSCB) technique for cloud computing VRM processes large current driving capability. Equal distribution between channels is accomplished and the stability of TSCB technique is ensured. The organization of this paper is as follows. Section II describes cloud computing VRM with the proposed TSCB technique. Equivalent model and stability analysis are derived in Section III. Circuit implementation of the TSCB technique is illustrated in Section IV. Measured results demonstrate the performance of the TSCB technique for cloud computing VRM as shown in Section V. Finally, conclusions are made in Section VI.

II. Cloud Computing VRM With TSCB Technique

Fig. 4 illustrates the architecture of the proposed cloud computing VRM with the TSCB. Four phases are adopted to provide large current to servers for accomplishing high current driving capability and low output ripple. Two feedback loops, voltage and current feedback loops, are controlled simultaneously to provide high performance power supply for servers in cloud computing. The voltage on the power line, $V_{\rm OUT}$, which is provided to the servers, is controlled by the voltage feedback loop. $V_{\rm OUT}$ is fed into the error amplifier, *EA*, and compare with the reference voltage, $V_{\rm REF}$, to generate the error signal, V_C. The duty cycles, D_1–D_4, which control the four power stages, PS_1–PS_4, are modulated by comparing V_C with four interleaving ramps, $V_{\rm Ramp1}$–$V_{\rm Ramp4}$, in voltage-mode control (four interleaving summing signals, $V_{\rm SUM1}$–$V_{\rm SUM4}$, in current-mode control). On the other hand, the TSCB technique, which dominates the current feedback loop, diminishes the current unbalance among the four channels.

The system in Fig. 4 can be operated in either voltage-mode or current-mode control for different applications. $V_{\rm SUMi}$ can be expressed as

$$V_{{\rm SUM}n} = V_{{\rm Ramp}n} + I_{{\rm S}n} \cdot R \text{ where } n = 1\text{–}4 \qquad (1)$$

where $I_{{\rm S}n}$ is the sensed inductor current by the current sensing circuit and the resistor R represents conversion ratio of the I-to-V function in the summing circuit. In voltage-mode operation, the second term $(I_{{\rm S}n}R)$ is not included in $V_{{\rm SUM}n}$. That is, $V_{{\rm SUM}n}$ is equal to $V_{{\rm Ramp}n}$. In the following description, $V_{{\rm Ramp}n}$ is used to represent $V_{{\rm SUM}n}$ in voltage-mode control for better understanding. On the other hand, $V_{{\rm Ramp}n}$ works as slope compensation to avoid subharmonic oscillation. The second term $(I_{{\rm S}n}R)$ is necessary for current-mode control.

For high performance and power saving, power requests are acknowledged by servers. When servers are executing massive calculation, large power demand is transmitted by phase number signal to activate all the phases. For high efficiency operation, active phase number is determined according to different load condition. Furthermore, the VID code generated by servers also can adjust the voltage reference by the digital-to-analog converter. Dynamically scaling the output voltage can reduce power consumption of servers during idle periods by lowering the supply voltage.

The block diagram of the TSCB technique is illustrated in Fig. 5. Inductor current of each phase is sensed by individual current sensors to generate I_{S1}–I_{S4}. Since I_{S1}–I_{S4} fluctuate with inductor current ripples, a sample and hold circuit is required to obtain fixed values, $V_{\rm CS1}$–$V_{\rm CS4}$, during each switching cycle. After dividing the summation of $V_{\rm CS1}, V_{\rm CS2}, V_{\rm CS3}$, and $V_{\rm CS4}$ by four, the average inductor current value, $V_{\rm CS,avg}$, can be obtained. To effectively suppress unbalanced level, the difference voltages between $V_{\rm CS1}$–$V_{\rm CS4}$ and $V_{\rm CS,avg}$ are amplified by operational amplifiers with the gain of $A_{\rm OP}(s)$ to generate $V_{\rm CB1}$–$V_{\rm CB4}$. Next, push–pull time-shift unit of which transconductance is G_{V_I} is used to generate current balance ac control currents, $\hat{i}_{\rm CB1}$–$\hat{i}_{\rm CB4}$. According to $\hat{i}_{\rm CB1}$–$\hat{i}_{\rm CB4}$, shifted clock signals, $CK_{\rm ts1}$–$CK_{\rm ts4}$, are generated by slightly shifting original clock signals, CK_1–CK_4. Finally, the amplitudes of $V_{\rm Ramp1}$–$V_{\rm Ramp4}$ in voltage-mode ($V_{\rm SUM1}$–$V_{\rm SUM4}$ in

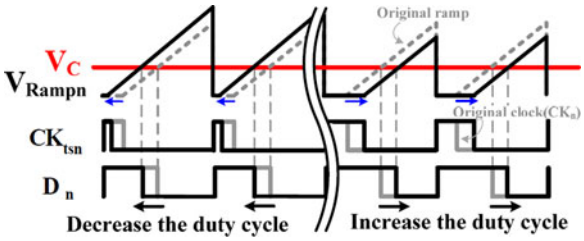

Fig. 6. Operation waveforms of the TSCB technique in voltage-mode controlled VRM.

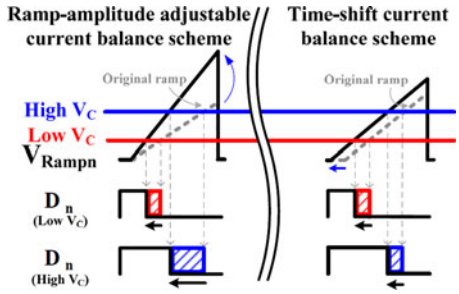

Fig. 7. Stability comparison of low and high output voltage (low and high V_C) with the RACB and the proposed TSCB in voltage-mode controlled VRM.

current-mode) are modulated to achieve current balance function. The gain of current unbalance amplification is $A_{\mathrm{CB}(s)}$ as shown in the following equation:

$$A_{\mathrm{CB}}(s) = A_{\mathrm{OP}}(s) \cdot G_{V-I}. \tag{2}$$

To conquer the drawbacks of conventional RACB, the operation waveforms of the TSCB technique is depicted in Fig. 6. Instead of adjusting the amplitude, ramp signals are shifted at the time domain according to different current unbalance levels. In Fig. 6, the ramp with dotted gray dashed line represents the original ramp signal without adopting any current balance mechanism. If one of the four channel currents, I_{Ln}, where $n =$ 1–4, is larger than the average current, I_{avg}, the duty cycle has to be decreased to suppress the current of channel n. Thus, the ramp signal with index n, V_{Rampn}, is adjusted by the advance of time shift based on the original ramp signal, i.e., the beginning time of the ramp signal is shifted in advance during one switching cycle. The beginning time is indicated by the shifted clock signal, CK_{tsn}, which is compressed by the original clock signal, CK_n, according to current unbalance level. Contrarily, if one of the four channel currents, I_n, where $n =$ 1–4, is smaller than I_{avg}, the duty cycle of the phase has to be increased to enlarge the channel current. Therefore, V_{Rampn} is adjusted by the postponement of time shift based on the original ramp signal, i.e., the beginning time of the ramp is shifted by a delay during one switching cycle. According to current unbalance level, the beginning time is indicated by CK_{tsn}, which is extended by the original clock signal, CK_n. Obviously, the slope of V_{Rampn} is kept constant in different current unbalance level.

The stability comparison of the RACB and the proposed TSCB techniques in voltage-mode controlled VRM, which contain two cases, is illustrated in Fig. 7. According to VID codes, low output voltage, which has lower V_C and smaller D_n, is required for power saving while high output voltage, which has higher V_C and larger D_n, is required for massive calculations. Assuming that one of the four channel currents, I_{Ln}, where $n =$ 1–4, is larger than the average current, the duty cycle, D_n, has to be decreased to ensure current balance. Conventional RACB technique increases the ramp amplitude to decrease D_n. Thus, the slope of the ramp is increased simultaneously. On the other hand, the TSCB balance technique shifts the ramp in advance without altering the slope.

When the output voltage is lowered to save power, the error signal, V_C, is located at a lower level (red line) to generate a reduced duty cycle. To solve current unbalance problem, the decreased duty cycles in red regions are the same either by RACB or TSCB technique. Thus, both current balance techniques can achieve the same current balance performance. When the output voltage is higher for high-speed operation, the error signal, V_C, is located at a higher level (blue line) to generate a larger duty cycle. In this case, the adjusted duty cycle by the RACB technique is much larger than that of the TSCB technique. In summary, with the same amplitude adjustment, duty cycle variations are different with different V_{OUT} and V_C in the RACB. On the other hand, with the same shifted time, duty cycle variations remain the same under all conditions. It is concluded that current balance gain varies with different duty cycle and output voltage in the RACB, while current balance gain remains the same in the TSCB. This phenomenon induces stability problem in the RACB since the system may be unstable (with insufficient phase margin) due to a large duty cycle. To increase system stability, the current balance gain has to be designed low to ensure stability during all output voltage conditions in the RACB. However, low current balance gain deteriorates current balance performance. On the other hand, the proposed TSCB technique conquers the stability problem and makes the modulation gain independent of duty cycle, V_{OUT}, V_C and current unbalance situation. Therefore, high current loop gain can be adopted to guarantee high current balance performance without being limited by the stability issue.

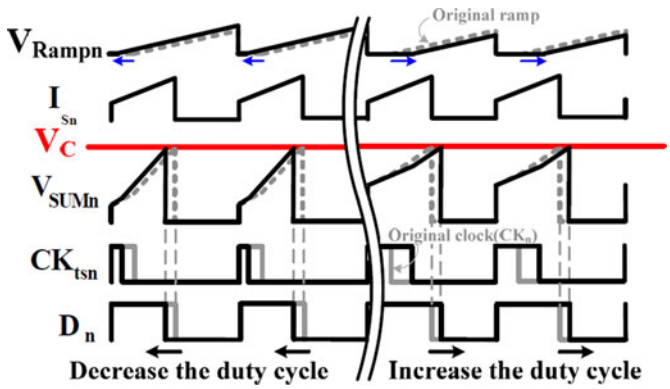

Fig. 8. Operation waveforms of TSCB technique in peak current-mode controlled VRM.

The implementation of the TSCB technique in the peak current-mode control is illustrated in Fig. 8. Similar to voltage-mode controlled VRM, V_{rampn}, is shifted from the original ramp

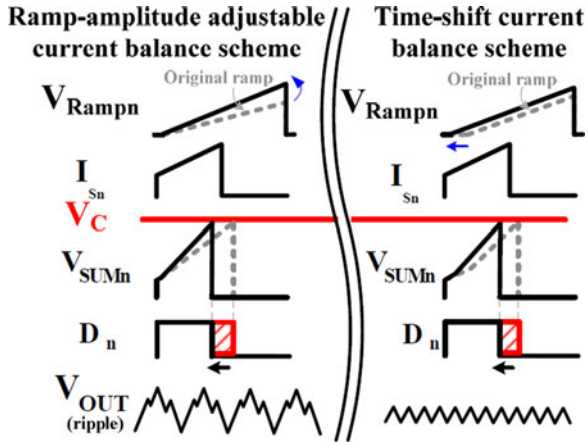

Fig. 9. Comparison of the RACB technique and the proposed TSCB technique in current-mode controlled VRM.

signal and the beginning time is defined by the shifted clock signal, CK_{tsn}, according to the current unbalance situation. Besides, adding $V_{\mathrm{ramp}n}$ to the current sense signal, I_{sn}, which indicates the current flows through the channel n, forms the summation signal, $V_{\mathrm{SUM}n}$. Comparing $V_{\mathrm{SUM}n}$ and V_C, the determined D_n can regulate V_{OUT} with a good current balance. Certainly, the slope of $V_{\mathrm{ramp}n}$ remains constant at all conditions. Different from voltage-mode controlled VRM, whose modulation gain depends on the slope of ramp signal, the slope of ramp signal is necessary for slope compensation. To avoid subharmonic oscillation, the criterion is shown as follows [16]:

$$m_a \geq \frac{V_{\mathrm{OUT}}}{2L} \text{ where } m_a \text{ is the slope of ramp signals.} \quad (3)$$

Comparison of the RACB and the proposed TSCB techniques in current-mode controlled VRM is illustrated in Fig. 9. If one of the four channel currents, I_{Ln}, where $n = 1$–4, is larger than the average current, the RACB technique increases the ramp amplitude. Thus, the slope of the ramp is increased simultaneously. Increasing slope results in over compensation and slows down transient response of the VRM [17]. To avoid over compensation, a small slope of original ramp is adopted to enhance system bandwidth and transient response. However, subharmonic oscillation will occur and result in large output ripple. On the other hand, applying the TSCB to peak current-mode control is feasible since the slope compensation mechanism is not affected by the TSCB. That is, oscillation caused by subharmonic can be avoided. Restriction in system bandwidth and transient response can be eliminated and an optimal slope compensation is simultaneously achieved.

Moreover, mismatches among current sensors and input-referred offset of operational amplifiers deteriorate the accuracy of current balance. More seriously, these effects cannot be calibrated by current balance loop. Unlike the aforementioned mismatches in power stages, which can be detected by current balance loop, mismatches in current balance circuit can be view as intrinsic offsets induced in current balance procedure. Even though this offset is much smaller than the sensed unbalanced signals, the offset is amplified by operational amplifier

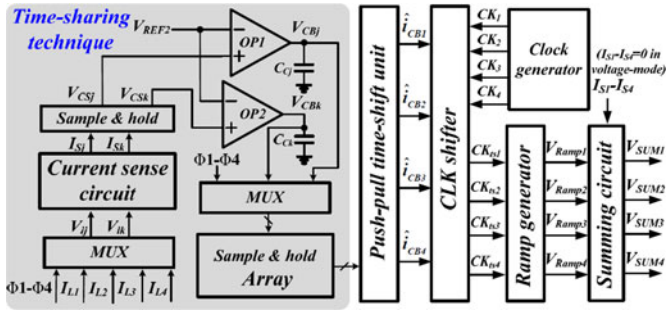

Fig. 10. Modified block diagram of the proposed TSCB with the time-sharing technique.

which are adopts for the purpose of current balance accuracy enhancement. To further enhance current balance performance, time-sharing technique is embodied in the TSCB to decrease inevitable mismatches in current balance function.

Modified block diagram of the proposed TSCB with time-sharing technique is shown in Fig. 10. Even though four phases provide energy to output simultaneously, only two sets of current balance circuits, which contain current sensor, operational amplifier and push–pull time-shift unit are adopted. To achieve current balance in four-phase operation, two of the inductor current information pieces are sent to time-sharing current balance circuit alternatively in different time slots, Φ1–Φ4. Two selected phases j and k sense the inductor current, $I_{Lj}(s)$ and $I_{Lk}(s)$, where j or $k = 1$, 2, 3, or 4, and $j \neq k$ through the use of current sensors to obtain $V_{\mathrm{CS}j}(s)$ and $V_{\mathrm{CS}k}(s)$, respectively. To achieve current balance function, current difference information of four phases is obtained by $\hat{i}_{CB1}(s)$–$\hat{i}_{CB4}(s)$. Since I_{L1}–I_{L4} are sensed and amplified by both two sets of current sensors and operational amplifiers in different time slots, $\hat{i}_{CB1}(s)$–$\hat{i}_{CB4}(s)$ are generated regardless of the offset in current balance circuits. Therefore, the mismatches between current balance circuits can be eliminated to enhance current balance performance. Moreover, two current sensing circuits, operational amplifiers and compensation capacitors are eliminated to decrease chip area and cost with a simple multiplexer and sample-and-hold circuits.

III. Stability Analysis

A. Basic Equivalent Model of the Voltage-Mode Controlled Four-Phase VRM

Basic equivalent model of the proposed voltage-mode controlled four-phase VRM is shown in Fig. 11. Four power stages, PS_1–PS_4 in Fig. 4, are controlled by duty cycle of each phase. When each channel current is perfectly matched, the duty cycle in frequency domain can be expressed as follows:

$$d_i(s) = D_i(s) \text{ where } i = 1\text{–}4 \quad (4)$$

where $D_i(s)$ is independent of load current and current unbalanced level since it is simply determined by the chosen input and output voltages as shown in the following equation:

$$D(s) = D_1(s) = D_2(s) = D_3(s) = D_4(s) = \frac{V_{\mathrm{OUT}}(s)}{V_{\mathrm{IN}}(s)}. \quad (5)$$

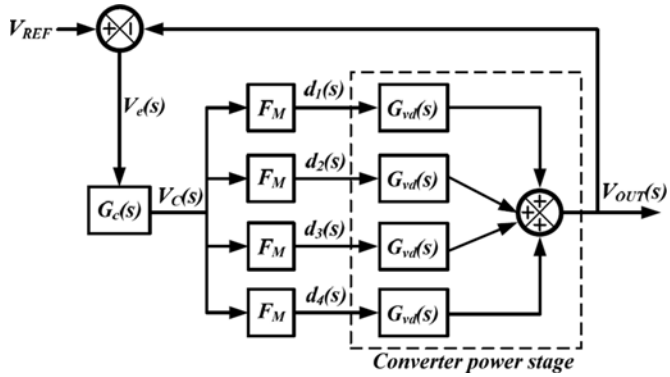

Fig. 11. Basic equivalent model of the voltage-mode four-phase VRM.

$D_1(s)$–$D_4(s)$ are with the same value, $D(s)$, which is used in the following formula derivations. The duty-to-output transfer function, contributed by the power stage, can be expressed as

$$G_{\rm vd}(s) = \frac{V_{\rm OUT}(s)}{d_i(s)} = V_{\rm IN}(s) \cdot \frac{1}{1 + s\frac{L}{R_L} + s^2 LC}$$
$$\text{where} \quad i = 1\text{–}4 \tag{6}$$

where L and C are the filter inductance and capacitance, respectively, of each phase, and R_L is equivalent load resistance of cloud computing servers.

The output voltage, $V_{\rm OUT}(s)$, collects energy from four power stages. The difference voltage, $V_e(s)$, between $V_{\rm OUT}(s)$ and $V_{\rm REF}$ is amplified by the error amplifier, *EA*, with the gain of $A_{\rm EA}$ to generate the error signal, $V_C(s)$. The error amplifier with the compensation network is represented by $G_C(s)$. The modulator transfer function, F_M, compares $V_C(s)$ with ramp signals, $V_{\rm Ramp1}$–$V_{\rm Ramp4}$, to modulate $d_1(s)$–$d_4(s)$ for regulating the output voltage according to different $V_{\rm REF}$ controlled by VID. The transfer function of the modulator is shown as

$$F_M = \frac{1}{V_M} \text{ where } V_M \text{ is the amplitude of } V_{\rm Ramp1}\text{–}V_{\rm Ramp4}. \tag{7}$$

To compensate the complex poles contributed by L and C, the proportional-integral-differential (PID) compensation network in (8) is required to increase the stability of voltage loop by inserting three poles and two zeros

$$G_c(s) = \frac{A_{EA}\left(1 + \frac{s}{\omega_{Z1}}\right)\left(1 + \frac{s}{\omega_{Z2}}\right)}{s\left(1 + \frac{s}{\omega_{P1}}\right)\left(1 + \frac{s}{\omega_{P2}}\right)}. \tag{8}$$

Two zeros, $\omega Z1$ and $\omega Z2$, can cancel the effect of LC complex poles. The dominant pole locates at the origin. Tow parasitic poles are placed above unit-gain frequency to alleviate high-frequency noise. Thus, PID compensation helps extend the system bandwidth and obtain an adequate system phase margin.

B. Model of the TSCB Technique

In the current balance control loop, inductor current of four phases are sensed in Fig. 10 by current sense circuit and sample-and-hold to generate current sense signals. The sensing factor

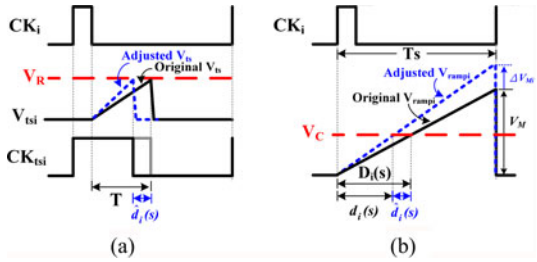

Fig. 12. Operation waveforms of duty cycle adjusted by (a) TSCB technique and (b) conventional RACB method.

of current sense circuit is R_i. According to [19], the sampling effect introduces a pair of complex right-half-plane (RHP) zeros at half the switching frequency and as expressed in (9), which is required to be considered in frequency response design

$$H_e(s) \approx \frac{s^2}{\omega_n^2} + \frac{s}{\omega_n Q_n} + 1 \text{ where } Q_n = -\frac{2}{\pi} \text{ and } \omega_n = \frac{\pi}{T_s}. \tag{9}$$

To achieve current balance function, the TSCB technique adjusts duty cycle from $D_1(s)$–$D_4(s)$ to $d_1(s)$–$d_4(s)$ by the adjustment of $\hat{d}_1(s)$–$\hat{d}_4(s)$, respectively, as shown in the following equation:

$$d_i(s) = D_i(s) - \hat{d}_i(s) \text{ where } i = 1\text{–}4 \tag{10}$$

$D_i(s)$ is the duty cycle generated by voltage loop while $\hat{d}_i(s)$ is the duty cycle adjustment caused by the TSCB technique.

To derive the TSCB model, $\hat{d}_i(s)$ has to be obtained first. The duty cycle adjustment is implemented by the CLK shifter in Fig. 10 which shifts the original clock signals CK_t to $CK_{\rm tsi}$ where $i = 1$–4. As depicted in Fig. 6, it can be observed that the shifted time of the clock signal is equal to $\hat{d}_i(s)$ where $i = 1$–4. Therefore, $\hat{d}_i(s)$ can be simply obtained by calculating the shifted time of clock signals. Fig. 12(a) illustrates operation waveforms of clock shifter and duty cycle adjusted by the TSCB technique. By changing the charge current of the time-shift capacitor, $C_{\rm tsi}$ where $i = 1$–4, in the CLK shifter, $CK_{\rm tsi}$ is modulated. The negative edge of the $CK_{\rm tsi}$ is generated when the voltage across $C_{\rm tsi}$, $V_{\rm tsi}$, reaches the reference voltage, V_R. With the shifted negative edge of the $CK_{\rm tsi}$, $\hat{d}_i(s)$ can be obtained.

Without current mismatches, a predefined constant current I_B charges the $C_{\rm tsi}$ and thus the charging time T is expressed as

$$T = \frac{V_R \cdot C_{\rm tsi}}{I_B} \text{ where } i = 1, 2, 3, \text{ or } 4. \tag{11}$$

Here, $C_{\rm ts1} = C_{\rm ts2} = C_{\rm ts3} = C_{\rm ts4} = C_{\rm ts}$. $C_{\rm ts}$ is the designed capacitance for charging and discharging in the TSCB technique.

With current mismatches, the TSCB technique superimposes a current balance control current, $\hat{i}_{{\rm CB}i}(s)$, on I_B. The current balance control current, $\hat{i}_{{\rm CB}i}(s)$, which indicates current unbalance level in each phase, is generated to achieve current balance function. Therefore, the rising slope of $V_{\rm tsi}$ is increased to shift the negative edge of $CK_{\rm tsi}$ by $\hat{d}_i(s)$ in advance. According to different current unbalance level, $\hat{i}_{{\rm CB}i}(s)$ and $\hat{d}_i(s)$ can be either

positive or negative values. Finally, (12) can be derived as

$$T - \hat{d}_i(s) = \frac{V_R \cdot C_{\rm ts}}{I_B + \hat{i}_{{\rm CB}i}(s)} \text{ where } i = 1, 2, 3, \text{ or } 4. \quad (12)$$

By substituting (11) into (12), (13) can be derived

$$\hat{d}_i(s) = \frac{V_R \cdot C_{\rm ts} \cdot \hat{i}_{{\rm CB}i}(s)}{(I_B + \hat{i}_{{\rm CB}i}(s)) \cdot I_B} \cong \frac{V_R \cdot C_{\rm ts} \cdot \hat{i}_{{\rm CB}i}(s)}{I_B^2}$$
$$\text{where} \quad i = 1,\ 2,\ 3,\ \text{or } 4. \quad (13)$$

Here, the control-current-to-duty transfer function of the TSCB technique, $CB_{\rm ts}(s)$, is defined by the ratio of $\hat{d}_i(s)$ to $\hat{i}_{{\rm CB}i}(s)$ and can be described as

$$CB_{\rm ts}(s) \equiv \frac{\hat{d}_i(s)}{\hat{i}_{{\rm CB}i}(s)} = \frac{V_R \cdot C_{\rm ts}}{I_B^2} \text{ where } i = 1,\ 2,\ 3,\ \text{or } 4. \quad (14)$$

The control-current-to-duty transfer function indicates the ability of phase current adjustment when current unbalance phenomenon happens. The duty cycle adjustment level can be easily designed by several parameters which include a constant current, I_B, a reference voltage, V_R, and the capacitance, $C_{\rm ts}$. In addition, it can be observed that $CB_{\rm ts}(s)$ is independent of output voltage, duty cycle, and inductor current. The stability can be ensured in all conditions.

On the other hand, the model of conventional RACB method is also derived for comparison. Fig. 12(b) illustrates operation waveform of duty cycle adjustment by conventional RACB. In the absence of the current balance function, the duty cycle is obtained by comparing the error signal, $V_C(s)$, with the original ramp signal, $V_{\rm rampi}$, in a switching period, T_S. The duty cycle is shown as

$$D_i(s) = \frac{V_C(s) \cdot T_S}{V_M} \text{ where } i = 1,\ 2,\ 3,\ \text{or } 4. \quad (15)$$

Here, $\Delta V_{\rm Mi}$, either a positive or a negative value, is generated and compensates the current unbalance situation to adjust the ramp amplitude as $V_M + \Delta V_{\rm Mi}$ in RACB technique. Comparing the adjusted ramp with $V_C(s)$, the duty cycle $d_i(s)$ can be expressed by

$$d_i(s) = \frac{V_C(s) \cdot T_S}{V_M - \Delta V_{\rm Mi}} \text{ where } i = 1,\ 2,\ 3,\ \text{or } 4. \quad (16)$$

$\Delta V_{\rm Mi}$ can be derived as (17) because $\Delta V_{\rm Mi}$ is produced by injecting the current balance control current, $\hat{i}_{{\rm CB}i}(s)$, into the ramp signal capacitor, $C_{{\rm ramp}i}$, within T_s for each phase

$$\Delta V_{Mi} = \hat{i}_{{\rm CB}i}(s) \cdot \frac{T_s}{C_{{\rm ramp}i}} \text{ where } i = 1,\ 2,\ 3,\ \text{or } 4 \quad (17)$$

where T_s is the switching period of the converter and $C_{\rm ramp1} = C_{\rm ramp2} = C_{\rm ramp3} = C_{\rm ramp4} = C_{\rm ramp}$. $C_{\rm ramp}$ is the designed capacitance for charging and discharging in RACB method.

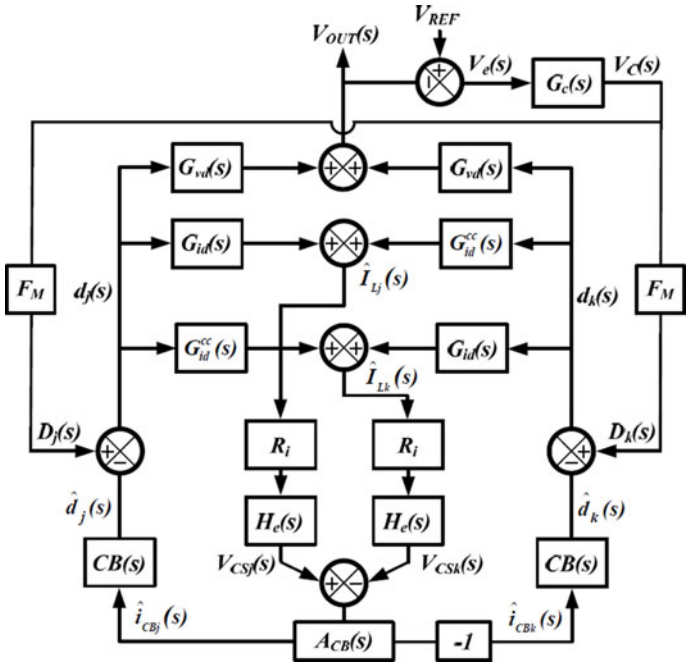

Fig. 13. Complete equivalent model of proposed TSCB VRM with the time-sharing technique and cross coupling effect.

Based on (15), (16), and (17), the duty cycle variation of the RACB method is given by

$$\hat{d}_i(s) = d_i(s) - D_i(s) \approx D(s)\frac{\Delta V_{\rm Mi}}{V_M} = \frac{D(s)\hat{i}_{{\rm CB}i}(s)T_s}{2V_M C_{\rm ramp}}$$
$$\text{where } i = 1,\ 2,\ 3,\ \text{or } 4 \text{ and } D_1(s) = D_2(s) = D_3(s)$$
$$= D_4(s) = D(s). \quad (18)$$

Again, the control-current-to-duty transfer function of RACB, $CB_{\rm RA}(s)$, is defined by the ratio of $\hat{d}_i(s)$ to $\hat{i}_{{\rm CB}i}(s)$ and can be described as

$$CB_{\rm RA}(s) \equiv \frac{\hat{d}_i(s)}{\hat{i}_{{\rm CB}i}({\rm s})} = \frac{D(s)T_s}{V_M C_{\rm ramp}} \text{ where } i = 1,\ 2,\ 3 \text{ or } 4. \quad (19)$$

Except for predefined parameters, which include V_M, $C_{\rm ramp}$ and T_s, the duty cycle, which changes with different VID code, alters control-current-to-duty transfer function of the RACB method. In other words, $CB_{\rm RA}(s)$ is proportional to the duty cycle and corresponds to the phenomenon described in Fig. 7. Comparing $CB_{\rm ts}(s)$ in (14) and $CB_{\rm RA}(s)$ in (19), the proposed TSCB technique conquers the unstable issue over a wide output voltage range. High current loop gain can be adopted to guarantee high current balance performance without being limited by the stability issue.

C. System Stability Analysis

Complete equivalent model of the proposed TSCB VRM with time-sharing technique and cross coupling effect is shown in Fig. 13. There contains voltage regulation control loop, current balance control loop, and cross coupling loop. Voltage regulation control loop regulates output voltage according to different

VID code at different load currents, while current balance control loop eliminates current unbalance phenomena caused by mismatches between different phases. In addition, cross coupling effect, which is modeled by cross coupling loop, is required to be considered since the inductor current in one phase is inevitably affected by the change in duty cycle of any other phase [20]. In other words, the duty cycle modulation of one phase may affect the current in the others through output node, $V_{\rm OUT}$. Moreover, the complete equivalent model in Fig. 13 is greatly simplified from four-phase to two-phase operation by time-sharing technique. Even though four phases provide energy to output simultaneously, only two selected channel currents, $\hat{I}_{Lj}(s)$ and $\hat{I}_{Lk}(s)$, are sent into current balance loop in one time slot. This time-sharing technique not only eliminates the offset induced by current balance loop but also largely decreases the complexity in loop analysis.

The voltage regulation control loop can be expressed in (20) regardless of phase number because the duty cycle of each phase is the same, i.e., $D_j(s) = D_k(s) = D(s)$ in Fig. 13

$$T_v(s) = G_c(s) F_M G_{vd}(s). \tag{20}$$

In current balance control loop, the duty-to-output-current transfer function of each phase is calculated in (21) by passive components

$$G_{id}(s) = \frac{I_{Li}(s)}{d_i(s)} = V_{\rm IN}(s) \frac{1 + sC\left(R_L + R_{\rm esr}\right)}{s^2 {\rm LCR}_1 + s\omega_0 Q_0 + R_{\rm DCR} + R_L}$$
$$\text{where } \omega_0\ Q_0 = L + C\left[R_L(R_{\rm DCR} + R_{\rm esr})\right] + R_{\rm DCR} R_{\rm esr}$$
$$\text{and } R_1 = R_L + R_{\rm esr} \tag{21}$$

where $R_{\rm esr}$ and $R_{\rm DCR}$ are equivalent series resistance (ESR) of output capacitor and direct current resistance (DCR) of inductor, respectively.

In cross coupling loop, the cross coupling duty-to-current transfer function, $G_{id}^{cc}(s)$, is calculated in (22) by passive components

$$G_{id}^{cc}(s) = -V_{\rm IN}(s) \frac{R_L(1 + sCR_{\rm esr})}{(sL + R_{\rm DCR})} \cdot \frac{1}{s^2 LCR_1 + s\omega_{cc} Q_{cc} + R_{\rm DCR} + 2R_L}$$
$$\text{where } \omega_{cc}\ Q_{cc} = L + C\left[R_L(R_{\rm DCR} + 2R_{\rm esr})\right] + R_{\rm DCR} R_{\rm esr}$$
$$\text{and } R_1 = R_L + R_{\rm esr}. \tag{22}$$

The cross coupling loop of the RACB and the TSCB techniques can be expressed as

$$T_{cc,ts}(s) = -A_{CB}(s) CB_{ts}(s) G_{id}^{cc}(s) R_i H_e(s) \tag{23}$$
$$T_{cc,RA}(s) = -A_{CB}(s) CB_{RA}(s) G_{id}^{cc}(s) R_i H_e(s). \tag{24}$$

However, the analysis of current balance control loop is more complex. It is noticed that a stable current balance control loop will not influence the output voltage. The operation of current balance loop is independent of load current. Instead, current balance loop relies on the difference of inductor currents. Therefore, $\hat{V}_{\rm OUT}(s)$ can be regarded as shorted to ground. The

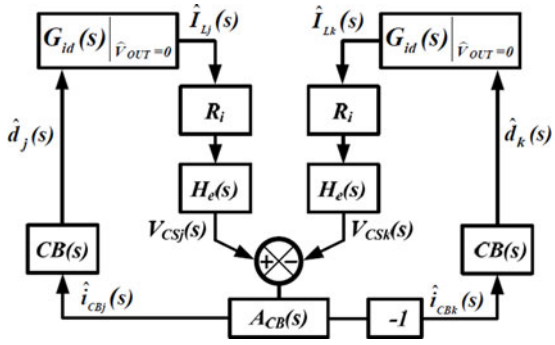

Fig. 14. Equivalent model of simplified current balance control loop with time-sharing.

duty-to-current transfer function is simplified to

$$G_{id}(s)|_{\hat{V}_{\rm OUT}=0} = V_{\rm IN}(s) \cdot \frac{1}{sL + R_{\rm DCR}}. \tag{25}$$

With shorted output, cross coupling duty-to-current transfer function is equal to zero as shown in (26). Both voltage loop and cross coupling loop will not affect the operation in current balance control loop. Therefore, the equivalent model of current balance control is further simplified to Fig. 14

$$G_{id}^{cc}(s)|_{\hat{V}_{\rm OUT}=0} = 0. \tag{26}$$

The small signals in the two phases are the same in magnitude and opposite in phase because the TSCB technique is based on the average current balance control [8]. That is, $\hat{i}_{CBj}(s) = -\hat{i}_{CBk}(s), \hat{d}_j(s) = -\hat{d}_k(s)$, and $\hat{I}_{Lj}(s) = -\hat{I}_{Lk}(s)$. Consequently, the two loops of the two phases become symmetric and can be added together. Finally, current balance control loop gain can be derived in (27) and (28) with the proposed TSCB technique and conventional RACB technique, respectively

$$T_{cb,ts}(s) = 2A_{\rm CB}(s) CB_{ts}(s) G_{id}(s)|_{\hat{V}_{\rm OUT}=0} R_i H_e(s) \tag{27}$$

$$T_{cb,RA}(s) = 2A_{\rm CB}(s) {\rm CB}_{\rm RA}(s) G_{id}(s)|_{\hat{V}_{\rm OUT}=0} R_i H_e(s). \tag{28}$$

Fig. 15(a) shows the simulated Bode plot of the voltage regulation loop, $T_v(s)$, current balance control loop, $T_{\rm cb,ts}(s)$, and cross-coupling loop, $T_{\rm cc,ts}(s)$, with $V_{\rm IN} = 3.3$ V, $L_1 = L_2 = L_3 = L_4 = 4.7$ μF, $C_L = 4.7$ F, $D = 0.3$, $R_{\rm DCR} = 150$ mΩ, $R_{\rm esr} = 30$ mΩ, $R_L = 1.8$ Ω, $T_S = 1.67$ s (per phase). In voltage regulation loop, *LC* double poles are located at 10.7 kHz. Since PID compensation inserts one dominate pole and two zeros to cancel *LC* double poles, voltage regulation loop is stable with the dc gain, phase margin and bandwidth of 91.9 dB, 50° and 30 kHz, respectively. In current balance loop, the pole generated in $G_{id}(s)|_{\hat{V}_{\rm OUT}=0}$ is located at 5.07 kHz, a pair of complex RHP zeros caused by sampling effect are located near 600 kHz. To ensure the stability of current balance loop, the dominant pole is formed by C_{Cj} and C_{Ck} in Fig. 10 which is also the dominant pole of cross-coupling loop. Thus, the dc gain, phase margin and bandwidth in current balance loop are 39.2, 46° and 3.99 kHz, respectively. The dc

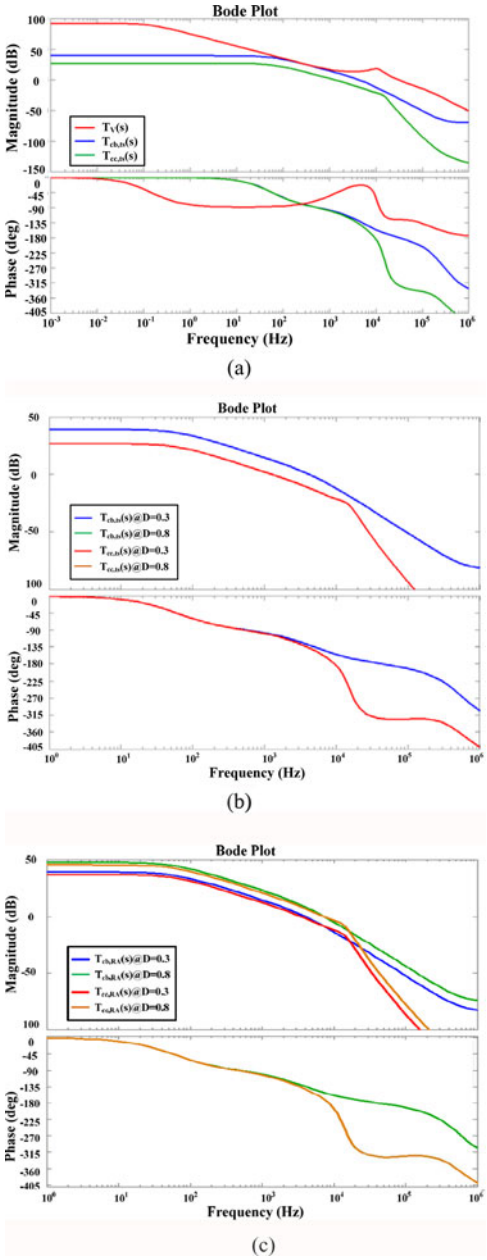

Fig. 15. (a) Simulated Bode plot of voltage, current balance and cross-coupling loops with the designed parameters. (b) Frequency response comparison of current balance and cross-coupling loop in the TSCB at different duty cycle conditions. (c) Frequency response comparison of current balance and cross-coupling loop in the RACB at different duty cycle conditions.

gain, phase margin and bandwidth in cross-coupling loop are 26.8, 76° and 1.27 kHz, respectively.

To demonstrate high stability of the proposed TSCB technique, frequency response comparison of current balance and cross-coupling loop in TSCB and RACB techniques are simulated in Fig. 15(b) and (c), respectively. When duty cycle is 0.3, the frequency response of TSCB and RACB are designed to be the same, whose dc gain, phase margin and bandwidth in current balance loop and cross-coupling loop are (39.2, 46° and 3.99 kHz), (26.8, 76° and 1.27 kHz), respectively. When duty cycle alters with the VID function, $T_{cb,ts}(s)$ and $T_{cc,ts}(s)$ remains

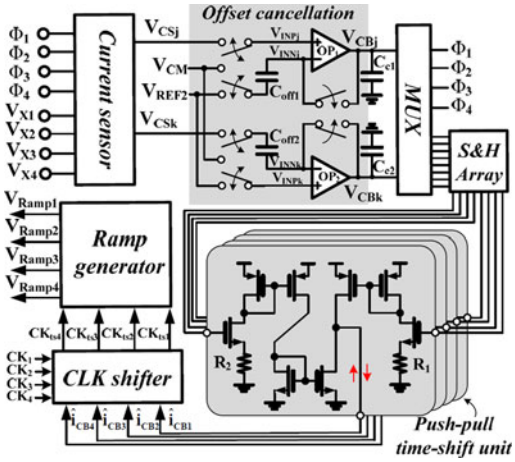

Fig. 16. Schematic of TSCB with the time-sharing technique.

the same. However, the dc gain of $T_{cb,RA}(s)$ and $T_{cc,RA}(s)$ is proportional to duty cycle which can be observed in (19). Therefore, the phase margin of $T_{cb,RA}(s)$ becomes 29°, which is not enough. The transient response performance is deteriorated. More seriously, phase margin may be smaller than 0° and the system is unstable if power, voltage, temperature (PVT) variations are taken into consideration. Therefore, the proposed TSCB technique can conquer this problem and ensure current balance performance and stability over a wide output range. The frequency responses are summarized in Table I.

In the design consideration of the three loops, voltage loop must dominate the whole operation of multiphase system to ensure voltage regulation. Therefore, the gain of voltage loop is required to be higher than current balance loop and cross-coupling loop. Ideally, the bandwidths of both loops are desired to be as large as possible to accelerate transient response. However, the enlarged bandwidth of the current balance loop slows down load transient response because of the lack of ability to rapidly increase inductor current in any of four phases. For instance, in the case of light-to-heavy load variation, one of the phases must quickly prolong the on-time to cope with the lack of energy, inevitably causing current unbalance as a consequence. Simultaneously, the current balance loop starts to pull down the unbalance inductor current. Owing to the enlarged bandwidth, suppression of the energy provided to the output will be reduced by the fast current balance loop. More switching cycles are needed to regulate the output voltage. In summary, loop gains and bandwidths of the three loops have to be carefully designed to meet the specifications.

IV. Circuit Implementation of the TSCB Technique

Fig. 16 depicts the schematic of the TSCB technique with the time-sharing technique. Current unbalance level in each channel must be estimated to shift the ramp signals accordingly to balance the channel currents of the four phases. Inductor current flowing through each channel is sensed by the current sensor to generate the current sense signals, V_{CSj} and V_{CSk}. To enhance current balance performance, operational amplifiers with the function of offset cancellation, OP_1 and OP_2 are

TABLE I
GAIN, PHASE MARGIN AND BANDWIDTH PERFORMANCE COMPARISON IN VOLTAGE, CURRENT, AND CROSS-COUPLING LOOPS WITH THE RACB AND THE TSCB TECHNIQUES IN DIFFERENT DUTY CYCLE CONDITIONS

Current balance technique		Voltage control loop (T_v(s))	Current loop ($T_{cb,RA}$(s) / $T_{cb,ts}$(s))	Cross-coupling loop ($T_{cc,RA}$(s) / $T_{cc,ts}$(s))
RACB @ D=0.3	Gain (dB)	91.9	39.2	26.8
	Phase margin (°)	51	46	76
	Bandwidth (kHz)	30	3.99	1.27
TSCB @ D=0.3	Gain (dB)	91.9	39.2	26.8
	Phase margin (°)	51	46	76
	Bandwidth (kHz)	30	3.99	1.27
RACB @ D=0.8	Gain (dB)	91.9	**47.7**	**35.3**
	Phase margin (°)	51	**29**	**54**
	Bandwidth (kHz)	30	**7.41**	**1.94**
TSCB @ D=0.8	Gain (dB)	91.9	39.2	26.8
	Phase margin (°)	51	46	76
	Bandwidth (kHz)	30	3.99	1.27

adopted to amplify V_{CSj} and V_{CSk} for generating V_{CBj} and V_{CBk}, respectively. The push–pull time-shift units, which are constituted of voltage-to-current converter, subtract V_{CBj} and V_{CBk} in current domain and generate current balance control currents, $\hat{i}_{\rm CB1}, \hat{i}_{\rm CB2}, \hat{i}_{\rm CB3}$ and $\hat{i}_{\rm CB4}$. $\hat{i}_{\rm CB1}, \hat{i}_{\rm CB2}, \hat{i}_{\rm CB3}$ and $\hat{i}_{\rm CB4}$, which indicate current unbalance levels of each phase, can shift original clock signals, CK_1–CK_4, to generate time-shifted clock signals, CK_{ts1}–CK_{ts4}, by the CLK shifter, respectively. Finally, time-shifted ramp signals, $V_{\rm Ramp1}$–$V_{\rm Ramp4}$, are generated to accomplish the TSCB technique.

Since the small amount of input referred offset voltage of OP_1 and OP_2 can be amplified to deteriorate current balance performance, input referred offset cancellation technique is embedded [21]. When CK_1, CK_2, CK_3, or CK_4 is high, the offset cancellation procedure starts. $V_{\rm INPj}, V_{\rm INPk}, C_{\rm off1}$, and $C_{\rm off2}$ are connected to common-mode reference voltage, $V_{\rm CM}$ and thus negative feedback loops of OP_1 and OP_2 are formed. Ideally, $V_{\rm INPj}$ and $V_{\rm INPk}$ are equal to $V_{\rm CM}$ and the voltages across $C_{\rm off1}$ and $C_{\rm off2}$ are zero. However, the input referred offset voltages are stored on $C_{\rm off1}$ and $C_{\rm off2}$ once offset voltage is not equal to zero. After the offset cancellation duration, OP_1 and OP_2 act as normal operational amplifiers but subtracting the offset voltage at the inputs of OP_1 and OP_2 by the offset voltage stored on $C_{\rm off1}$ and $C_{\rm off2}$. Therefore, the current balance performance of the TSCB can be ensured.

Even though the TSCB can detect current unbalance situation and average the channel currents, mismatches between current balance circuits, which includes current sensors, operational amplifiers and push–pull time-shift units, will induce irretrievable unbalance situation. Therefore, time-sharing technique is proposed to solve this problem. Time-sharing technique divides time domain into four time slots, Φ_1, Φ_2, Φ_3 and Φ_4. In Φ_1, currents of phases 1 and 2 are sent in to the TSCB circuit to balance the currents of phases 1 and 2. Similarly, currents of phases 2 and 3, 3 and 4, or 4 and 1 are sent in to the TSCB circuit in Φ_2, Φ_3, and Φ_4, respectively. Finally, current in each phase approaches to the average inductor current with the advantage of mismatch elimination between current balance circuits.

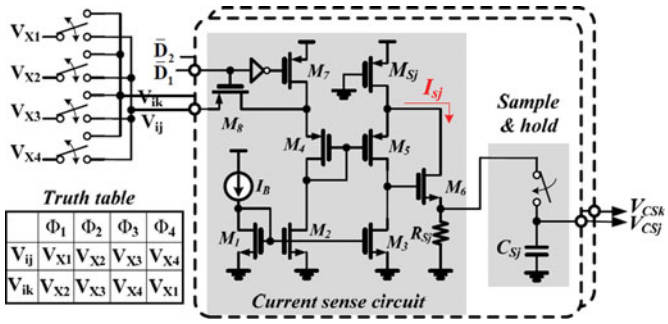

Fig. 17. Circuit implementation of current sensor.

Fig. 17 shows circuit implementation of current sensor which contains current sense circuit and sample-and-hold circuit. The power transistors, M_{P1}–M_{P4}, in Fig. 4 conduct the inductor current during its turn-on periods. The common-gate amplifier, which is composed of M_4–M_6, can ensure near source-to-drain voltages between the M_{P1}, M_{P2}, M_{P3}, or M_{P4} and the sensing MOSFET, $M_{\rm Sj}$ or $M_{\rm Sk}$. Thus, the sensing currents $I_{\rm sj}$ and $I_{\rm sk}$ as replicas of the inductor current depend on the aspect ratio between M_{P1}, M_{P2}, M_{P3} or M_{P4} and $M_{\rm Sj}$ or $M_{\rm Sk}$, respectively. $I_{\rm sj}$ and $I_{\rm sk}$ flow through sensing resistors, $R_{\rm Sj}$ and $R_{\rm Sk}$, respectively, to carry out the current sensing signals. Followings are sample-and-hold circuits to obtain $V_{\rm CSj}$ and $V_{\rm CSk}$ which include inductor current information.

Fig. 18 shows the schematic of the four-phase clock generator. Fixed frequency generator produces a clock signal, *CK*, by charging and discharging the capacitor, $C_{\rm CK}$. Clock signals of the four phases, CK_1–CK_4, can be generated by logic circuits in Fig. 18. Fig. 19 illustrates the schematic of CLK shifter in the TSCB. Current balance control currents, $\hat{i}_{\rm CB1}$–$\hat{i}_{\rm CB4}$, which generate by push–pull time-shift unit are sent into the CLK shifter to adjust the charging time of C_{ts1}–C_{ts4}, in each period. Thus, the negative edges of CK_1–CK_4 are shifted to be leading or lagging for generating CK_{ts1}–CK_{ts4}. $V_{\rm Ramp1}$–$V_{\rm ramp4}$ are modulated by shifting the clock signals, CK_1–CK_4, according to $\hat{i}_{\rm CB1}$–$\hat{i}_{\rm CB4}$.

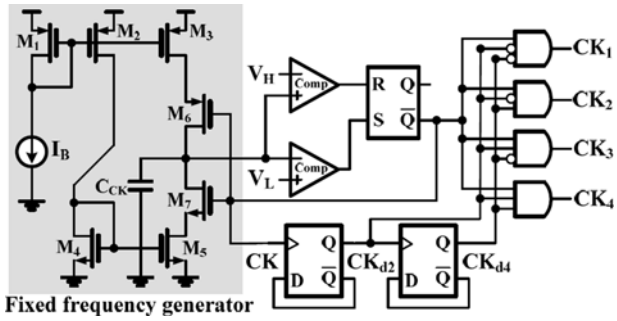

Fig. 18. Schematic of four-phase clock generator.

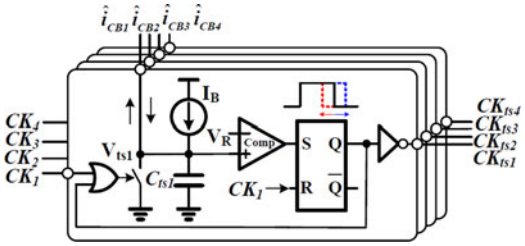

Fig. 19. Schematic of CLK shifter in the TSCB.

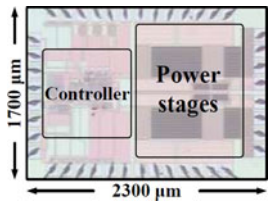

Fig. 20. Chip photo of the proposed VRM with the TSCB technique.

Since the converter output voltage dependent control and the channel current dependent control are separated into the error signal, V_C, and the time-shifted ramp signals, V_{Ramp1}–V_{ramp4}, respectively, two feedback loops can be manipulated in conformity with different requirements. In the voltage feedback loop, a high dc gain error amplifier, *EA* in Fig. 10 is adopted to meet high regulation accuracy requirement of servers. The frequency response is compensated by the compensation networks with PID or PI in voltage-mode or peak current-mode, respectively. In the current feedback loop, current balance performance is managed by the dc gain of OP_1–OP_2 in Fig. 16. C_{c1} and C_{c2} in Fig. 16 form the compensation network for the TSCB technique. Voltage feedback loop and current feedback loop are well-compensated to ensure the stability of the cloud computing VRM with the TSCB.

V. Experimental Results

TSCB technique for cloud computing VRM prototype was fabricated in TSMC 0.25 μm CMOS process. The output filters are $L_1 = L_2 = L_3 = L_4 = 4.7\mu H$ and $C_L = 47\mu F$. ESRs of filter inductor and capacitor are 150 and 30 m·Ω nominally. Input voltage is 3.3 V. The switching frequency is 600 kHz per phase. The maximum load current is scaled down to 2 A owing to limited silicon area. Fig. 20 demonstrates the chip photo of

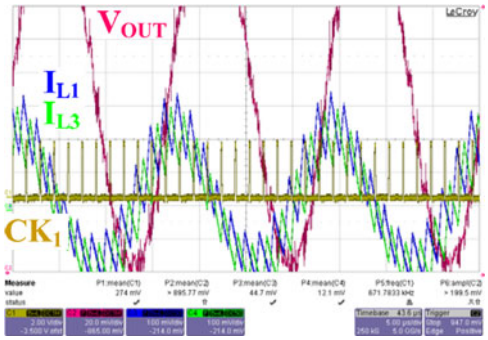

Fig. 21. Measured results of conventional RACB $V_{\mathrm{OUT}} = 950$ mV and $I_L = 0$ A.

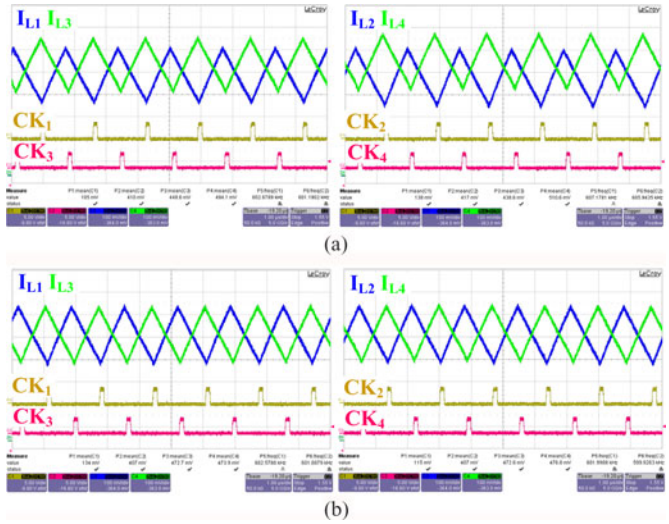

Fig. 22. Measured results of the proposed cloud computing VRM (a) without and (b) with the TSCB technique when $V_{\mathrm{OUT}} = 950$ mV and $I_L = 2$ A.

the proposed VRM with TSCB technique. Fig. 21 shows the measured results of conventional RACB when output voltage is set to 950 mV and total load current is set to 0 A. The channel currents are oscillating and output voltage cannot be regulated. By adopting the proposed TSCB technique in cloud computing system, the output voltage is regulated at 950 mV and the load current can increase to 2 A, which is the maximum load of the proposed prototype, for the servers as demonstrated in Fig. 22. The clock signals, CK_1–CK_4, which are interleaved, control the timing of the VRM system. Without the TSCB, unequal distribution of the channel currents is caused by the mismatches between phases intrinsically. Four channel currents are 448.6, 438.6, 494.1, and 510.6 mA as shown in Fig. 22(a). When the TSCB is adopted, the current difference of the four phases is suppressed as shown in Fig. 22(b) and the channel currents are 472.7, 472.6, 473.9, and 476.8 mA. The TSCB technique is proved to achieve good current balance performance by decreasing 94.1% of the current unbalance. The load transient response from 0 to 800 mA with $V_{\mathrm{OUT}} = 950$ mV is shown in Fig. 23. It shows that current balance can be ensured during both transient response and steady-state.

To demonstrate VID function, Figs. 24 and 25 show the measured results of power line with different VID code. In Fig. 24,

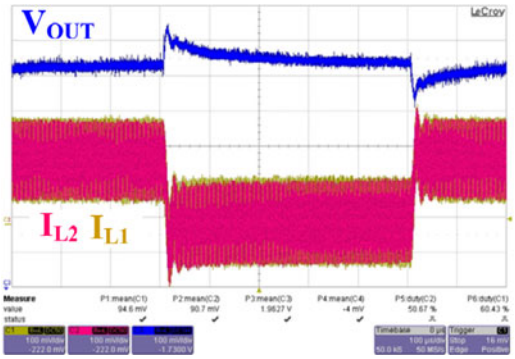

Fig. 23. Measured load transient response from 0 to 800 mA with $V_{\rm OUT}$ = 950 mV.

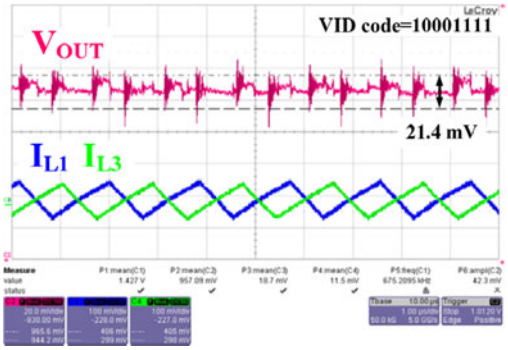

Fig. 24. Measured results when $V_{\rm REF}$ = 0.96 V where the 8-bit VID code is equal to "10001111" accordingly.

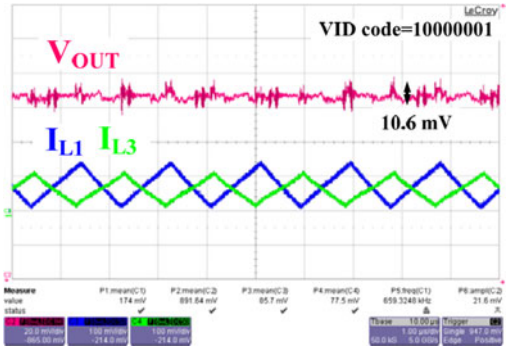

Fig. 25. Measured results when $V_{\rm REF}$ = 0.89 V where the 8-bit VID code is equal to "10000001" accordingly.

the reference voltage, $V_{\rm REF}$, is set to 0.96 V, i.e., the 8-bit VID code is "10001111." The voltage of power line, $V_{\rm OUT}$, which is controlled by the voltage feedback loop, follows the $V_{\rm REF}$ and regulates at 0.96 V. The ripple of $V_{\rm OUT}$ is synthesized by the four interleaved current ripples and suppressed to 21.4 mV. As shown in Fig. 24, the $V_{\rm OUT}$ is regulated at 0.89 V by adjusting the 8-bit VID code to "10000001." Since the duty cycle is close to 50%, the ripple of $V_{\rm OUT}$ is further decreased. Fig. 26 shows the measured frequency response of the proposed TSCB technique when $V_{\rm OUT}$ = 950 mV and I_L = 2 A. The dc gain, phase margin and bandwidth in voltage regulation loop, current balance loop, and cross-coupling loop are (91 dB, 48°, 35 kHz), (42.1 dB, 50°, 9.2 kHz), and (28.3 dB, 70°, 2.75 kHz).

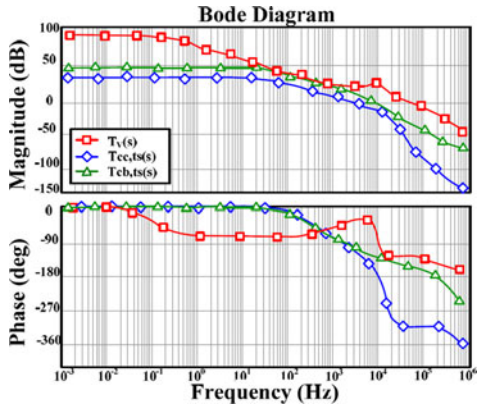

Fig. 26. Measured Bode plot of the voltage regulation loop, current balance control loop, and cross-coupling loop in the TSCB technique when $V_{\rm OUT}$ = 950 mV and I_L = 2 A.

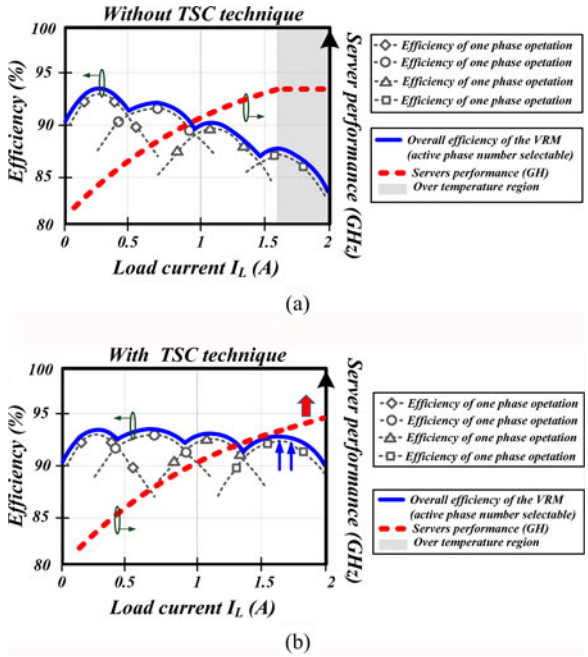

Fig. 27. Efficiency and server performance versus load current of the VRM for the servers without the TSCB technique in (a) and with the TSCB technique in (b).

Performance improvement is shown in Fig. 27. The efficiency curves of adopting one to four phases are illustrated. According to different load conditions, active phase number is properly selected by the server and sent to the VRM for high efficiency over a wide load range. Without the TSC, current unbalance level becomes larger at heavy loads and thus deteriorates the efficiency. Most of load current flows through one of the four channels and increases the temperature. To prevent the damage of VRM, load current which is larger than 1.6 A is unable to be provided in extremely unbalance situation. Thus, the operation frequency and performance of the server in stable operation are limited. After adopting the TSCB, the efficiency of the VRM is promoted to over 90% over the whole load range. The maximum load current is consistent with the designed value and the performance of the server is improved.

VI. Conclusion

A cloud computing VRM with the TSCB technique is proposed for large current demand from high performance servers. The functions of active phase number section and voltage VID are embodiment additionally. The proposed TSCB technique conquers the stability issue in all conditions in conventional RACB. Moreover, time-sharing mechanism eliminates undetectable offset voltage in current balance loop to further improve current balance performance. The prototype with four-phase operation and 2 A maximum load current is implemented in TSMC 0.25 μm CMOS process. By decreasing 94.1% of current unbalance caused by the mismatches of the four phases, the current balance performance of the TSCB technique is confirmed. The infallible of voltage regulation according to different reference voltage realizes the VID function.

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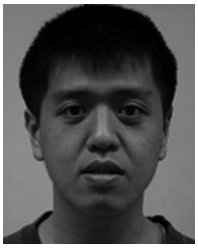

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