Small-Signal Analysis and Optimal Design of Constant Frequency V^2 Control

Shuilin Tian, *Student Member, IEEE*, Fred C. Lee, *Life Fellow, IEEE*, Paolo Mattavelli, *Senior Member, IEEE*, and Yingyi Yan, *Member, IEEE*

***Abstract*—Recently, V^2 control and its variety named ripple-based control has been gaining more and more popularity in academia research and commercial products. However, for constant frequency V^2 control, design methodology is not clear due to insufficient knowledge about the small-signal model. This paper investigates the small-signal model and optimal design strategy for constant frequency V^2 control. The factorized small-signal control-to-output voltage transfer function and output impedance are investigated. The stability criterion is obtained and design considerations are analyzed. Moreover, the small-signal model with ramp compensations is presented and optimal design guidelines from dynamic performance point of view are provided. For the first time, it is found the external ramp is good enough to get a well-damped performance when current feedback strength is strong (for example, when employing OSCON capacitors). However, the current ramp is necessary to achieve a good dynamic performance when the current feedback strength is weak (for example, when employing ceramic capacitors). As a result, a new control strategy with the hybrid ramp is proposed for ceramic capacitor applications. The small-signal model and proposed design guidelines are verified with Simplis simulation and experimental results.**

***Index Terms*—Constant frequency V^2 control, current ramp, dynamic performance, external ramp, ripple-based control, small-signal model, stability criterion.**

I. Introduction

RECENTLY, V^2 control architecture [1], [2], and its variety named ripple based control, as shown in Fig. 1, has been widely applied in point of load Buck converters. Compared with the traditional voltage mode control or current mode control, this control structure has the following three features: 1) no current sensing network is required; 2) fast load transient characteristics with direct output voltage feedback; and 3) the outer-loop compensator is much simpler, usually a simple integrator with low bandwidth is adequate.

The outer-loop compensation is shown as a dashed line in Fig. 1 as the integrator can be further eliminated in many applications, which is called ripple-based control in some literature [3], [4].

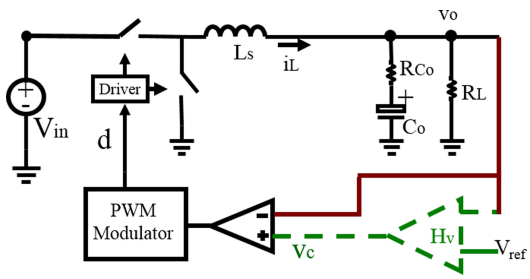


Fig. 1. Structure of V^2 control (with outer loop compensator shown in dashed line) and ripple-based control (without outer loop compensator).

However, the output voltage does not only include the current information, but also the capacitor voltage, which has a 90° additional phase delay. This additional phase delay will cause subharmonic oscillation in a case where the capacitor voltage overwhelms the current information, for example, when a ceramic output capacitor is used. Depending on the different modulation schemes, there are several V^2 control structures, such as constant frequency V^2 control including peak control [13]–[19], [21] and valley control [20], [22], [31], and variable frequency V^2 control including constant on-time V^2 control [10]–[12], [33] and constant off-time V^2 control [1], [2]. Among these four schemes, constant on-time V^2 control [5]–[7] and constant frequency V^2 peak control [8], [9] are the two most popular structures in commercial products.

For constant on-time V^2 control, several technical papers have been published about the small-signal model, analysis, and optimal design strategy. In [10], the control-to-output voltage transfer function and output impedance are derived for constant on-time V^2 control based on the describing function method, which is accurate over all frequency ranges. The stability criterion is obtained for both constant on-time V^2 and enhanced V^2 control. In [11] and [12], design guideline of the external ramp is provided to solve the instability problem and optimize the dynamic performance when employing ceramic capacitors, based on an easy-to-use factorized small-signal model. It was found that external ramp is a simple solution for small duty-cycle application, while for large duty-cycle application, only an external ramp cannot provide a well-damped performance. In [32] and [33], a digital constant on-time ripple-based control with a hybrid ramp (external ramp and inductor current ramp) for voltage regulator module (VRM) application is proposed and design guidelines are presented based on the factorized small-signal model. The small-signal model and design

Manuscript received December 31, 2013; revised March 10, 2014; accepted April 25, 2014. Date of publication April 29, 2014; date of current version October 15, 2014. This work was supported by the Power Management Consortium in the Center for Power Electronics Systems, Virginia Tech. Recommended for publication by Associate Editor Y.-M. Chen.

S. Tian, F. C. Lee, and Y. Yan are with the Center for Power Electronics Systems, The Bradley Department of Electrical and Computer Engineering, Virginia Tech, Blacksburg, VA 24061 USA (e-mail: tianshuilinpe@gmail.com; fclee@vt.edu; yanyingyi@gmail.com).

P. Mattavelli is with DTG, University of Padova, Italy (e-mail: pmatta@vt.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2014.2320980

strategy for constant on-time V^2 control is, therefore, clarified to industry engineers with the help of these research efforts.

For constant frequency V^2 control, although there are several papers published discussing the small-signal analysis and design considerations [3], [4], [14]–[17], [22], more research efforts are still required for a complete understanding and optimal design purpose. In [14]–[17], the small-signal models are not accurate since these models are the extensions from the modified average model of peak current mode control in [23], which is based on the result from sample-data model in [24] and does not consider the influence of the capacitor voltage feedback. In [4], the Krylov–Bogoliubov–Mitropolsky technique is used to improve the accuracy of the small-signal model. However, this technique is too complex for practical use. In [3], the sampled-data modeling technique is employed. It can accurately predict the stability criterion of constant frequency V^2 peak control. However, only the critical stability point can be predicted and no design guideline can be provided with a certain stability margin. In [22], accurate analysis based on the discrete-time modeling and Floquet theory is presented. However, it is based on numerical analysis, and no symbolic expression can be extracted and very little physical insight is provided. In [10], the continuous small-signal model is derived based on the describing function method, the model is very accurate, as all the nonlinearity is included in this modeling strategy. However, the results for constant frequency V^2 control are nonfactorized fourth-order equations, which are difficult for a thorough analysis. As a result, no explicit stability criterion and design strategy is given, and therefore, the engineers have no clue on design strategy to improve the dynamic performance.

The research goal of this paper is to provide an optimal design strategy by a thorough investigation of the small-signal model for constant frequency V^2 control. The physical causation of two pairs of double poles is identified and explicit stability criterion is presented. Stability margin can be easily controlled by controlling the quality factor of double poles. For the first time, it is found that different design strategies should be used with different capacitors. For OSCON capacitors, designing an external ramp appropriately is adequate, while for ceramic capacitors an additional current ramp is required to control the stability margin. This paper will mainly focus on constant frequency V^2 peak control, but the analysis is also applicable to constant frequency V^2 valley control based on the duality principle. The remaining of this paper is organized as follows: The factorized small-signal model for constant frequency V^2 peak control is presented in Section II. Current feedback strength is defined and physical causation of double poles is identified. In Section III, the small-signal model with external ramp compensation is presented and the design guideline of an external ramp from the dynamic performance point of view is provided. In Section IV, a new control strategy with the hybrid ramp (external ramp and current ramp) is proposed for ceramic capacitor applications and design guidelines are presented. Simulation and experimental results for the small-signal model and load transient performance are shown in Section V. Finally, a summary is given in Section VI.

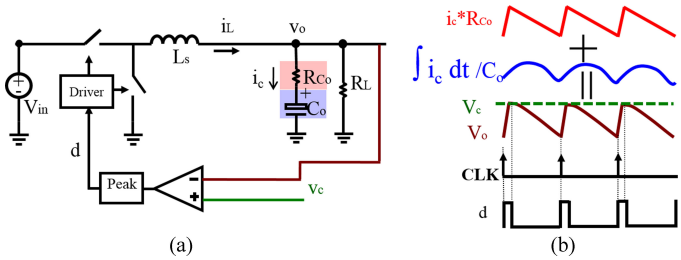


Fig. 2. Constant frequency V^2 peak control (a) circuit diagram; (b) steady-state waveform.

II. Small-Signal Analysis and Design Considerations Without Ramp

Fig. 2(a) shows the circuit diagram of a constant frequency V^2 peak control, and Fig. 2(b) illustrates the steady-state waveforms. The turn-on point is determined by the clock signal, while the turn-off point is determined the comparison of the output voltage and control signal (or reference voltage in ripple-based control). Note that, in Fig. 2(b), equivalent series inductance (ESL) of the output capacitor is neglected. As the steady-state waveform of ESL ripple is a constant positive value during on-time and a constant negative value during off-time, it just provides a bias for the total output voltage. As a result, it does not affect the decision point of feedback control and has no relation to the control stability.

The output voltage ripple contains two parts: equivalent series resistance (ESR) ripple and capacitor voltage ripple. The capacitor voltage ripple is integration of the capacitor current, which has 90° of additional phase delay. Intuitively, the influence of this additional phase delay is dependent on the magnitude of capacitor ripple voltage relative to the ESR ripple. For the purpose of quantification analysis, current feedback strength is defined as follows.

A. Definition of Current Feedback Strength α and its Physical Meaning

The ratio of the ESR ripple magnitude over the cap voltage ripple magnitude is shown as follows:

$$\frac{\Delta v_{\rm ESR}}{\Delta v_{Co}} = \frac{R_{Co}\Delta i_L}{\frac{1}{8C_o}\Delta i_L T_{\rm sw}} = \frac{8R_{Co}C_o}{T_{\rm sw}} = 8\alpha \tag{1}$$

where current feedback strength α is defined as

$$\alpha = \frac{R_{Co}C_o}{T_{\rm sw}} = \frac{1}{2\pi}\frac{f_{\rm sw}}{f_{\rm esr}}. \tag{2}$$

It can be seen from the aforementioned equation that α represents the relative strength of the current feedback: The larger the α value, the larger the ESR ripple when compared with the capacitor voltage ripple. From a design point of view, (2) also states that α is the ratio of switching frequency over ESR zero frequency. For the typical capacitor, the values of α are shown in Table I.

Table I shows that the current feedback strength is relatively large when using the OSCON and SP capacitors with a typical

TABLE I
VALUES OF CURRENT STRENGTH A WITH VARIOUS CAPACITORS

Cap Type	Cap Parameters	F_{sw}(Hz)	F_{esr}/F_{sw}	α	$\Delta V_{esr}/\Delta V_{co}$
OSCON	6mΩ/560uF	300k	≈ 1/6	≈ 1	≈ 8
SP	6mΩ/330uF	300k	≈ 1/4	≈0.6	≈ 5
Ceramic	1.4mΩ/100 uF	300k	≈ 4	≈0.04	≈0.3
		4.2M	≈ 1/4	≈0.6	≈ 5

300-kHz switching frequency, while it is very small for ceramic capacitors. It also shows that the switching frequency needs to be increased to 4.2 MHz for ceramic capacitors so that it has the same current feedback strength as the SP capacitors with a 300-kHz switching frequency. The importance of α is shown in the following analysis of the small-signal model.

B. Small-Signal Control-to-Output Voltage Transfer Function Analysis

The accurate continuous small-signal model is shown based on the describing function method in [10]. Using Pade approximation, the small-signal model is simplified and accurate up to switching frequency, as shown in the following:

$$\frac{v_o(s)}{v_c(s)} \approx \frac{(R_{Co}C_o s+1)}{\left(1+\frac{s}{Q_6\omega_2}+\frac{s^2}{\omega_2^2}\right)\left(1+\frac{s}{Q_2\omega_2}+\frac{s^2}{\omega_2^2}\right)-X\cdot s^2}$$
$$Q_6=\frac{1}{\left(\frac{1}{2}+\frac{R_{Co}C_o-T_{\rm sw}}{T_{\rm sw}s_n/(s_n+s_f)+T_{\rm on}}\right)\pi},\quad Q_2=\frac{2}{\pi}$$
$$\omega_2=\frac{\pi}{T_{\rm sw}},\quad X=\frac{(s_f-s_e)R_{Co}C_o-s_fT_{\rm off}/2}{s_n+s_f}\cdot T_{\rm sw}. \tag{3}$$

Although the model in (3) is very accurate, it is difficult for analysis and little physical insight is provided since it is in a nonfactorized fourth-order form. Based on the factorization method shown in [12], the aforementioned transfer function can be factorized and the results without an external ramp are shown in the following:

$$\frac{v_o(s)}{v_c(s)} \approx \frac{(R_{Co}C_o s+1)}{\left(1+\frac{s}{Q_{e1}\omega_2}+\frac{s^2}{\omega_2^2}\right)\left(1+\frac{s}{Q_{e2}\omega_2}+\frac{s^2}{\omega_2^2}\right)}$$
$$Q_{e1}=\frac{2}{\pi}\frac{1}{\alpha+\sqrt{\alpha^2+(4D-2)\alpha+(1-D)^2+D^2}}$$
$$Q_{e2}=\frac{2}{\pi}\frac{1}{\alpha-\sqrt{\alpha^2+(4D-2)\alpha+(1-D)^2+D^2}}. \tag{4}$$

For small duty-cycle application, with simple mathematical manipulation, Q_{e1} and Q_{e2} in the aforementioned equation can be approximated and rewritten as follows:

$$Q_{e1}\approx\frac{1}{\pi}\frac{1}{D'-0.5},\quad Q_{e2}\approx\frac{1}{\pi}\frac{1}{\alpha-0.5}. \tag{5}$$

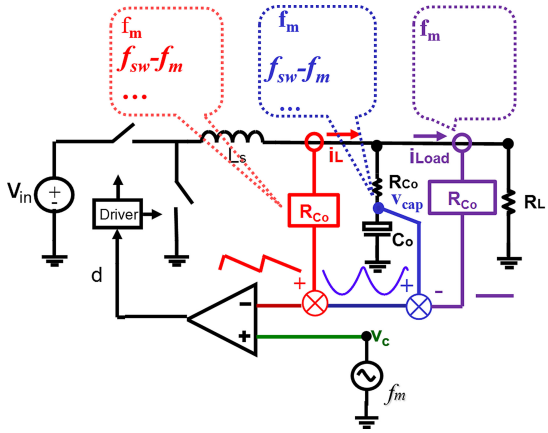


Fig. 3. Frequency spectrum in V^2 control with separated feedback information.

To explain why there are two pairs of double poles at half of switching frequency and to relate V^2 control with well-understood peak current mode control, the feedback information is separated into three parts, which is proposed in the equivalent circuit models of V^2 control [28]–[30]: inductor current feedback, capacitor voltage feedback, and load current feedback, as shown in Fig. 3.

The inner current loop is a peak current mode control loop. When the control signal is perturbed with modulation frequency f_m, sideband components $f_s - f_m$, and $f_s + f_m$ are generated through the PWM modulator. Therefore, the inductor current not only contains the fundamental frequency component f_m, but also switching frequency and its sideband components. By closing the current loop, one pair of double pole, which is located at half of switching frequency shows up. The quality factor Q_{e1} is related to duty cycle, as in the peak current mode case. Note that, the expression Q_{e1} shown in (5) is the same as the expression of Q of the double pole in peak current mode control shown in [23], [25], and [26].

However, for constant frequency V^2 peak control, there is additional capacitor voltage feedback loop and load current feedback loop, as shown in Fig. 3. The capacitor voltage loop is a direct feedback without any compensation. When low-ESR caps are employed, the switching frequency component is very rich and it will participate in modulation, therefore, the sideband frequency components of capacitor voltage in general also needs to be taken into consideration. The essential difference between V^2 control and current mode control is that the sidebands of capacitor voltage also participate in modulation. As a result, another pair of double pole, which is also located at half of switching frequency shows up and the quality factor Q_{e2} is related to the current feedback strength α, as shown in (5).

The effect of the current feedback strength α can be clearly seen in (5), as the quality factor Q_{e2} is related to α. For illustration purpose, with different types of output capacitors, the comparisons of pole zero maps and Bode plots for control-to-output voltage transfer function under $D = 0.1$ and $f_{\rm sw} = 300$ kHz are shown in Fig. 4. With smaller α, the capacitor voltage feedback is stronger, which means the phase-delay effect is more severe,

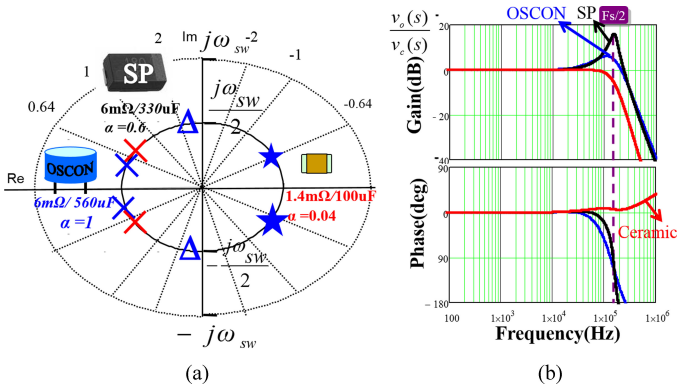


Fig. 4. Comparisons between OSCON, SP, and ceramic capacitors with $D = 0.1$ and $f_{\rm sw} = 300$ kHz. (a) Pole-zero maps. (b) Control-to-output voltage transfer function.

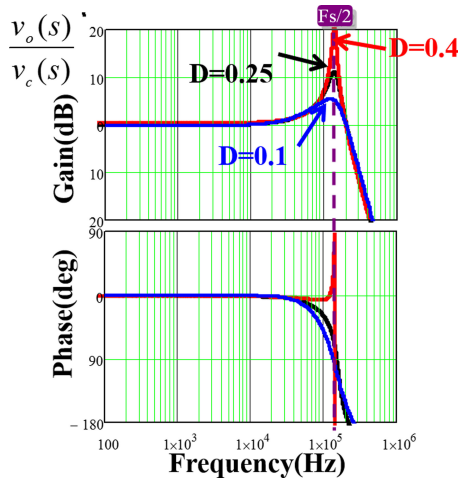


Fig. 5. Comparison of Bode plots of control-to-output voltage transfer function for OSCON capacitors with 300-kHz switching frequency and different duty cycles.

and the circuit is more unstable. Comparing SP capacitor with OSCON capacitor, the second pair of double poles has a larger quality factor and the peaking is larger. For ceramic capacitor, since α is 0.04 with a 300-kHz switching frequency, which is smaller than 0.5, the double pole locates on right-half-plane, which means that the circuit is unstable.

Duty cycle is related with the sample-and-hold effect in peak current mode control [23]. As peak current control loop still exists in constant frequency V^2 peak control, duty cycle also impacts the control-to-output voltage transfer function, as it affects Q_{e1} and Q_{e2} shown in (4). To illustrate this point, the Bode plots of control-to-output voltage transfer function for OSCON caps with $f_{\rm sw} = 300$ kHz and different duty cycles are shown in Fig. 5. When D is larger, the peaking at half of switching frequency is larger, which indicates a smaller stability margin. The phenomenon is the same with respect to peak current mode control: when D is larger, the sample-and-hold effect of the current loop is stronger and the stability is worse. However, the difference is that in constant frequency V^2 peak control, the additional capacitor voltage phase delay affects the stability and instability may happen before $D = 0.5$. As shown in Fig. 5, when $D = 0.4$, the phase plot goes up, which indicates that there is a right-half-plane double pole and the system is already unstable.

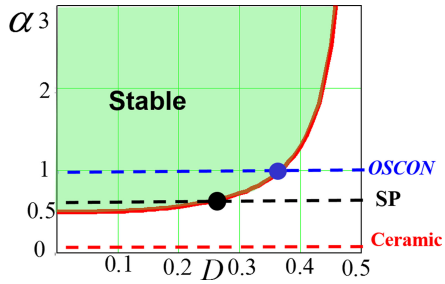


Fig. 6. Stability criterion of constant frequency V^2 peak control with $F_{\rm sw} = 300$ kHz.

C. Stability Criterion and Design Consideration

As shown previously, when D is small, the two kinds of sidebands can be decoupled, inductor current sidebands cause one pair of double pole and capacitor voltage sidebands cause another pair of double pole, as shown in (5). When D is becoming larger, the two kinds of sidebands are coupled and interacting with each other, as shown in (4). In general, the criterion for stable operation is that all the poles are located at the left half plane, or equivalently the quality factors related with the double poles are both positive. The stability criterion can then be solved from (4) as shown in the following equation:

$$D \le \frac{1}{2} - \frac{1}{2}\frac{1}{2\alpha + \sqrt{4\alpha^2 - 1}}. \tag{6}$$

The stability now is not only related to duty cycle, as in the peak current mode control, but also to the current feedback strength α, which also reflects the phenomenon that the phase delay of the capacitor voltage plays an important role in the constant frequency V^2 peak control.

Equation (6) can be represented as Fig. 6, which shows the stability criterion with respect to duty cycle and current feedback strength α. As an example, at 300 kHz, for the OSCON cap, as shown in Table I, $\alpha \approx 1$, from Fig. 6, D should be smaller than 0.37 shown as the blue point, while for the SP cap, D should be smaller than 0.23, which is the black point. For the ceramic cap, it is unstable for any D since $\alpha < 0.5$. The stability criterion shown in (6) is consistent with peak current mode control case: When α is infinite, the stability criterion reduces to $D \le 1/2$, which is a well-known stability criterion for the peak current mode control. When α is finite, the stability region of the constant frequency V^2 peak control is smaller due to the effect of the capacitor voltage feedback.

Given certain type of capacitor, α is only related to switching frequency. (6) can be rewritten as follows:

$$F_{\rm SW} \ge \frac{1}{R_{Co}C_o}\left(\frac{1}{2} + \frac{D^2}{1-2D}\right). \tag{7}$$

Table II shows the switching frequency requirement for different types of capacitors and different duty cycles, and several important points can be derived as follows.

TABLE II
SWITCHING FREQUENCY REQUIREMENT WITH DIFFERENT TYPES OF CAPS AND DUTY CYCLES

Switching Freq. Requirement			α Requirement	Duty cycle
Ceramic 1.4mΩ/100uF	SP 6mΩ/*330* uF	OSCON 6mΩ/*560* uF		
10.8M	*720k*	*430k*	α≥1.3	D=0.4
3.5M	*250k*	*150k*	α≥0.5	D=0.1

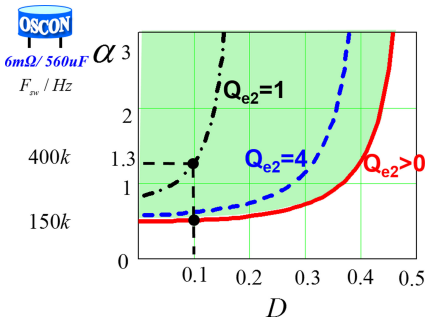


Fig. 7. Stability margin control by controlling Q_{e2}.

1) With given capacitor, higher switching frequency is required for larger duty-cycle applications. For example, with the OSCON capacitor, for 0.1 and 0.4 duty-cycle applications, the critical switching frequency is 150 and 430 kHz, respectively.
2) Given a certain duty cycle, a higher switching frequency should be used for capacitors with smaller time constants. For $D = 0.1$ case, the critical switching frequency for the OSCON, SP, and ceramic capacitor is 150, 250, and 3.5 MHz, respectively.
3) For the ceramic cap, a several Megahertz switching frequency is required to avoid instability problem, which is very challenging for practical use.

For design purpose, designing the converter to avoid the critical stability is not enough. Enough stability margin should be obtained. The same concept shown in peak current mode control [23], [25] can be adopted here in constant frequency V^2 peak control: control the quality factor of double poles. For example, choose Q_{e2} around 1 to gain enough margin. Fig. 7 shows the relations between different Q_{e2} values and parameters of duty cycle and current feedback strength α. To control Q_{e2} around 1, a larger α is required for a given duty cycle, for example, when $D = 0.1$, for critical stability, α is around 0.5, while α needs to be increased to around 1.3 to design Q_{e2} around 1. As for OSCON capacitor, the switching frequency should be around 400 kHz to control Q_{e2} around 1, compared with 150 kHz for critical stability.

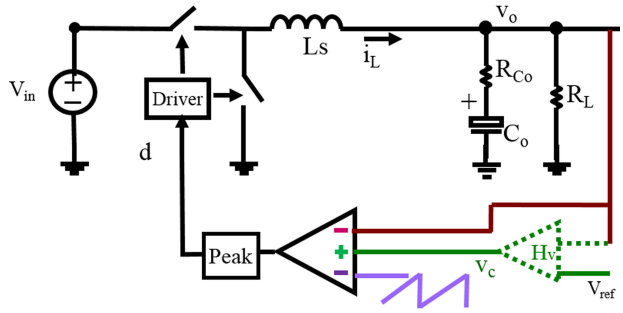


Fig. 8. Diagram of constant frequency V^2 peak control with external ramp compensation.

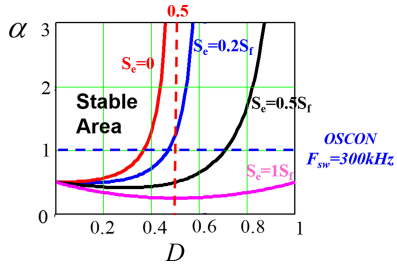


Fig. 9. Diagram of stability criterion with external ramp compensation.

III. SMALL-SIGNAL ANALYSIS AND DESIGN WITH EXTERNAL RAMP

External ramp compensation is a well-known solution to eliminate subharmonic oscillation in peak current-mode control, and this strategy can be employed to eliminate subharmonic oscillation in constant frequency V^2 peak control as well. Fig. 8 shows the circuit diagram of constant frequency V^2 peak control with external ramp compensation.

By factorizing the result in (3), the small-signal control-to-output voltage transfer function is as follows:

$$\frac{v_o(s)}{v_c(s)} \approx \frac{R_{Co}C_o s + 1}{\left(1 + \frac{s}{Q_{e1}\cdot\omega_2} + \frac{s^2}{\omega_2^2}\right)\left(1 + \frac{s}{Q_{e2}\cdot\omega_2} + \frac{s^2}{\omega_2^2}\right)}$$

$$Q_{e1} = \frac{2}{\pi}\frac{1}{\alpha + \sqrt{\alpha^2 + (4D - 2 - 4D\cdot s_e/s_f)\alpha + (1-D)^2 + D^2}}$$

$$Q_{e2} = \frac{2}{\pi}\frac{1}{\alpha - \sqrt{\alpha^2 + (4D - 2 - 4D\cdot s_e/s_f)\alpha + (1-D)^2 + D^2}}$$

$$s_f = R_{Co}\frac{V_o}{L_s}. \tag{8}$$

In (8), s_e is the external ramp slope, while s_f represents the falling slope of ESR ripple voltage. Compared with (4), it can be seen that the external ramp affects quality factors of the double poles. The minimum external ramp for critical stability can be derived by solving (8), which is shown in (9) as follows:

$$\frac{s_e}{s_f} > \left(\frac{(1-D)^2 + D^2}{4D\alpha}\right) + 1 - \frac{1}{2D}. \tag{9}$$

Fig. 9 shows the stability criterion diagram with different external ramp compensations. Note that, in Fig. 9, the horizontal axis is the whole duty-cycle range. It is obvious that with an

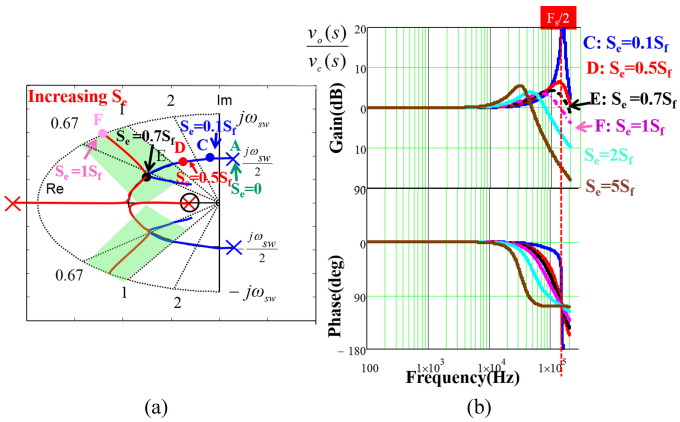


Fig. 10. (a) Pole-zero mapping and (b) Bode plots of the control-to-output voltage transfer function with increasing external ramp for OSCON capacitor with $F_{\rm sw} = 300$ kHz and $D = 0.4$.

external ramp, the stability region can be expanded: using OSCON capacitor with 300-kHz switching frequency ($\alpha \approx 1$) as an example, it is unstable when duty cycle is larger than 0.37 without an external ramp, when $S_e = 1S_f$, it is stable within all the duty-cycle range.

For optimal design purposes, external ramp should be selected appropriately to improve the dynamic performance. For illustration purpose, the pole-zero maps and Bode plots of control-to-output voltage transfer function with a series of different external ramps for an OSCON capacitor with $F_{\rm sw} = 300$ kHz and $D = 0.4$ are plotted in Fig. 10. Without an external ramp (shown as green point A), $Q_{e2} < 0$ and the circuit is unstable. With the external ramp increasing, this double pole moves toward left half plane (shown as blue point C and red point D) and meets with another double pole at black point E, which is a key point since the quality factor for Q_{e2} is the smallest during the whole trajectory. The quality factor of the key point Q_{e_k} can be derived from (8) and is expressed as follows:

$$Q_{e\_k} = \frac{2}{\pi}\frac{1}{\alpha}. \tag{10}$$

In this case, the value of Q_{e_k} is approximately $2/\pi$, which is smaller than 1. Further increasing S_e separates two pairs of double poles, one moves to a higher frequency, while the other one to a lower frequency. For design purposes, the external ramp should be designed appropriately: On one hand, it should be large enough to control quality factor for enough stability margin; on the other hand, it should not be too large, as it will slow down the transient performance by bringing a low-frequency double pole with increased quality factor [12]. The suggested area is Q around 1, which is shown as the light green shaded area in Fig. 10(a). For example, the external ramp can be chosen to make $Q_{e2} = 2/\pi$, the required ramp magnitude can

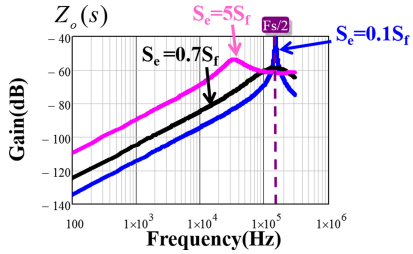


Fig. 11. Bode plots of Output Impedance with different external ramps for OSCON capacitor with $F_{\rm sw} = 300$ kHz and $D = 0.4$.

be solved from (8), as shown follows:

$$\frac{s_e}{s_f} \approx 1 - \frac{1-D}{2\alpha}. \tag{11}$$

As shown in Fig. 10, when the external ramp is too small (point C: $S_e = 0.1S_f$), the peaking is large indicating a bad dynamic performance. When the external ramp is too large ($S_e = 5S_f$), there is a low frequency dominant double pole, which slows the transient performance. Therefore, the external ramp should be designed appropriately, e.g., around $Q_{e2} = 2/\pi$, which is between point E and point F in Fig. 10(a) and between the black dashed line ($S_e = 0.7S_f$) and pink dashed line ($S_e = 1S_f$) in Fig. 10(b). The preferred external ramp, in this case is between $0.7S_f$ to $1S_f$.

From optimum transient performance point of view, it is meaningful to investigate the output impedance. The transfer function of the output impedance with external ramp compensation is also derived in [10] and shown at the bottom of the page.

The factorized output impedance is shown as follows:

$$Z_o(s) \approx \frac{-R_{Co}T_{\rm sw}\left(\frac{1}{2} - D + D\frac{s_e}{s_f}\right) * s * (R_{Co}C_o s + 1)}{\left(1 + \frac{s}{Q_{e1}\omega_2} + \frac{s^2}{\omega_2^2}\right)\left(1 + \frac{s}{Q_{e2}\omega_2} + \frac{s^2}{\omega_2^2}\right)}. \tag{13}$$

For the output impedance, the external ramp not only influences the quality factor of double poles, but also increases the low-frequency output impedance. As shown in Fig. 11, the low-frequency impedance of $S_e = 5S_f$ is much larger than $S_e = 0.1S_f$ case, while the high-frequency impedance is much lower. This is because adding too much external ramp reduces the weight of the output voltage in modulation process, which indicates reducing the ability to control the output voltage. Consider the total output impedance performance, $S_e = 0.7S_f$ is the best among the three, which is the same conclusion from the control-to-output voltage transfer function.

However, using an external ramp to improve the dynamic performance has its limitation, which is dependent on current feedback strength α. As shown in (10), when α is too small, the smallest quality factor is very large, which indicates that

$$Z_o(s) \approx \left(\frac{(R_{Co}C_o s + 1)}{\left(1 + \frac{s}{Q_6\omega_2} + \frac{s^2}{\omega_2^2}\right)\left(1 + \frac{s}{Q_2\omega_2} + \frac{s^2}{\omega_2^2}\right) - \frac{(s_f - s_e)R_{Co}C_o - s_f T_{\rm off}/2}{s_n + s_f}T_{\rm sw}\cdot s^2} - 1\right)\left(R_{Co} + \frac{1}{C_o s}\right) \tag{12}$$

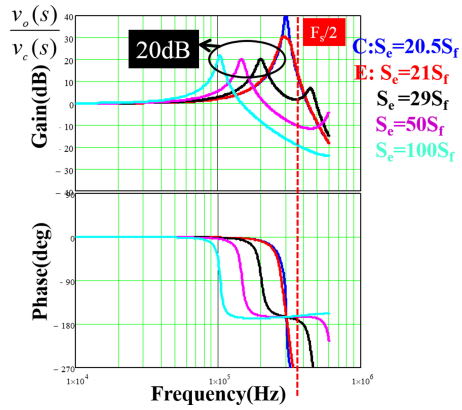


Fig. 12. Bode plots of the control-to-output voltage transfer function with increasing external ramp for ceramic capacitor with $F_{\rm sw} = 600$ kHz and $D = 0.1$.

the peaking will be large for any case. To illustrate this point, consider the ceramic capacitor with $f_{\rm sw} = 600$ kHz ($\alpha \approx 0.08$) and $D = 0.1$ case, the Bode plots with different external ramps are shown in Fig. 12. For this case, the minimum value of Q_{e2} is about 7.6, no matter how much external ramp is used, the peaking is no less than 20 dB. This is also the conclusion from [34], where it shows that for constant frequency V^2 peak control with ceramic capacitors, the dynamic performance is very bad with only external ramp compensation. Therefore, an additional current ramp is needed to improve the dynamic performance.

IV. Small-Signal Analysis and Design With Hybrid Ramp

As analyzed in Section III, to provide better damping for the ceramic cap case, it is necessary to enhance the current strength feedback by adding current information. Therefore, a hybrid ramp strategy is proposed for the optimum design purpose: a current ramp is used to enhance the current strength feedback to minimize the effect of the capacitor voltage feedback loop, while an external ramp is used to reduce the effect of sample and hold effect for the inductor current feedback loop. The hybrid ramp strategy is first proposed in [32] in digital constant on-time VRM application. The hybrid ramp includes the external ramp and the estimated inductor current ramp, which is provided by a digital inductor current estimator, by only sampling the input voltage, output voltage, and average inductor current with low oversampling rate ADCs. For analog constant frequency V^2 control, either inductor current or capacitor current can be used to enhance current feedback strength, as shown in Fig. 13(a) and (b). To sense inductor current, the traditional sensing methods by sensing resistor or DCR current sensing method can be used. To sense capacitor current, a simple lossless capacitor current sensing method has been proposed in [27]. Alternatively, a non-invasive capacitor current sensing method, which considers the ESL effect has been proposed in [35].

Additional current feedback changes the current feedback strength from α to α', which is defined as follows:

$$\alpha' = \frac{(R_{Co} + R_i)C_o}{T_{\rm sw}}. \tag{14}$$

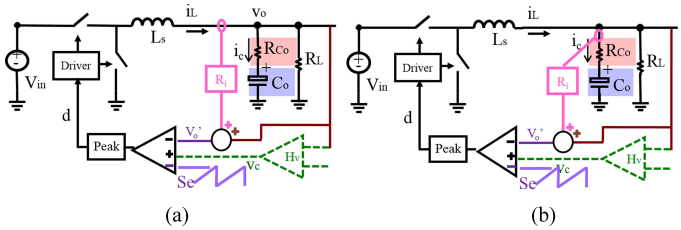


Fig. 13. Constant frequency V^2 peak control with hybrid ramp compensation: (a) with inductor current ramp (b) with capacitor current ramp.

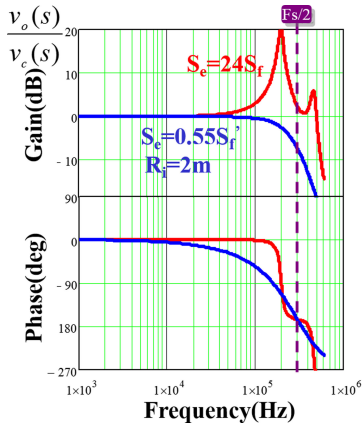


Fig. 14. Comparisons of Bode plots of control-to-output voltage transfer function for the ceramic capacitor with $F_{\rm sw} = 600$ kHz and $D = 0.1$: external ramp (red) and hybrid ramp (blue).

Compared with (2), it can be seen that R_i enhances current feedback strength as a virtual ESR. The small-signal model for constant frequency V^2 peak control with a hybrid ramp is very similar as (8); the only difference is that α is replaced with α' and s_f is replaced with s'_f which is defined in (15). Both of the parameters are modified by R_i. Therefore, the conclusions associated with (8) are all applicable to the hybrid ramp case

$$s'_f = (R_{Co} + R_i)\frac{V_o}{L_s}. \tag{15}$$

The suggested design guidelines are as follows:

Step 1: Design R_i to enhance current information so that the following equation is met:

$$\alpha' = \frac{(R_{Co} + R_i)C_o}{T_{\rm sw}} = 1. \tag{16}$$

Step 2: Design S_e to control Q_{e2}: for example, $Q_{e2} = 2/\pi$, then S_e should be as follows:

$$\frac{s_e}{s'_f} \approx 1 - \frac{1-D}{2\alpha'} = \frac{1+D}{2}. \tag{17}$$

For example, for ceramic capacitors with $f_{\rm sw} = 600$ kHz and $D = 0.1$, according to the aforementioned design guideline, design $R_i = 2$ mΩ and $S_e = 0.55S'_f$. As shown in Fig. 14, a flat gain up to a very high frequency can be achieved. Compared with the large peaking using only external ramp compensation, a well-damped system can be achieved with a hybrid ramp.

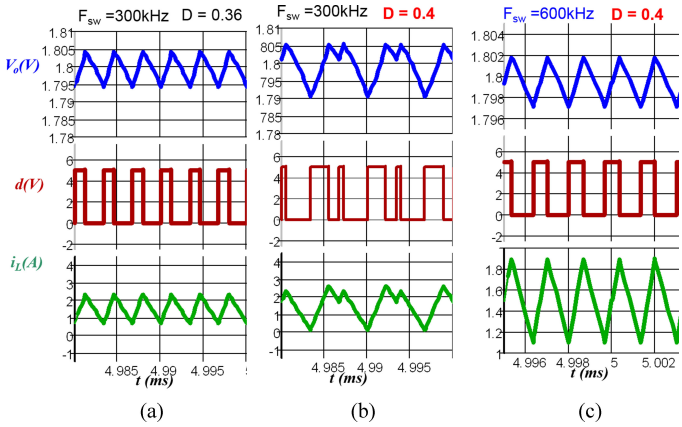


Fig. 15. Operating waveform with different circuit parameters (a) $F_{\rm sw} = 300$ kHz, $V_{\rm in} = 5$ V, $D = 0.36$, stable (b) $F_{\rm sw} = 300$ kHz, $V_{\rm in} = 4.5$ V, $D = 0.4$, unstable (c) $F_{\rm sw} = 600$ kHz, $V_{\rm in} = 4.5$ V, $D = 0.4$, stable.

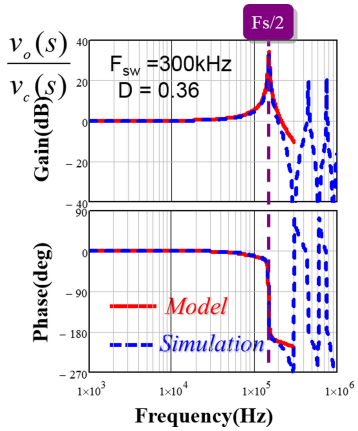


Fig. 16. Small-signal control-to-output voltage verification with $F_{\rm sw} = 300$ kHz, $V_{\rm in} = 5$ V, $D = 0.36$.

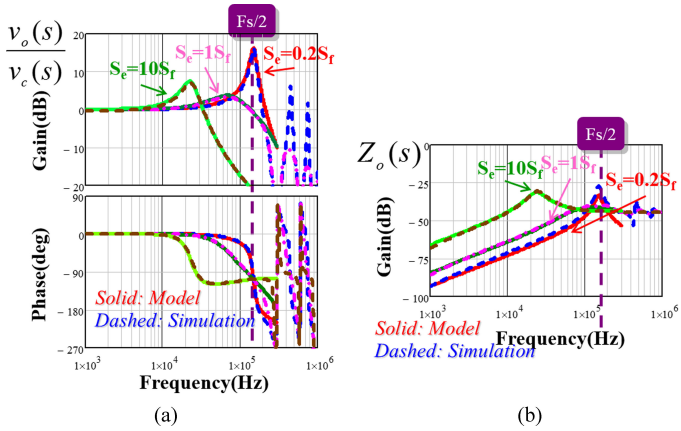


Fig. 17. Small-signal model verification for constant frequency V^2 peak control with different external ramps and with parameters: OSCON capacitor, $F_{\rm sw} = 300$ kHz, $D = 0.4$. (a) Control-to-output voltage transfer function. (b) Output impedance.

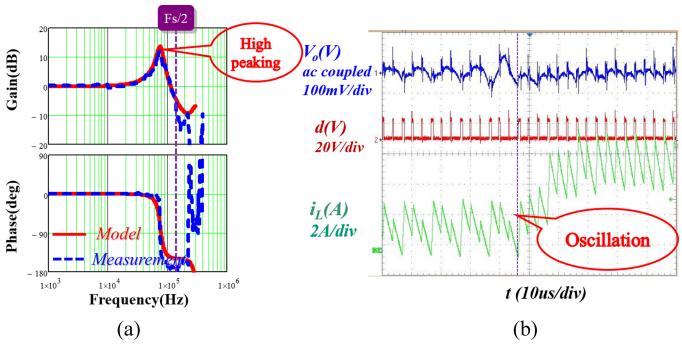


Fig. 18. Experimental results for ceramic caps with only external ramp compensation. (a) Control-to-output voltage transfer function. (b) Load transient step-up (1.5–5 A) performance.

V. Simulation and Experimental Results

The SIMPLIS simulation tool is used to verify the small-signal analysis for constant frequency V^2 control. Circuit parameters are shown as follows: OSCON capacitor, $C_o = 560\ \mu$F, $R_C = 6\ m\Omega$, $V_o = 1.8$ V, $L_s = 2.3\ \mu$H, and $I_o = 1.5$ A. From stability criterion (6), for $F_{\rm sw} = 300$ kHz, α is around 1, the instability point occurs when D is 0.37. As shown in Fig. 15(a), when $V_{\rm in} = 5$ V corresponding to $D = 0.36$, the circuit is stable, while in Fig. 15(b), when $V_{\rm in} = 4.5$ V corresponding to $D = 0.4$, the circuit is unstable as subharmonic oscillation is shown. This agrees with the prediction from (6). Fig. 15(c) shows the effect of current feedback strength α on stability, in this case, $F_{\rm sw} = 600$ kHz, α is around 2, from (6) or Fig. 6, with increasing α, the instability point is $D = 0.43$, which means the circuit should be stable at 0.4 duty cycle, which is verified in Fig. 15(c).

Fig. 16 shows the comparison between analytical model shown in (4) and simulation results. It can be seen that the model is accurate at half of switching frequency and useful up to switching frequency. For this case, although from Fig. 15(a), the circuit is stable, however, it is very close to the instability point as the double pole at half of switching frequency has a very large quality factor, which can be seen from Fig. 16, where the peaking on gain plot is very high and the phase drops very fast at half of switching frequency.

Fig. 17 shows the small-signal verification for constant frequency V^2 peak control with different external ramps and the following circuit parameters: OSCON capacitor, $C_o = 560\ \mu$F, $R_C = 6\ m\Omega$, $F_{\rm sw} = 300$ kHz, $V_{\rm in} = 4.5$ V, and $D = 0.4$. The model agrees with simulation results very well.

To verify the ineffectiveness of the external ramp compensation for ceramic capacitor applications, where current feedback strength α is very small. Experiments on the control-to-output voltage transfer function and load transient measurements are conducted based on the demo-board NCP5422A from ON semiconductor. The circuit parameters are shown as follows: $F_{\rm sw} = 305$ kHz, D = 0.15, $V_{\rm in} = 12$ V, $V_o = 1.8$ V, Ceramic capacitor: $C_o = 300\ \mu$F, $R_C = 2\ m\Omega$, and $L_s = 1.3\ \mu$H and the measurement is based on the network analyzer Agilent 4395A. Fig. 18(a) shows the small-signal measurements using only an external ramp $S_e = 21$ mV/μs. The results show that the model [shown in (8)] agrees very well with the experiment. Since α is only around 0.2 in this case, although a relatively large external ramp is used, there is still high peaking from the gain plot. Fig. 18(b) shows step-up load transient (1.5–5 A) experimental

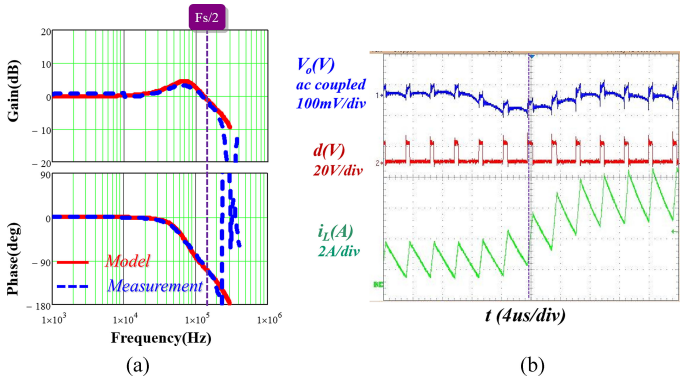


Fig. 19. Experimental results for ceramic caps with hybrid ramp compensation. (a) Control-to-output voltage transfer function. (b) Load transient step-up (1.5–5 A) performance.

result, the dynamic performance is very poor and there is oscillation during transient due to large quality factor.

Fig. 19 shows the small-signal measurement and load transient result with additional current feedback strength. In this case, $R_i = 7$ m and α is around 0.8. As shown in Fig. 19(a), the small-signal model [shown in (15)] agrees with the measurement result and the peaking decreases significantly when compared with Fig. 18(a). Therefore, the dynamic load transient performance shown in Fig. 19(b) improves substantially. This verifies that for ceramic caps, current ramp is required in order to achieve a well-damped performance.

VI. Summary and Conclusion

In this paper, the characteristics of constant frequency V^2 control are analyzed and design guidelines for different applications are provided. By separating the feedback information, it is found that there are two pairs of double poles located at half of the switching frequency; one pair is caused by the sample-and-hold effect in the inner current loop, while the other pair is due to the capacitor voltage feedback loop. Stability is not only related to the duty cycle, but also to current feedback strength. For constant frequency V^2 peak control, a subharmonic oscillation occurs either in a large duty-cycle application or in application with small current feedback strength (e.g., with ceramic capacitors). With large current feedback strength (e.g., with OSCON capacitors), the external ramp is effective to solve the instability problems and achieves a good dynamic performance as long as it is designed appropriately [e.g., shown in (11)]. However, using only an external ramp is not an effective solution when current feedback strength is small (e.g., with ceramic capacitors). In this case, the hybrid ramp, which includes both external ramp and current ramp, is proposed to improve the dynamic performance.

References

[1] D. Gorder and W. R. Pelletier, "V^2 architecture provides ultra fast transient response in switch mode power supplies," in *Proc. High Freq. Power Convers. Conf.*, 1996, pp. 19–23.

[2] D. Gorder, "Switching regulators," U.S. Patent, 5,770,940, 1998.

[3] R. Redl and J. Sun, "Ripple-based control of switching regulators —An overview," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2669–2680, Dec. 2009.

[4] J. Sun, "Characterization and performance comparison of ripple based control for voltage regulator modules," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 346–353, Mar. 2006.

[5] (2009, Jul.). Texas Instruments, TPS51116 datasheet. [Online]. Available: http://focus.ti.com/lit/ds/symlink/ tps51116.pdf

[6] (2012, Jun.). Monolithic power systems, MP38900 datasheet. [Online]. Available: http://www.monolithicpower.com/

[7] (2007, Oct.). STMicroelectronics, PM6685 data sheet. [Online]. Available: http://www.st.com/

[8] (2013, Jan.). Texas Instruments, TPS51220 datasheet. [Online]. Available: http://www.ti.com/lit/ds/symlink/tps51220a.pdf

[9] (2007, Oct.). On-Semi Conductors, NCP5422A datasheet. [Online]. Available: http://www.onsemi.com/

[10] J. Li and F. C. Lee, "Modeling of V^2 current-mode control," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 9, pp. 2552–2563, Sep. 2009.

[11] S. Tian, K. Cheng, F. Lee, and P. Mattavelli, "Small-signal model analysis and design of constant on-time V^2 control for low-ESR caps with external ramp compensation," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2011, pp. 2944–2951.

[12] S. Tian, F. Lee, P. Mattavelli, K. Cheng, and Y. Yan, "Small-signal analysis and optimal design of external ramp for constant on-time V^2 control with multilayer ceramic caps," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4450–4460, Aug. 2014.

[13] S. Tian, F. Lee, P. Mattavelli, and Y. Yan, "Small-signal analysis and design of constant frequency V^2 peak control," in *Proc. IEEE Appl. Power Electron. Conf.*, 2013, pp. 1717–1724.

[14] S. Qu, "Modeling and design considerations of V^2 controlled buck regulator," in *Proc. IEEE Appl. Power Electron. Conf.*, 2001, pp. 507–513.

[15] W. Huang and J. Clarkin, "Analysis and design of multiphase synchronous buck converter with enhanced V^2 control," in *Proc. High Freq. Power Convers. Conf.*, 2000, pp. 74–81.

[16] W. Huang, "A new control for multi-phase buck converter with fast transient," in *Proc. IEEE Appl. Power Electron. Conf.*, 2001, pp. 273–279.

[17] K. Lee, K. Yao, X. Zhang, Y. Qiu, and F. C. Lee, "A novel control method for multiphase voltage regulators," in *Proc. IEEE Appl. Power Electron. Conf.*, 2003, pp. 738–743.

[18] Y. Mai and P. Mok, "A constant frequency output-ripple-voltage-based buck converter without using large ESR capacitor," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 55, no. 8, pp. 748–752, Aug. 2008.

[19] Y. Lee, S. Wang, and K. Chen, "Quadratic differential and integration technique in V^2 control buck converter with small ESR capacitor," *IEEE Tran. Power Electron.*, vol. 25, no. 4, pp. 829–838, Apr. 2010.

[20] G. Zhou, J. Xu, J. Sha, and Y. Jin, "Valley V^2 control technique for switching converters with fast transient response," in *Proc. IEEE Energy Convers. Congr. Expo. Asia*, 2011, pp. 2788–2791.

[21] G. Zhou, J. Xu, and J. Wang, "Constant-frequency peak-ripple-based control of buck converter in CCM: Review, unification, and duality," *IEEE Tran. Ind. Electron.*, vol. 61, no. 3, pp. 1280–1291, Mar. 2014.

[22] J. Cortes, V. Svikovic, P. Alou, J. Oliver, and J. Cobos, "Design and analysis of ripple-based controllers for buck converters based on discrete modeling and Floquet theory," in *Proc. IEEE COMPEL*, 2013, pp. 1–9.

[23] R. B. Ridley, "A new, continuous-time model for current-mode control," *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp. 271–280, Apr. 1991.

[24] A. R. Brown and R. D. Middlebrook, "Sample-data modeling of switched regulators," in *Proc. IEEE Power Electron. Spec. Conf.*, 1981, pp. 349–369.

[25] J. Li and F. C. Lee, "New modeling approach and equivalent circuit representation for current-mode control," *IEEE Trans. Power Electron.*, vol. 25, no. 5, pp. 1218–1230, May 2010.

[26] Y. Yan, F. C. Lee, and P. Mattavelli, "Unified three-terminal switch model for current mode controls," *IEEE Trans. Power Electron.*, vol. 27, no. 9, pp. 4060–4070, Sep. 2012.

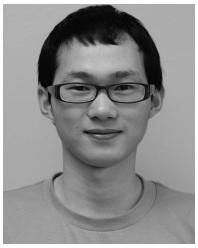
[27] Y. Yan, P. Liu, F. C. Lee, Q. Li, and S. Tian, "V^2 control with capacitor current ramp compensation using lossless capacitor current sensing," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2013, pp. 117–124.

[28] F. Yu and F. C. Lee, "Design-oriented model for constant on-time V^2 control," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2010, pp. 3115–3122.

[29] Y. Yan, F. C. Lee, P. Mattavelli, and S. Tian, "small signal analysis of V^2 control using current mode equivalent circuit model," in *Proc. IEEE Appl. Power Electron. Conf.*, 2013, pp. 1709–1716.

[30] S. Tian, F. C. Lee, Q. Li, and Y. Yan, "Unified equivalent circuit model of V^2 control," in *Proc. IEEE Appl. Power Electron. Conf.*, 2014, pp. 1016–1023.

[31] S. He, S. Wu, Y. Xu, T. Yan, Y. Chen, and L. Chen, "Nonlinear modeling and analysis of valley V^2 controlled buck converter," in *Proc. IEEE Int. Symp. Microw. Propag. Antennas EMC Technol. Wireless Commun.*, 2013, pp. 659–663.
[32] K.-Y. Cheng, F. Yu, S. Tian, F. C. Lee, and P. Mattavelli, "Digital hybrid ripple-based constant on-time control for voltage regulator modules," in *Proc. IEEE Appl. Power Electron. Conf.*, 2011, pp. 346–353.
[33] K.-Y. Cheng, S. Tian, F. Yu, F. C. Lee, and P. Mattavelli, "Digital hybrid ripple-based constant on-time control for voltage regulator modules," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 3132–3144, Jun. 2014.
[34] J. Cortes, V. Svikovic, P. Alou, J. Oliver, and J. Cobos, "Impact of the control on the size of the output capacitor in the integration of Buck converters," in *Proc. Int. Conf. Integr. Power Syst.*, 2014, pp. 1–6.
[35] S. Huerta, P. Alou, J. Oliver, O. Garcia, J. Cobos, and A. Abou-Slfotouh, "Design methodology of a non-invasive sensor to measure the current of the output capacitor for a very fast non-linear control," in *Proc. IEEE Appl. Power Electron. Conf.*, 2009, pp. 806–811.



Shuilin Tian (S'11) received the B.S. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2008, and the M.S. degree in power electronics from the Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA, in April 2012, where he is currently working toward the Ph.D. degree.

From May 2012 to Aug 2012, he was an application Engineer Intern in Linear Technology, Milpitas, CA, USA. He has published more than ten peer-reviewed papers in journals and conferences. His research interests include modeling, analysis, control of PWM converters (including point of load converters and voltage regulator) and resonant converters.

Fred C. Lee (S'72–M'74–SM'87–F'90) received the B.S. degree in electrical engineering from the National Cheng Kung University, Tainan, Taiwan, in 1968, and the M.S. and Ph.D. degrees in electrical engineering from Duke University, Durham, NC, USA, in 1972 and 1974, respectively.

He is currently a University Distinguished Professor at Virginia Polytechnic Institute and State University (Virginia Tech), Blacksburg, VA, USA, and the Founder and Director of the Center for Power Electronics Systems. He holds 72 U.S. patents, and has published 252 journal articles and 639 refereed technical papers.

Dr. Lee has served as the President of the IEEE Power Electronics Society (1993—1994) and is a received the William E. Newell Power Electronics Award in 1989, the Arthur E. Fury Award for Leadership and Innovation in 1998, the Honorary Sun Yuen Chuan Chair Professor at National Tsinghua University, Taiwan, in 2001, the Outstanding Alumni Award from National Cheng Kung University in 2004, the Ernst–Blickle Award for achievement in the field of power electronics in 2005, and the Honorary Kwoh-Ting Li Chair Professor Award at National Cheng Kung University, Taiwan, in 2011. He is a member of the National Academy of Engineering, USA and an academician of Academia in Taiwan.

Paolo Mattavelli (S'95–A'96–M'00–SM'10) received the master's (Hons.) and Ph.D. degrees in electrical engineering from the University of Padua, Padua, Italy, in 1992 and 1995, respectively.

From 1995 to 2001, he was a Researcher at the University of Padua. From 2001 to 2005, he was an Associate Professor with the University of Udine, Udine, Italy, where he led the Power Electronics Laboratory. In 2005, he joined the University of Padova, Vicenza, Italy, with the same duties. From 2010 to 2012, he was a Professor and Member of the Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA. He is currently at the University of Padova, with an adjunct position at Virginia Tech. His research interests include analysis, modeling and analog and digital control of power converters, grid-connected converters for renewable energy systems and microgrids, and high-temperature and high-power density power electronics. In these research fields, he has been leading several industrial and government projects.

Dr. Mattavelli served as an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2003 to 2012. From 2005 to 2010, he was the Industrial Power Converter Committee Technical Review Chair for the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS. For terms 2003–2006 and 2006–2009, he was also a Member-at-Large of the IEEE Power Electronics Society's Administrative Committee. He received the Prize Paper Award in the IEEE TRANSACTIONS ON POWER ELECTRONICS, in 2005, 2006, and 2011 and the second Prize Paper Award at the IEEE Industry Application Annual Meeting, in 2007.

Yingyi Yan (S'10–M'13) received the Bachelor degree in electronic and information engineering from Zhejiang University, Hangzhou, China, in 2007, and the M.S. and Ph.D. degrees in 2010 and 2013, respectively, both in electrical engineering from Virginia Tech, Blacksburg, Virginia. USA.

He is currently an application engineer in Linear Technology for the Digital Power System Management products and high current power modules. He has published more than 15 peer-reviewed papers in journals and conferences. His research interests include modeling and control of converters, digital control techniques for power converters and low-voltage high-current conversion techniques.