Resonance Analysis and Soft-Switching Design of Isolated Boost Converter With Coupled Inductors for Vehicle Inverter Application

Yuxi Wang, *Student Member, IEEE*, Wei Liu, *Student Member, IEEE*, Hao Ma, *Member, IEEE*, and Longyu Chen

***Abstract*—The comprehensive resonance analysis and soft-switching design of the isolated boost converter with coupled inductors are investigated in this paper. Due to the resonance participated by the voltage doubler capacitor, clamping capacitor, and leakage inductance of coupled inductors, the reverse-recovery problem of the secondary diodes is restrained within the whole operation range. By choosing appropriate magnetic inductance of the coupled inductors, zero-voltage switching ON of the main MOSFETs is obtained collectively at the same working conditions without any additional devices. Moreover, the range of duty ratio is enlarged to achieve soft switching and an optimal operation point is obtained with minimal input current ripple, when duty ratio approaches 0.5. Additionally, two kinds of resonances are analyzed and an optimized resonance is utilized to achieve better power density. The prototype is implemented for the vehicle inverter requiring a 150 W output power, input voltage range varying from 10.8 to 16 V, and 360 V output voltage. Experiment results verify the design and show that the minimum efficiency is about 93.55% and 90.53% at low load and full load, respectively.**

***Index Terms*—Interleaved boost converter, resonance analysis, soft switching, vehicle inverter application.**

I. Introduction

VEHICLE inverter is now spreading across the world. Top-end Audi and Bavarian Motor Works cars are enjoying comfort and convenience of vehicle inverters. Most traditional vehicle inverters are composed by two stages: dc/dc converter and dc/ac inverter. To achieve 220 V root-mean-square sine wave, the input voltage of dc/ac inverter should be at least 360 $V_{\rm dc}$ in a highly efficient manner [1]. It is worth noticing that the vehicle battery presents low-voltage characteristic (10.8 to 16 V, typical 12 V), the dc/ac inverter must have a high-voltage conversion ratio dc/dc converter on the front end. Considering life span of vehicle battery, mounting space and natural cooling, dc/dc converter with low-input current ripple, high operation frequency, and high efficiency are required in this application [2]–[9]. Besides, galvanic isolation is necessary to meet the safety standards.

Push–pull topology is widely used in dc/dc stage [8]–[13]. Voltage-fed push–pull converter proposed in [9] features high input current ripple because the current in the primary side is discontinuous. A low-pass *LC* input filter is applied to minimize the ripple. Then it increases the volume of the system for high input current. Moreover, the converter's voltage conversion ratio is only determined by turn ratio of transformer. To achieve a high step up feature, a large turn ratio brings large transformer volume and leakage inductance which degrades power density and circuit performance.

Current-fed push–pull is suitable for low input voltage, high input current application due to the input inductor. Furthermore, significant topologies are used in fuel cell system and battery sourcing application [10], [11] and active clamping with resonance technology has gained attraction which can realize zero-voltage switching (ZVS) on of MOSFETs [14]–[16] or resolve reverse-recovery problem of secondary rectifying diodes [12], [17]. With soft-switching characters, the operation frequency can be high enough to obtain not only high power density but also high efficiency. An active-clamping current-fed push–pull converter in [8] has satisfied performance for vehicle inverter application. Comparison of two mentioned converters is listed in Table I. However, more detailed resonance analysis still needs to be presented. Optimized resonance will be designed to minimize capacitors volume, and improve power density.

From the previous research studies [11]–[17], converters with resonance can be divided into two classes in terms of soft-switching characteristic. One is to obtain ZVS on of the main MOSFETs [11], [14]–[16] while the other is to turn OFF secondary diodes softly [12], [13], [17]. A novel isolated zero-voltage transition (ZVT) boost converter with coupled inductors has been proposed which belongs to the first class [14]. The input-parallel configuration is adopted to share the large input current and to reduce the conduction losses. Besides, the active clamp circuits are employed to achieve ZVT for all the active switches. However, reverse-recovery problem of secondary diodes is still remained and duty ratio must be larger than 0.5 to achieve ZVS on of the main MOSFETs. Furthermore, these two kinds of soft-switching characteristics are still not obtained collectively at the same working conditions among the mentioned converters yet.

In this paper, resonance analysis and soft-switching design of the isolated boost converter with coupled inductors are

Manuscript received November 19, 2013; revised February 24, 2014; accepted April 8, 2014. Date of publication April 16, 2014; date of current version October 15, 2014. This paper was supported in part by the National High Technology Research and Development Program of China (SS2012AA053602). Recommended for Publication by Associate Editor M. Ferdowsi.

Y. Wang, W. Liu, and H. Ma are with the Institute of Power Electronics, College of Electrical Engineering, Zhejiang University, Hangzhou 310027, China (e-mail: neutronxi@zju.edu.cn; liuwei0860@zju.edu.cn; mahao@zju.edu.cn).

L. Chen is with the GE (China) Research and Development Center Co., Ltd., Shanghai 201203, China (e-mail: cly319@gmail.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2014.2317838

TABLE I
COMPARISON OF TWO MENTIONED CONVERTERS

Converter	Input current ripple	Soft switching of MOSFETs	Soft switching of Diodes	Efficiency (12V input voltage)	Core of Transformer
Voltage-fed push-pull in [9]	Large	Part ZVS on	ZCS off	95.4% @150W 94.3% @60W	PQ32/30 PC44
Current-fed push-pull in [8]	Small	ZVS on when D>0.5	ZCS off	92.4% @150W 91.1% @60W	PQ26/25 PC40

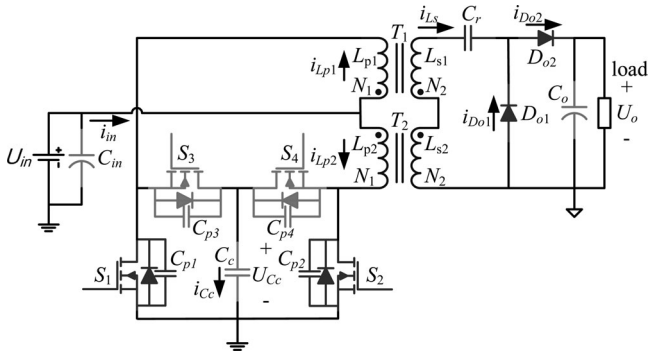


Fig. 1. Schematic of the converter.

presented. The schematic of converter is implemented as Fig. 1. Compared with the former proposed converter, both ZVS on of the main MOSFETs and zero-current switching (ZCS) off of the secondary diodes are obtained collectively at the same working conditions without any additional devices. Moreover, the range of duty ratio is enlarged due to the design and an optimal operation point is obtained when duty ratio approaches 0.5 and the ripple of input current moves in close to zero. The volume of the converter can also be decreased because of smaller transformers and smaller capacitors. A dc/dc converter for vehicle inverter is implemented to verify the design.

This paper is organized as following. Principle of operations is shown in Section II. The analysis and design of resonance and circuit are illustrated in Sections III and IV, respectively. Finally, experimental results in Section IV validate the analysis and design. The summarization is given in the final section.

II. PRINCIPLE OF OPERATIONS

Due to interleaved control of S_1 and S_2, the frequency of i_L is twice as high as the switching frequency so input current ripple is reduced. When D is 0.5, input current ripple is approximately zero. Principle of operation is presented as follows.

A. Operational Principle for $D < 0.5$

When D is small than 0.5, resonance operates at nonoverlapping interval.

Mode 1 $[t_0, t_1]$*:* S_1 is turned OFF at t_0 while S_2 is off. Inductor L_{p1} and L_{p2} are discharging and *di/dt* equals $(U_{\rm in}–U_{Cc})/L_p$. Due to small inductance of L_{p1} and L_{p2}, i_{Lp2} is under zero at t_1. The reverse current is flowing from clamping capacitor C_c, auxiliary MOSFET S_4 to inductor L_{p2}. No energy is transferred to secondary side. Equivalent circuit is presented as Fig. 2(a).

Mode 2 $[t_1, t_2]$*:* S_4 is turned OFF at t_1 when i_{Lp2} is reverse. Inductor L_{p2} discharges parasitic capacitor C_{p2} of S_2 for freewheeling. If the reverse current of L_{p2} is large enough, there will be sufficient energy to discharge $u_{\rm DS2}$ to zero at t_2. Equivalent circuit is presented as Fig. 2(b).

Mode 3 $[t_2, t_3]$*:* S_2 is turned ON at t_2 when $u_{\rm DS2}$ reaches zero. ZVS on of S_2 is achieved. S_1 is still off. Hence, inductor L_{p1} is discharging and *di/dt* equals $(U_{\rm in}–U_{Cc})/L_p$. Inductor L_{p2} is charging and *di/dt* equals $U_{\rm in}/L_p$. Secondary circuit begins to conduct. Transformer T_1 works as a flyback converter and transformer T_2 works as a forward converter. Leakage inductor of transformer, clamping capacitor C_c and voltage doubler capacitor C_r start to resonate. Therefore, both i_{Lp1} and i_{Lp2} contain magnetizing current and resonant current. Equivalent circuit is presented as Fig. 2(c).

Mode 4 $[t_3, t_4]$*:* Secondary current i_{Ls} decreases to zero at t_3 and resonant circuit is cut off by diode D_{o2}. Therefore, secondary diode is turned OFF softly and reverse-recovery problem is removed. Inductor L_{p1} is still discharging with rate determined by $(U_{\rm in}–U_{Cc})/L_p$. Inductor L_{p2} is still charging with rate determined by $U_{\rm in}/L_p$. Equivalent circuit is presented as Fig. 2(d).

During the remaining half period of T_S, Modes 5 to 8 are analogous to the operation of Modes 1 to 4. Voltage–second balance law of inductor L_{p1} and L_{p2} is written as

$$U_{\rm in}D + (U_{\rm in} - U_{C_c})(1 - D) = 0. \tag{1}$$

Thus

$$U_{C_c} = \frac{U_{\rm in}}{1 - D}. \tag{2}$$

Since secondary topology is secondary windings in series and a voltage doubler rectifying circuit, output voltage is

$$U_o = 2 \times \left[\frac{N_2}{N_1}U_{\rm in} + \frac{N_2}{N_1}(U_{C_c} - U_{\rm in})\right] = \frac{2N_2U_{\rm in}}{N_1(1 - D)}. \tag{3}$$

From (3), though magnetizing currents of inductor L_{p1} and L_{p2} are reverse at some intervals, the voltage gain does not change. Fig. 3 shows key waveforms for $D < 0.5$.

B. Operational Principle for $D > 0.5$

When D is > 0.5, resonance operates at overlapping interval. Analogous analysis is omitted due to space restriction. Fig. 4 shows key waveforms for $D > 0.5$.

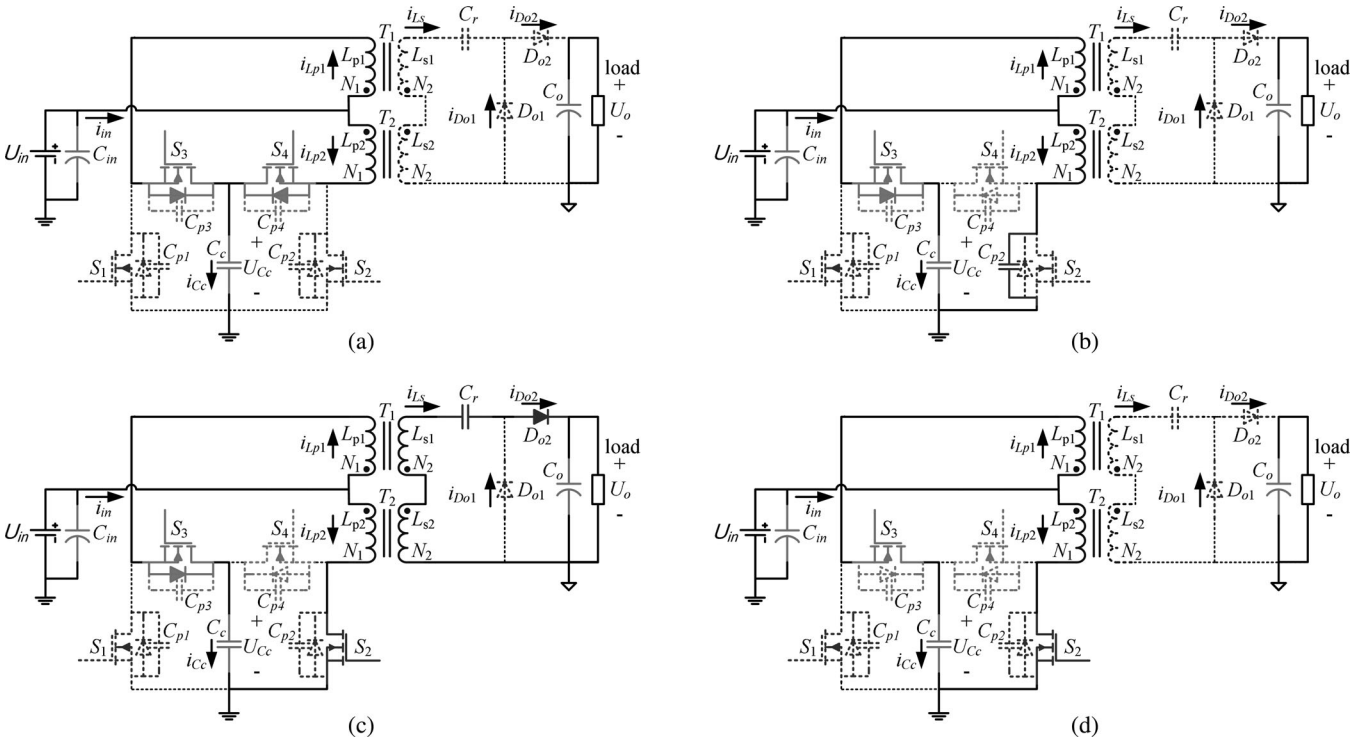


Fig. 2. Operation modes of the proposed converter. (a) Mode 1 $(t_0$–$t_1)$. (b) Mode 2 $(t_1$–$t_2)$. (c) Mode 3 $(t_2$–$t_3)$. (d) Mode 4 $(t_3$–$t_4)$.

III. Analysis and Design of Resonance

There are significant high step-up topologies such as current-fed push–pull [12], flyback-forward [14], [18], and dual-boost [15]. Resonance is an important interval of these converters. Appropriate resonant parameter can obtain soft-switching performance. Primary-dominant resonance is used in [1], [11], [14]–[16] and ZVS on of primary main MOSFETs is achieved. Secondary-dominant resonance is used in [12], [13], and [17] and secondary rectifying diodes are turned OFF softly. Resonance model of this converter and relationship between two kinds of resonances will be presented and analyzed.

A. Analysis of Equivalent Resonant Circuit

Current of primary winding is composed by magnetizing component $(i_{Lp}(t))$ and resonant component $(N_2 i_{Ls}(t)/N_1)$. Hence, equivalent circuit of resonant interval is shown as Fig. 5. State equations are listed as:

$$u_s(t) = u_{Cr}(t) + L_{k,s}\frac{\mathrm{d}i_{Ls}(t)}{\mathrm{d}t} \tag{4}$$

$$i_{Ls}(t) = C_r\frac{\mathrm{d}u_{Cr}(t)}{\mathrm{d}t} \tag{5}$$

$$i_{Cc}(t) = i_{Lp2}(t) - \frac{N_2}{N_1}i_{Ls}(t) \tag{6}$$

$$i_{Cc}(t) = C_c\frac{\mathrm{d}u_{Cc}(t)}{\mathrm{d}t} \tag{7}$$

$$u_s(t) = \frac{N_2}{N_1}u_{Cc}(t) \tag{8}$$

$$i_{Ls}(0) = 0 \tag{9}$$

$$u_s(0) = \frac{N_2}{N_1}u_{Cc}(0) = u_{Cr}(0) + L_{k,s}\frac{\mathrm{d}i_{Ls}(t)}{\mathrm{d}t}|_{t=0} \tag{10}$$

$$i_{Lp2}(t) = i_{Lp2}(0) - \frac{V_c - V_{\mathrm{in}}}{L_m}t. \tag{11}$$

So current of secondary winding is

$$i_{Ls}(t) = A\sin(\omega_{\mathrm{eq}}t + \theta) + \frac{nC_r(U_{\mathrm{in}} - U_{C_c})}{L_m(n^2C_r + C_c)}t + \frac{nC_r i_{Lp2}(0)}{n^2C_r + C_c} \tag{12}$$

where

$$n = \frac{N_2}{N_1}, C_{eq} = \frac{n^2C_rC_c}{n^2C_r + C_c}, L_{\mathrm{eq}} = \frac{L_{k,s}}{n^2}, \omega_{\mathrm{eq}} = \frac{1}{\sqrt{L_{\mathrm{eq}}C_{\mathrm{eq}}}}$$

$$B = \frac{nU_{Cc}(0) - U_{Cr}(0)}{\omega_{\mathrm{eq}}L_{k,s}} - \frac{nC_r(U_{\mathrm{in}} - U_{C_c})}{\omega_{\mathrm{eq}}L_m(n^2C_r + C_c)}$$

$$C = \frac{-nC_r i_{Lp2}(0)}{n^2C_r + C_c}$$

$$\theta = \arctan\frac{C}{B} \tag{13}$$

$$A = \sqrt{B^2 + C^2}. \tag{14}$$

B. Primary-Dominant Resonance and Secondary-Dominant Resonance

Equation (13) can be expressed as

$$\theta = \operatorname{arccot}\left\{ - \frac{nu_{Cc}(0) - u_{Cr}(0)}{i_{Lp2}(0)}\sqrt{\frac{C_c(n^2C_r + C_c)}{n^2C_rL_{k,s}}}\right.$$

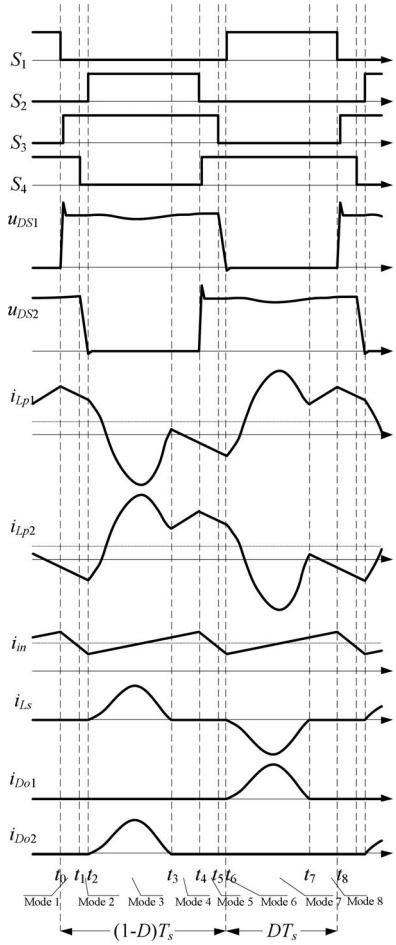


Fig. 3. Key waveforms for $D < 0.5$.

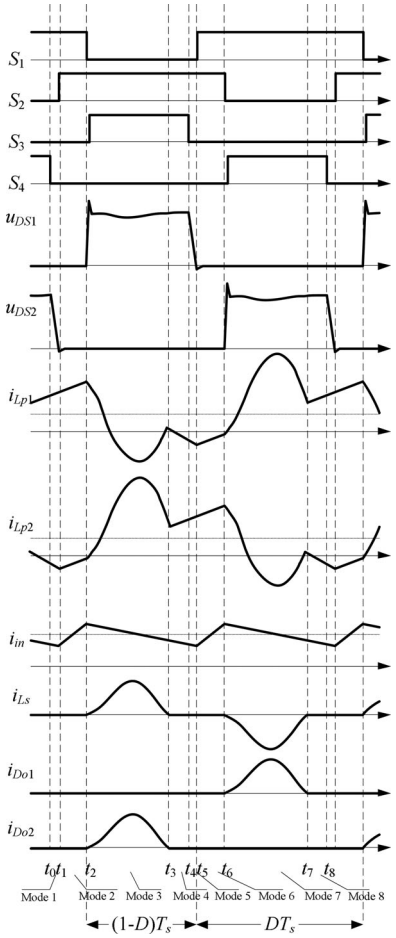


Fig. 4. Key waveforms for $D > 0.5$.

$$+\frac{C_c(u_{\text{in}}-u_C)}{ni_{Lp2}(0)}\sqrt{\frac{n^2C_rL_{k,s}}{C_c(n^2C_r+C_c)}}\Bigg\}$$

$$\approx -\arctan\frac{i_{Lp2}(0)}{nu_{Cc}(0)-u_{Cr}(0)}\sqrt{\frac{n^2C_rL_{k,s}}{C_c(n^2C_r+C_c)}}. \tag{15}$$

Equation (15) shows that resonant parameter and initial status of $C_c, C_r, L_{k,s}$ make contribution to the phase of resonance. Comparing C_r with C_c, θ tends to be $-\pi/2$ when C_r is relatively large enough. The current of secondary winding then is a cosine-like curve. C_r is too large to have any influence on the resonance so it can be named as primary-dominant resonance. Secondary current is just the reflection of primary resonant current. Fig. 6 shows waveforms of simulation for primary-dominant resonance. Current of primary leakage inductor $i_{k,p}$ is reversed and reaches trough after half of resonant cycle$\Delta t = \pi\sqrt{L_{\text{eq},p}C_c}$ ($L_{\text{eq},p}$ is equivalent leakage inductance of primary winding). If auxiliary switch is turned OFF at this moment, primary leakage inductor will discharge capacitor C_{ds} of main MOSFET [14]. ZVS on of main MOSFETs can be achieved when reverse current is sufficiently large. Meanwhile, secondary current is near to its peak at the switching moment. Therefore,

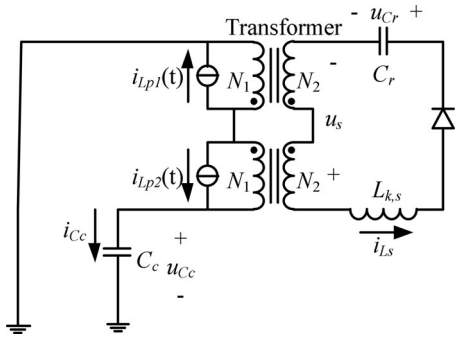


Fig. 5. Equivalent circuit of resonant interval.

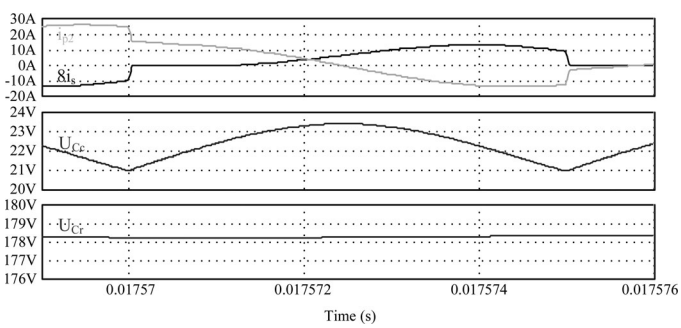


Fig. 6. Primary-dominant resonance ($N_2/N_1 = 8, C_c = 10$ μF, $C_r = 47$ μF, $L_{k,s} = 10.74$ μH $L_{p1} = L_{p2} = 3$ μH).

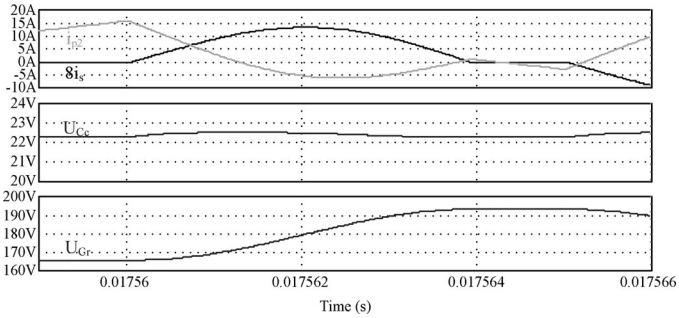


Fig. 7. Secondary-dominant resonance ($N_2/N_1 = 8, C_c = 40\ \mu$F, $C_r = 150$ nF, $L_{k,s} = 10.74\ \mu$H $L_{p1} = L_{p2} = 3\ \mu$H).

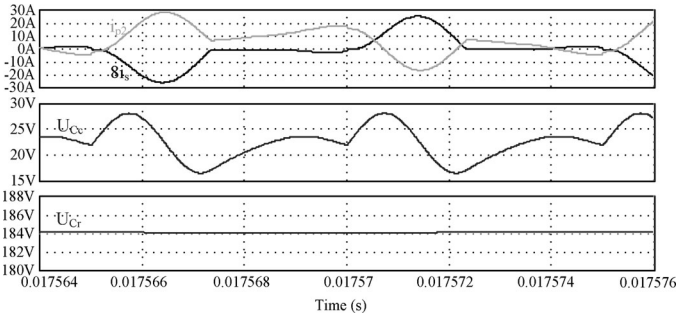


Fig. 8. Primary-dominant resonance cannot achieve ZCS off of secondary diodes ($N_2/N_1 = 8, C_c = 1.25\ \mu$F, $C_r = 100\ \mu$F, $L_{k,s} = 10.74\ \mu$H $L_{p1} = L_{p2} = 3\ \mu$H).

reverse-recovery problem of secondary diodes is remained and only alleviated by secondary leakage inductor.

θ tends to be zero when C_c is relatively large enough. The current of secondary winding then is a sine-like curve. C_c is too large to have any influence on the resonance so it can be named as secondary-dominant resonance. Primary resonant current is just the reflection of secondary resonant current. Fig. 7 shows waveforms of simulation for secondary-dominant resonance. Differently, current of primary leakage inductor $i_{k,p}$ is reversed and reaches trough after a quarter of resonant cycle $\Delta t = \frac{\pi}{2}\sqrt{L_{\mathrm{eq},s}C_r}$ ($L_{\mathrm{eq},s}$ is equivalent leakage inductance of secondary winding). Switching at this moment can achieve ZVS on of main MOSFETs while reverse-recovery problem is still not removed. Current $i_{k,p}$ is above zero again and returns to i_{Lp} after half of resonant cycle $\Delta t = \pi\sqrt{L_{\mathrm{eq},s}C_r}$. Accordingly, secondary current reaches to zero at the moment and resonant circuit is cut off by secondary diodes so diodes are turned OFF softly [12]. If minimal overlapping ($D > 0.5$) or nonoverlapping ($D < 0.5$) interval is longer than half of the resonant cycle, ZCS off will be obtained within the whole operation range.

Hence from previous analysis, ZVS on of main MOSFETs and ZCS off of secondary diodes cannot be obtained simultaneously at the same working conditions.

In primary-dominant resonance, resonant component of current will return to zero after an entire resonant cycle $\Delta t = 2\pi\sqrt{L(_{\mathrm{eq},p}C_c}$. However, auxiliary switch is still conducting so primary resonant circuit is not cut off and another resonant cycle begins. As a result, reverse-recovery problem of secondary diodes is remained. Waveforms for this situation are shown as Fig. 8.

Unfortunately, ZVS on of main MOSFETs cannot be achieved when D is <0.5. Shown as Fig. 9, resonance is terminated when S_2 is turned OFF. Then current flows from primary leakage inductor to clamping capacitor C_c before S_1 is turned ON. Hence, there is no reverse current to discharge capacitor C_{ds} of S_1.

Based on the aforementioned analysis, comparison of two kinds of resonances is presented as Table II.

So it comes to a tradeoff between primary switching loss and secondary reverse-recovery loss in the particular application. ZVS on should be obtained if primary switching loss dominates. ZCS off is preferred when reverse-recovery loss is relatively high. Design of circuit parameter is simple to determine which soft-switching performance will be utilized. In this converter,

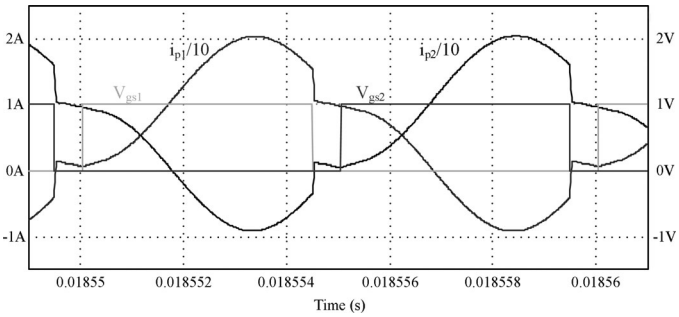


Fig. 9. Resonant waveforms for $D < 0.5$ ($N_2/N_1 = 8, C_c = 6\ \mu$F, $C_r = 47\ \mu$F, $L_{k,s} = 10.74\ \mu$H, $L_{p1} = L_{p2} = 5\ \mu$H).

TABLE II
COMPARISON OF TWO KINDS OF RESONANCES

Resonant timing point	ZVS on of main switches	ZCS off of secondary diodes
Primary -dominant resonance	After $T_r/2 = \pi\sqrt{L_{eq,p}C_c}$ (D>0.5)	Cannot be achieved
Secondary-dominant resonance	After $T_r/4 = \frac{\pi}{2}\sqrt{L_{eq,s}C_r}$ (D>0.5)	After $T_r/2 = \pi\sqrt{L_{eq,s}C_r}$

the design utilizes reverse magnetizing currents of L_{p1} and L_{p2} due to their small inductances which obtain ZVS on of main MOSFETs. Thus, ZVS ON of the main MOSFETs does not have relation with resonant interval so it can be realized without the restricted range of duty ratio in [8], and can coexist with ZCS off of secondary diodes.

C. Design of the Optimized Resonance

In this particular vehicle inverter application, operation point at $D = 0.5$ is preferred because of minimized input current ripple. ZVS on of main switches can be achieved when magnetizing inductances are small enough. Meanwhile, ZCS off of secondary diodes is designed within the whole input voltage and load range. Due to relatively high turn ratio of transformer, C_c needs to be extraordinarily large to obtain secondary-dominant resonance. In the designed converter, a communal clamping capacitor C_c is used and its capacitance is properly not large due to

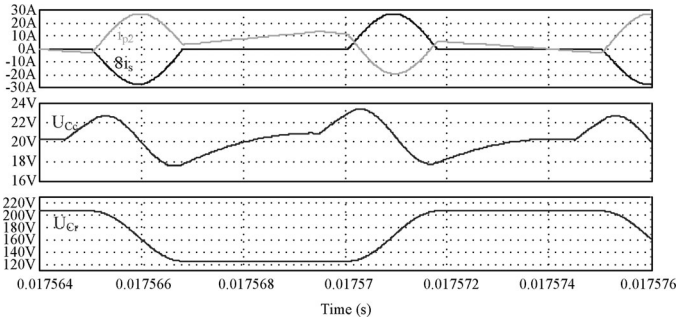


Fig. 10. Waveforms of simulation for designed resonance ($N_2/N_1 = 8, C_c = 3\ \mu$F, $C_r = 47$ nF, $L_{k,s} = 10.74\ \mu$H, $L_{p1} = L_{p2} = 3\ \mu$H).

the design of optimized resonance. Thus, the designed resonance is between the aforementioned two resonances and the volume of capacitor is reduced. Three factors should be considered for design of this optimized resonance.

1) Duration of resonance. In order to achieve ZCS off of secondary diodes, duration of resonance should be shorter than minimal overlapping interval ($D > 0.5$) or nonoverlapping interval ($D < 0.5$). However when duration of resonance is shortened, the peak of resonant current rises to transfer equivalent energy. That means C_c and C_r should be sufficiently large to alleviate current stress of both primary and secondary side.

2) Ripple of clamping voltage. Main MOSFETs will sustain high voltage stress if C_c is too small. Hence, C_c should restrict the ripple of clamping voltage into an acceptable range.

3) Capacitor volume. After taking the previous two into consideration, a combination of C_c and C_r should be adopted to get minimal volume of capacitors.

In this converter, C_r is 47 nF and C_c is 3 μF while turn ratio of transformer is 3:3:24. Waveforms of simulation for resonance are shown as Fig. 10. Obviously, the resonance is the one between primary-dominant resonance and secondary-dominant resonance.

IV. Analysis and Design of Circuit

A. Design of ZCS of Secondary Diodes

Secondary circuit is conducting at nonoverlapping interval ($D < 0.5$) or overlapping interval ($D > 0.5$). When D is smaller than 0.5, the minimal nonoverlapping period is

$$\Delta t_{\min 1} = T_s D_{\min}. \tag{16}$$

When D is greater than 0.5, the minimal overlapping period is

$$\Delta t_{\min 2} = T_s(1 - D_{\max}). \tag{17}$$

If the clamping capacitor C_c is large enough to make little contribution to the resonance, the current of secondary side can be written as

$$i_{Ls}(t) = I_{Ls\_\text{peak}} \sin \omega_{\text{eq}} t \tag{18}$$

where $\omega_{\text{eq}} = \frac{1}{\sqrt{(L_{k,\text{s1}} + L_{k,\text{s2}})C_r}}$.

$L_{k,\text{s1}}$ and $L_{k,\text{s2}}$ are equivalent leakage inductances of secondary side.

Thus, the period of resonance is

$$\Delta t_{\text{res}} = \pi/\omega_{\text{eq}} = \pi\sqrt{(L_{k,\text{s1}} + L_{k,\text{s2}})C_r}. \tag{19}$$

To ensure ZCS off of secondary diodes can be obtained throughout the entire operation range, the period of resonance should be restricted

$$\Delta t_{\text{res}} \le \{\Delta t_{\min 1}, \Delta t_{\min 2}\}_{\min}. \tag{20}$$

Given the leakage inductance of the transformers T_1 and T_2, voltage doubler capacitor C_r can be sketched from (17) to (21):

$$C_r \le \{\frac{D_{\min}^2}{\pi^2(L_{k,\text{s1}} + L_{k,\text{s2}})f_s^2}, \frac{(1 - D_{\max})^2}{\pi^2(L_{k,\text{s1}} + L_{k,\text{S2}})f_s^2}\}_{\min}. \tag{21}$$

B. Design of ZVS of Main MOSFETs

During the resonant interval in [14], reverse currents of L_{p1} and L_{p2} are utilized for ZVS on of the main MOSFETs. However, the design in this converter utilizes reverse magnetizing currents of L_{p1} and L_{p2} due to their small inductances. Thus, ZVS on of the main MOSFETs does not have relation with resonant interval so it can be realized without the restricted range of duty ratio in [14].

To obtain ZVS on of main MOSFETs, the following condition should be achieved:

$$\frac{1}{2}L_p I_{\text{reverse,peak}}^2 \ge \frac{1}{2}C_P U_{\text{clamp}}^2 \tag{22}$$

where L_p is primary inductance of the transformer and C_p is parasitic capacitance of the main MOSFET. $I_{\text{reverse,peak}}$ is peak of the reverse magnetizing current

$$I_{\text{reverse,peak}} = |\frac{1}{2}I_{\text{in}} - \frac{1}{2}\Delta I_{Lp1}|. \tag{23}$$

To obtain sufficient energy for ZVS of main MOSFETs, peak-to-peak ripple ΔI_{Lp1} of magnetizing current should be large

$$\Delta I_{Lp1} = \frac{U_{\text{in}}}{L_p} D T_s. \tag{24}$$

Due to close-loop control of the output voltage and relation between clamping voltage and output voltage, (24) can be written as

$$\Delta I_{Lp1} = \frac{N_1 U_o D(1 - D)}{2N_2 L_p f_s}. \tag{25}$$

Shown as Fig. 11, largest ripple is obtained for ZVS of the main MOSFETs when D is 0.5 and small inductance enlarges the ripple as well.

However, due to (23), $I_{\text{reverse,peak}}$is decreased when dc component of input current rises. Thus, ZVS on of the main MOSFETs is more accessible at light load with the same input voltage or high input voltage with the same load.

C. Analysis of Input Ripple Current

Because of small inductors L_{p1} and L_{p2}, large ripple currents of i_{Lp1} and i_{Lp2} are obtained. However, due to interleaved control of S_1 and S_2, input ripple current is decreased remarkably. Input ripple current can be derived as follows.

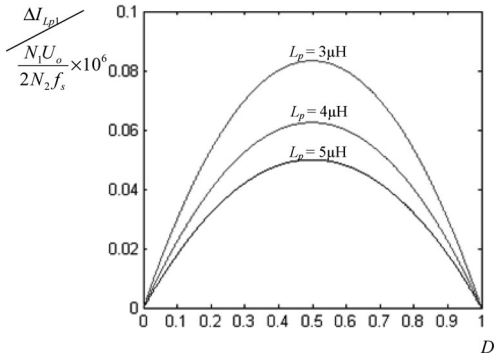


Fig. 11. Peak-to-peak value of magnetizing ripple current with respect to duty ratio.

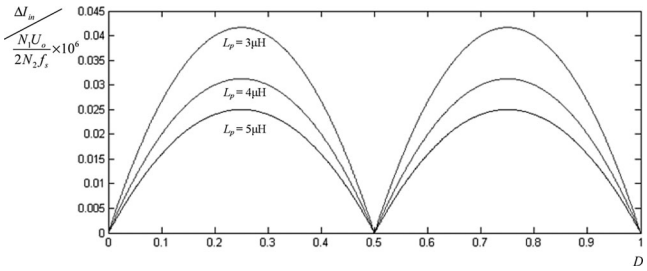


Fig. 12. Peak-to-peak value of input ripple current with respect to duty ratio.

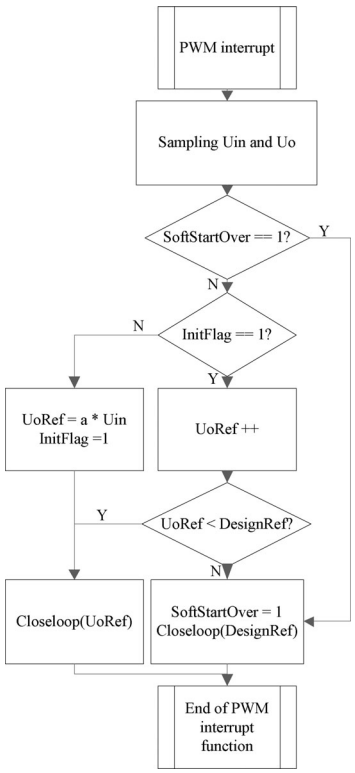


Fig. 13. Flow chart of soft start-up.

When D is smaller than 0.5

$$\Delta I_{\rm in} = 2\frac{U_{Cc}-U_{\rm in}}{L_p}(0.5-D)T_s = \frac{N_1U_o}{2N_2L_pf_s}D(1-2D). \tag{26}$$

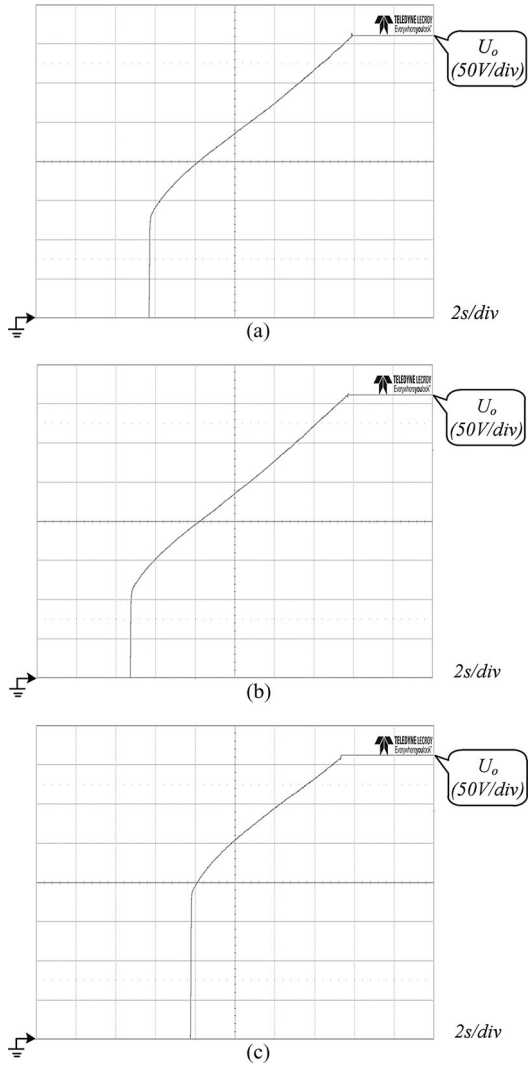


Fig. 14. Waveforms of soft start-up. (a) $U_{\rm in} = 10.8$ V. (b) $U_{\rm in} = 12$ V. (c) $U_{\rm in} = 16$ V.

When D is larger than 0.5

$$\Delta I_{\rm in} = 2\frac{U_{\rm in}}{L_p}(D-0.5)T_s = \frac{N_1U_o}{2N_2L_pf_s}(1-D)(2D-1). \tag{27}$$

Presented as Fig. 12, input ripple current is zero theoretically when D is 0.5.

From Figs. 11 and 12, it is obvious that an optimal operation point is obtained when duty ratio approaches 0.5. Peak-to-peak values of magnetizing ripple currents ΔI_{Lp1} and ΔI_{Lp2} are maximized to achieve ZVS on of the main MOSFETs. Moreover, the ripple of input current is approximately zero at this operation point. Therefore, ZVS on of the main MOSFETs, ZCS off of the secondary diodes and minimal input ripple current are obtained collectively.

However, as shown in Figs. 11 and 12, small inductances of L_{p1} and L_{p2} are advantageous to ZVS on of the main MOSFETs while they enlarge the ripple of input current as well. The designer should take this tradeoff between these two performances into consideration.

TABLE III
PARAMETERS AND COMPONENTS OF THE PROTOTYPE

Parameters	Symbols	Values
Input voltage	U_{in}	10.8~16V
Output voltage	U_o	360V
Output power	P_o	0~150W
Switching frequency	f_s	100kHz
Inductance of primary winding	L_{p1}, L_{p2}	4μH
Inductance of secondary winding	L_{s1}, L_{s2}	256μH
Secondary equivalent leakage inductance	$L_{k,s1}$, $L_{k,s2}$	5.4μH
Primary winding turns	N_1	3
Secondary winding turns	N_2	24
Clamping capacitor	C_c	3.3μF
Resonant capacitor (voltage doubler capacitor)	C_r	47nF
Input capacitor	C_{in}	1000μF
Output capacitor	C_o	220μF
Components	Symbols	Part numbers
Main switches	S_1, S_2	IPP023NE7N3_G
Auxiliary switches	S_3, S_4	IPP015N04NG
Secondary rectifying diodes	D_{o1}, D_{o2}	MUR460
Transformer core	T_1, T_2	PQ26/20
Driver IC		IR2110
DSP		DSPIC33FJ06GS101

D. Scheme of Soft Start-Up

Because input voltage varies from 10.8 to 16 V, open-loop start-up which means increasing duty ratio softly will establish output voltage far away from the prospective 360 V. Overshoot of output voltage will happen when open loop is switched to close loop. Flow chart of soft start-up in this converter is shown as Fig. 13. At the beginning of start-up, input voltage $U_{\rm in}$ is sampled. Then DSP calculates the reference of output voltage $U_{o\rm Ref}$ to ensure initial close-loop duty ratio of MOSFET is 0.05 with input voltage from 10.8 to 16 V. The converter operates in close loop and $U_{o\rm Ref}$ is softly rising to constant (DesignRef) corresponding to 360 V. Waveforms of soft start-up when input voltage is 10.8, 12, and 16 V are shown as Fig. 14. Output voltage is softly rising without overshoot.

V. EXPERIMENTAL RESULTS

To verify the theoretical analysis and design procedures a prototype for vehicle inverter is implemented. The input voltage range of the converter is from 10.8 to 16 V and output voltage is 360 V. The full load is 150 W and switching frequency is 100 kHz.

Clamping voltage is 24 V so duty ratio is nearly 0.5 when input voltage is 12 V normally. According to (2), ideal duty ratio range is from 0.33 to 0.55. Inductances of primary windings are small to utilize reverse magnetizing current for ZVS on of the main MOSFETs.

Detailed parameters and components of the prototype are listed in Table III.

Fig. 15(a)–(c) are the waveforms of the converter at full load. A ripple frequency of the boost inductor is twice as high as the switching frequency. According to Fig. 7(b), though ripple current of i_{Lp1} is large, input ripple current is remarkably tiny which validates the design. To achieve high efficiency on wide input voltage and load conditions, reverse magnetizing current is not large enough at full load because of relatively large magnetic inductance and high dc component of input current. Thus, reverse magnetizing current can reduce turn-on loss of the main MOSFETs but ZVS on is not achieved at full load.

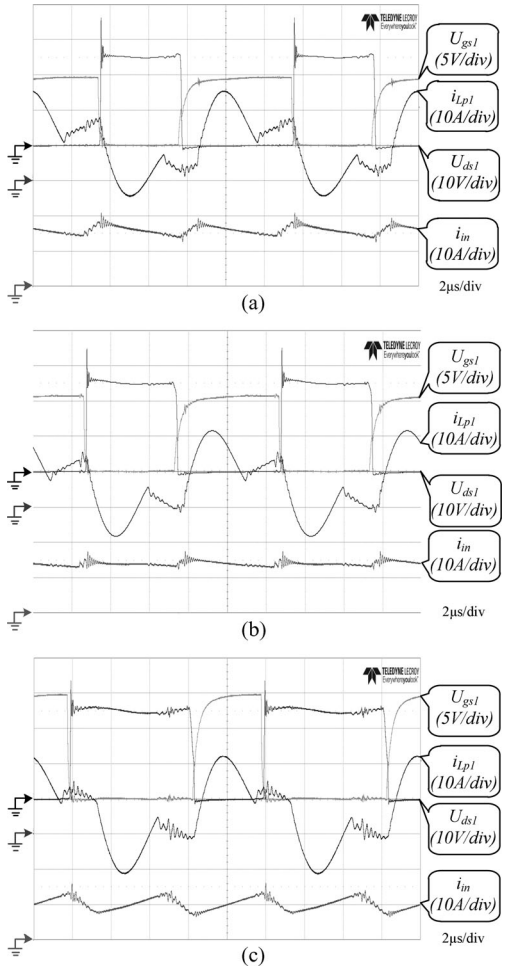


Fig. 15. (a) Waveforms of the converter at full load ($U_{\rm in} = 10.8$ V). (b) Waveforms of the converter at full load ($U_{\rm in} = 12$ V). (c) Waveforms of the converter at full load ($U_{\rm in} = 16$ V).

Nevertheless, ZVS on of the main MOSFETs can be achieved within the most range of operation when dc component of input current is smaller than a proper value. Fig. 16(a)–(c) are the waveforms of the soft switching at proper operation points with different input voltages. Magnetizing current of the primary inductor is reverse when the main MOSFET S_1 is about to turn ON. ZVS on of the main MOSFETs is realized at these operation points. In addition, when $U_{\rm in}$ is 10.8 V, ZVS on can be gained with P_o lower than 95.6 W (63.73% load). When $U_{\rm in}$ is 12 V, ZVS on can be gained with P_o lower than 105 W (70% load). As to $U_{\rm in} = 16$ V, it is the range lower than 114 W (76% load). It is also obvious that the current of secondary diode decreases to zero softly. Therefore, reverse-recovery problem of secondary diode is removed within the entire operation range, meanwhile ZVS on of main MOSFETs is still obtained.

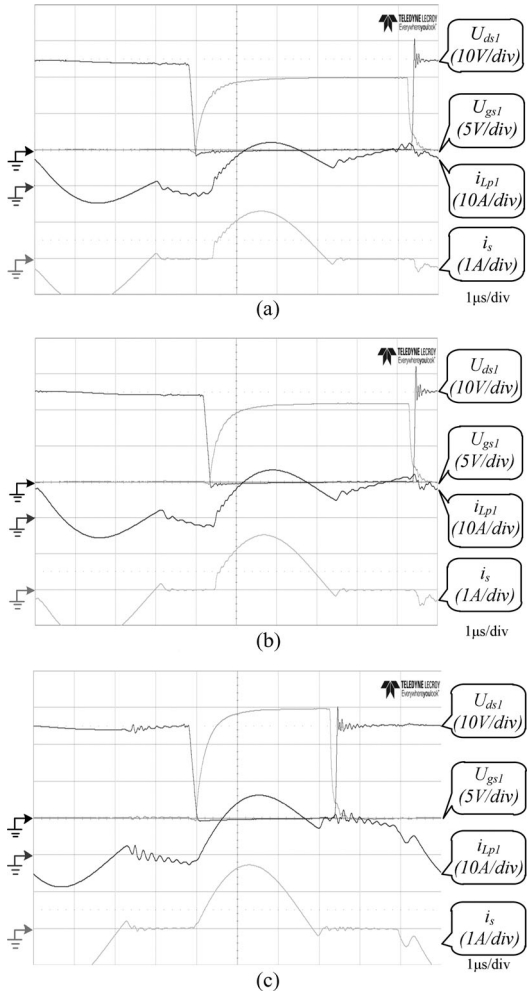


Fig. 16 (a) Waveforms of soft switching ($U_{\rm in} = 10.8$ V, $P_o = 95.6$ W). (b) Waveforms of soft switching ($U_{\rm in} = 12$ V, $P_o = 105$ W). (c) Waveforms of soft switching ($U_{\rm in} = 16$ V, $P_o = 114$ W).

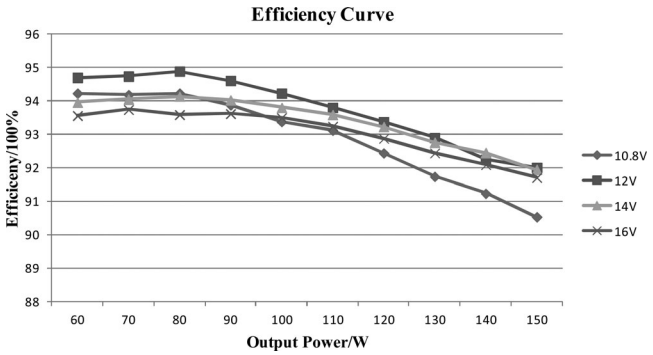


Fig. 17. Efficiency curves of the prototype at different loads and input voltages.

Fig. 17 shows the measured efficiency curve of the prototype. Compared with efficiency of 10.8, 12, 14, and 16 V input, the efficiency of 12 V input within the entire operation range is relatively high which is above 92%. The highest efficiency of 12 V input is 94.88%. The efficiency of the proposed converter is superior to the current-fed push–pull converter [8]. The converter can certainly achieve ZVS on of all the MOSFETs at the whole load conditions with small enough magnetic inductance

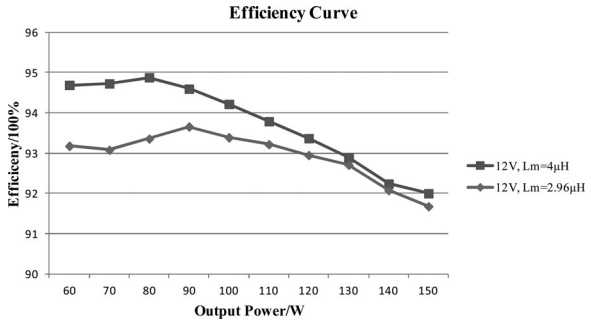


Fig. 18. Efficiency curves of the prototype at 12 V input voltage with different magnetic inductances.

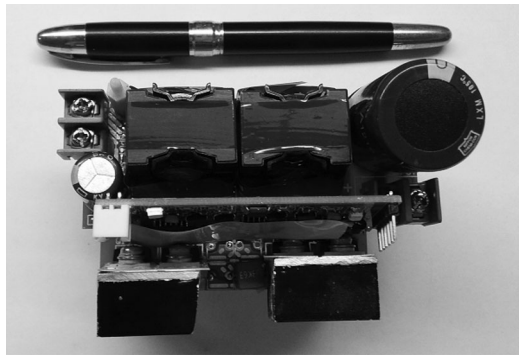


Fig. 19. Hardware circuit of the prototype.

according to (22). But the concomitant large input current ripple results in worse alternating current (ac) copper losses which bring down the efficiency of the converter, which can be seen in Fig. 18. Fig. 19 is the hardware circuit of the prototype.

The experimental results are consistent with the design. However, the proposed design is not applicable in high-power field because the large magnetizing ripple current increases the current stress of MOSFETs. It is suitable for low-power application such as vehicle inverters.

VI. Conclusion

In this paper, resonance analysis and soft-switching design of an isolated boost converter with coupled inductors are presented. Two kinds of resonance are analyzed to obtain ZVS on of main switches or ZCS off of secondary rectifying diodes. Relationship between the resonances is sketched and an optimized resonance between the two kinds of resonances is used to increase power density and lower converter cost. Moreover, by choosing appropriate magnetic inductance of the coupled inductors, ZVS on of the main MOSFETs and ZCS off of the secondary diodes can be achieved collectively at the same working conditions without any additional devices. In addition, the restricted range of duty ratio is removed and an optimal operation point with zero input ripple current is gained. At last, a 150 W, 12–360 V high efficiency prototype converter is built to verify the analysis, and the experimental results illustrate that the proposed converter is a competitive candidate for low power and high step-up applications with isolation requirements.

REFERENCES

[1] S.-J. Jang, C.-Y. Won, B.-K. Lee, and J. Hur, "Fuel cell generation system with a new active clamping current-fed half-bridge converter," *IEEE Trans. Energy Convers.*, vol. 22, no. 2, pp. 332–340, Jun. 2007.

[2] Z. Zhang, Z. Ouyang, O. C. Thomsen, and M. A. E. Andersen, "Analysis and design of a bidirectional isolated DC–DC converter for fuel cells and supercapacitors hybrid system," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 848–859, Feb. 2012.

[3] O. Hegazy, J. Van Mierlo, and P. Lataire, "Analysis, modeling, and implementation of a multidevice interleaved DC/DC converter for fuel cell hybrid electric vehicles," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4445–4458, Nov. 2012.

[4] L. Tang and G.-J. Su, "An interleaved reduced-component-count multivoltage bus dc/dc converter for fuel cell powered electric vehicle applications," *IEEE Trans. Power Electron.*, vol. 44, no. 5, pp. 1638–1644, Sep./Oct. 2008.

[5] Y. Park, B. Jung, and S. Choi, "Nonisolated ZVZCS resonant PWM DC–DC converter for high step-up and high-power applications," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3568–3575, Aug. 2012.

[6] I. Aharon and A. Kuperman, "Topological overview of powertrains for battery-powered vehicles with range extenders," *IEEE Trans. Power Electron.*, vol. 26, no. 3, pp. 868–876, Mar. 2011.

[7] R. L. Andersen and I. Barbi, "A ZVS-PWM three-phase current-fed push–pull DC–DC converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 3, pp. 838–847, Mar. 2013.

[8] H. Ma, L. Chen, and Z. Bai, "An active-clamping current-fed push-pull converter for vehicle inverter application and resonance analysis," in *Proc IEEE Int. Symp. Ind. Electron.*, 2012, pp. 160–165.

[9] Y. Wang, Q. Liu, J. Ma, and H. Ma, "A new ZVCS resonant voltage-fed push-pull converter for vehicle inverter application," in *Proc IEEE Int. Symp. Ind. Electron.*, 2013, pp. 1–6.

[10] V. Vaisanen, T. Riipinen, J. Hiltunen, and P. Silventoinen, "Design of 10 kW resonant push-pull DC–DC converter for solid oxide fuel cell applications," in *Proc. IEEE 14th Eur. Power Electron. Appl.*, 2011, pp. 1–10.

[11] T.-F. Wu, J.-C. Hung, J.-T. Tsai, C.-T. Tsai, and Y.-M. Chen, "An active-clamp push–pull converter for battery sourcing applications," *IEEE Trans. Ind. Appl.*, vol. 44, no. 1, pp. 196–204, Jan./Feb. 2008.

[12] E.-H. Kim and B.-H. Kwon, "High step-up resonant push-pull converter with high efficiency," *IET Trans. Power Electron.*, vol. 2, no. 1, pp. 79–89, Jan. 2009.

[13] I. Boonyaroonate and S. Mori, "A new ZVCS resonant push–pull DC/DC converter topology," in *Proc. IEEE 17th Annu. Appl. Power Electron. Conf.*, 2002, vol. 2, pp. 1097–1100.

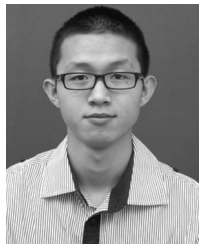
[14] Y. Zhao, W. Li, Y. Deng, and X. He, "Analysis, design, and experimentation of an isolated ZVT boost converter with coupled inductors," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 541–550, Feb. 2011.

[15] S.-K. Han, H.-K. Yoon, G.-W. Moon, M.-J. Youn, Y.-H. Kim, and K.-H. Lee, "A new active clamping zero-voltage switching PWM current-fed half bridge converter," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1271–1279, Nov. 2005.

[16] C.-L. Chu and C.-H. Li, "Analysis and design of a current-fed zero-voltage-switching and zero-current-switching CL-resonant push-pull dc–dc converter," *IET Trans. Power Electron.*, vol. 2, no. 4, pp. 456–465, Jul. 2009.

[17] J.-M. Kwon, K. Eung-Ho, B.-H. Kwon, and K.-H. Nam, "High-efficiency fuel cell power conditioning system with input current ripple reduction," *IEEE Trans. Ind. Electron.*, vol. 56, no. 3, pp. 826–834, Mar. 2009.

[18] W. Li, L. Fan, Y. Zhao, X. He, D. Xu, and B. Wu, "High-step-up and high-efficiency fuel-cell power-generation system with active-clamp flyback–forward converter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 599–610, Jan. 2012.



Yuxi Wang (S'13) was born in Zhejiang, China, in 1988. He received the B.Sc. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2011, where he is currently working toward the Ph.D. degree.

His current research interests include dc/dc converters and fault diagnosis.

Wei Liu (S'14) was born in Jilin, China, in 1988. He received the B.Sc. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2012, where he is currently working toward the M.Sc. degree.

His current research interests include LED drivers and LLC resonant converter.

Hao Ma (M'99) received the B.Sc., M.Sc., and Ph.D. degrees in applied power electronics and electrical engineering from Zhejiang University, Hangzhou, China, in 1991, 1994, and 1997, respectively.

He is currently a Professor in the College of Electrical Engineering, Zhejiang University. His research interests include advanced control in power electronics, fault diagnosis of power electronic circuits and systems, and application of power electronics.

Longyu Chen was born in Liaoning, China, in 1988. He received the B.Sc. and M.Sc. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 2010 and 2013, respectively.

He is currently an Electrical Engineer in GE (China) Research and Development Center Co., Ltd. His research interests include energy recycling system, resonance analysis and soft-switching design of high step-up dc/dc converters.