Naturally Clamped Zero-Current Commutated Soft-Switching Current-Fed Push–Pull DC/DC Converter: Analysis, Design, and Experimental Results

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***Abstract*—The proposed converter has the following features: 1) zero-current commutation (ZCC) and natural voltage clamping (NVC) eliminate the need for active-clamp circuits or passive snubbers required to absorb surge voltage in conventional current-fed topologies. 2) Switching losses are reduced significantly owing to zero-current switching of primary-side devices and zero-voltage switching of secondary-side devices. Turn-on switching transition loss of primary devices is also negligible. 3) Soft switching and NVC are inherent and load independent. 4) The voltage across primary-side device is independent of duty cycle with varying input voltage and output power and clamped at rather low reflected output voltage enabling the use of low-voltage semiconductor devices. These merits make the converter good candidate for interfacing low-voltage dc bus with high-voltage dc bus for higher current applications. Steady state, analysis, design, simulation, and experimental results are presented.**

***Index Terms*—Current-fed converter, dc/dc converter, natural clamping, soft switching, zero-current commutation.**

I. Introduction

TRANSPORTATION electrification has received significant interest owing to limited supply of fossil fuels and concern of global climate change [1], [2]. Battery-based electric vehicles (EVs) and fuel cell vehicles (FCVs) are emerging as viable solutions for transportation electrification with lower emission, better vehicle performance, and higher fuel economy. Compared with pure battery-based EVs, FCVs are quite appealing with the merits of zero-emission, satisfied driving range, short refueling time, high efficiency, and high reliability. A diagram of a typical FCV propulsion system is shown in Fig. 1 [3]–[5]. Bidirectional and unidirectional dc/dc converters are utilized to develop high-voltage bus for the inverter. The energy storage system (ESS) is used to overcome the limitations of lacking energy storage capability and fast power transient of FCVs.

Bidirectional converter with high boost ratio and high efficiency is required to connect the low-voltage ESS and high-voltage dc-link bus. Compared with nonisolated topologies, high-frequency (HF) transformer isolated converters are preferred with merits of high step up ratio, galvanic isolation, and flexibility of system configuration [6]. HF transformer isolated converters could be either voltage-fed [7]–[9] or current-fed [10]–[20]. Advantages and disadvantages of both types are compared in [21]–[23]. The voltage-fed converters have low switch voltage ratings enabling the use of switches with low ON-state resistance. This can significantly reduce conduction loss of primary-side switches. However, voltage-fed converters suffer from several limitations, i.e., high pulsating current at input, limited soft-switching range, rectifier diode ringing, duty cycle loss (if inductive output filter), high circulating current through devices and magnetics, and relatively low efficiency for high-voltage amplification and high-input current applications. Compared with voltage-fed converters, current-fed converters exhibit smaller input current ripple, lower diode voltage rating, lower transformer turns-ratio, negligible diode ringing, no duty cycle loss, and easier current control ability. Besides, current-fed converters can precisely control the charging and discharging current of ESS, which helps achieving higher charging/discharging efficiency. Thus, current-fed converter is more feasible for the application of ESS in FCVs.

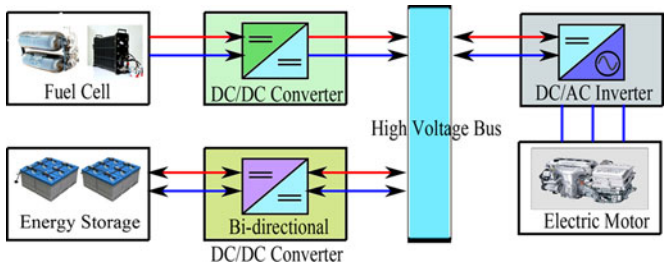

Fig. 1. Diagram of a FCV propulsion system.

Three topologies of isolated current-fed dc/dc converters, i.e., full-bridge [10]–[12], L-type half-bridge [13]–[15], and push–pull [16], [17] have been researched. One drawback of current-fed converters is the high turn-off voltage spike across the devices. Normally, active-clamp circuits [14]–[16], [24], [25], RCD passive snubbers [11], or energy recovery snubber [6] are employed to absorb the surge voltage and assist soft-switching. In RCD snubbers, energy absorbed by the clamping capacitor is dissipated in the resistor resulting in low efficiency. Active-clamp suffers from high current stress (peak) and higher circulating current at light load.

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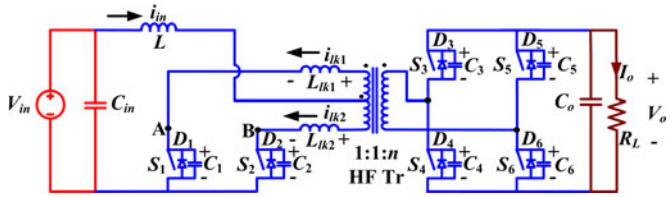

Fig. 2. Proposed ZCS current-fed push–pull dc/dc converter.

The leakage inductance and parasitic capacitance of the HF transformer were utilized to achieve zero-current switching (ZCS) in [17]–[19]. However, resonant current is much higher than input current that increases the current stress of devices and magnetics requiring higher VA rating components. Besides, the variable frequency modulation makes the control implementation difficult and complex [20]. External auxiliary circuits are utilized to achieve ZCS and reduce the circulating current in [26]–[28] but complex. Although the trapped energy can be recycled, the auxiliary circuits still contribute to a significant amount of loss. In current-fed bidirectional converter, active soft commutation technique [11], [29], [30] is proposed to divert the switch current to another switch through transformer to achieve natural or zero-current commutation (ZCC) thus reducing or eliminating the need of snubber.

In this paper, a novel secondary modulation-based naturally clamped soft-switching bidirectional snubberless current-fed push–pull converter is proposed as shown in Fig. 2. Natural voltage clamping (NVC) with ZCS of primary devices is achieved by proposed secondary modulation and therefore avoids the need of passive snubbers or active clamp making it snubberless. Switching losses are reduced significantly owing to ZCS of primary switches and ZVS of secondary switches that permits HF switching operation with smaller magnetics.

The objectives of this paper are to explain steady-state operation and analysis, illustrate design, and demonstrate experimental performance of the proposed converter. The objectives are realized and outlined in various sections as follows. Steady-state operation of the converter is explained and its mathematical analysis is reported in Section II. Detailed converter design procedure is illustrated in Section III. Analysis and design are verified by simulation results using PSIM 9.0.4 in Section IV. Experimental results on a laboratory prototype of 250 W are demonstrated to validate and show the converter performance in Section IV.

II. Operation and Analysis of the Converter

For the sake of simplicity, the following assumptions are made to study the operation and explain the analysis of the converter: 1) Boost inductor L is large enough to maintain constant current through it. 2) All the components are ideal. 3) Series inductors L_{lk1} and L_{lk2} include the leakage inductances of the transformer. The total value of L_{lk1} and L_{lk2} is represented as L_{lk_T}. L_{lk} represents the equivalent series inductor reflected to the high-voltage side. 4) Magnetizing inductance of the transformer is infinitely large.

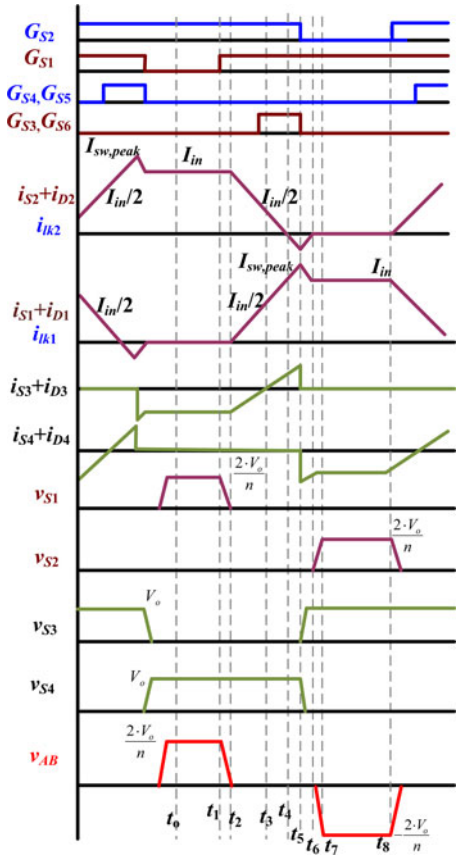

Fig. 3. Operating waveforms of proposed ZCS current-fed push–pull converter in the boost mode.

A. Boost Mode (Discharging Mode) Operation

In this part, the steady-state operation and analysis with ZCC and NVC concept has been explained. Before turning OFF one of primary-side switches (say S_1), the other switch (say S_2) is turned-on. Reflected output voltage $2Vo/n$ appears across the transformer primary. It diverts the current from one switch to the other one through transformer causing current through just triggered switch to rise and the current through conducting switch to fall to zero naturally resulting in ZCC. Later, the body diode across switch starts conducting and its gating signal is removed leading to ZCS turn-off of the device. Commutated device capacitance starts charging with NVC.

The steady-state operating waveforms of boost mode are shown in Fig. 3. The primary switches S_1 and S_2 are operated with identical gating signals phase-shifted with each other by 180° with an overlap. The overlap varies with the duty cycle, and the duty cycle should be kept above 50%. The steady-state operation of the converter during different intervals in a one half HF cycle is explained using the equivalent circuits shown in Fig. 4. For the rest half cycle, the intervals are repeated in the same sequence with other symmetrical devices conducting to complete the full HF cycle.

Interval 1 (Fig. 4(a); $t_o < t < t_1$): In this interval, primary-side switches S_2 and antiparallel body diodes D_3 and D_6 of secondary-side H-bridge switches are conducting. Power is transferred to the load through HF transformer. The

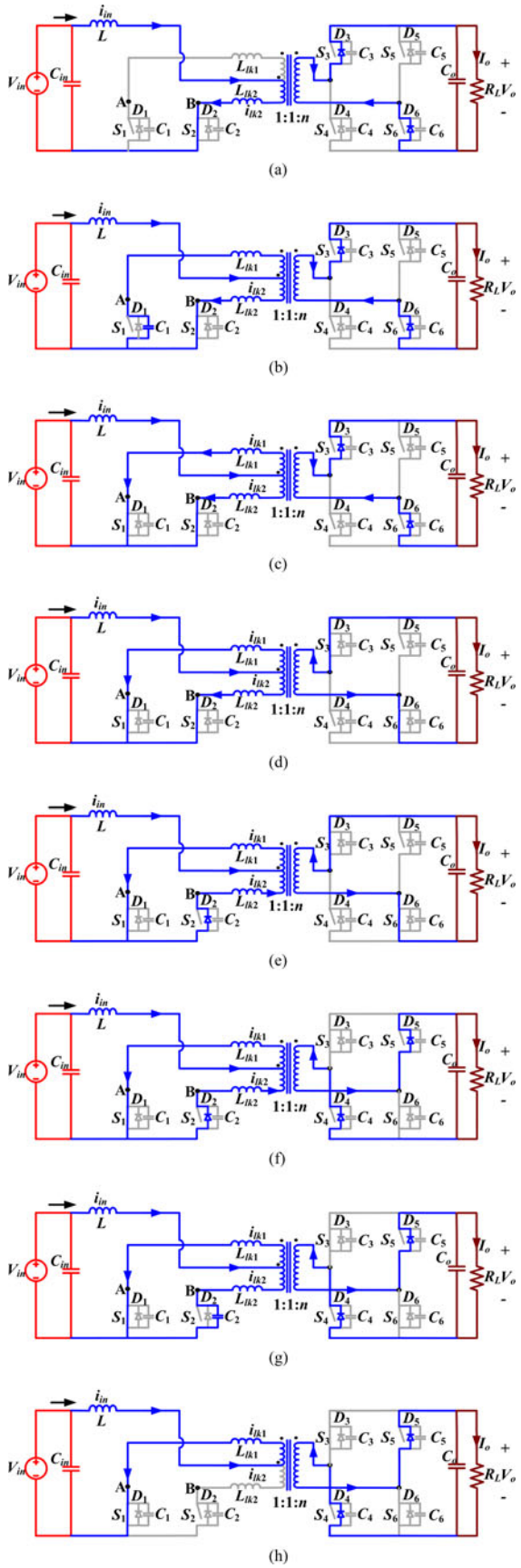

Fig. 4. Equivalent circuits during different intervals of the boost mode operation.

nonconducting secondary devices S_4 and S_5 are blocking output voltage V_o and the nonconducting primary devices S_1 are blocking reflected output voltage $2V_o/n$. The values of current through various components are

$$i_{S1} = 0, i_{S2} = I_{\text{in}}, i_{lk1} = 0, i_{lk2} = I_{\text{in}}, i_{D3} = i_{D6} = I_{\text{in}}/n.$$

Voltage across the switch S_1:V_{S1}= $2V_{\text{o}}/n$.

Voltage across the switches S_4 and S_5:$V_{S4} = V_{S5} = Vo$.

Interval 2 (Fig. 4(b); $t_1 < t < t_2$): At $t = t_1$, primary switch S_1 is turned-on. The corresponding snubber capacitor C_1 discharges in a very short period of time.

Interval 3 (Fig. 4(c); $t_2 < t < t_3$): All two primary switches are conducting. Reflected output voltages appear across inductors L_{lk1} and L_{lk2}, diverting/transferring the current through switch S_2 to S_1. It causes current through previously conducting device S_2 to reduce linearly. It also results in conduction of switch S_1 with zero current which helps reducing associated turn-on loss. The currents through various components are given by

$$i_{lk1} = i_{S1} = \frac{2 \cdot V_o}{n \cdot L_{lk\_T}} \cdot (t - t_2) \tag{1}$$

$$i_{lk2} = i_{S2} = I_{\text{in}} - \frac{2 \cdot V_o}{n \cdot L_{lk\_T}} \cdot (t - t_2) \tag{2}$$

$$i_{D3} = i_{D6} = \frac{I_{\text{in}}}{n} - \frac{4 \cdot V_o}{n^2 \cdot L_{lk\_T}} \cdot (t - t_2) \tag{3}$$

where $L_{lk\_T} = L_{lk1} + L_{lk2}$. At the end of this interval $t = t_3$, the antiparallel body diode D_3 and D_6 are conducting. Therefore, S_3 and S_6 can be gated on for ZVS turn-on. At the end of this interval, D_3 and D_6 commutates naturally. Current through all primary devices reaches $I_{\text{in}}/2$. Final values are: $i_{lk1} = i_{lk2} = I_{\text{in}}/2, i_{S1} = i_{S2} = I_{\text{in}}/2, i_{D3} = i_{D6} = 0$.

Interval 4 (Fig. 4(d); $t_3 < t < t_4$): In this interval, secondary H-bridge devices S_3 and S_6 are turned-on with ZVS. Currents through all the switching devices continue increasing or decreasing with the same slope as interval 3. At the end of this interval, the primary device S_2 commutates naturally with ZCC and the respective current i_{S2} reaches zero obtaining ZCS. The full current, i.e., input current is taken over by other device S_1. Final values are: $i_{lk1} = i_{S1} = I_{\text{in}}, i_{lk2} = i_{S2} = 0, i_{S3} = i_{S6} = I_{\text{in}}/n$.

Interval 5 (Fig. 4(e); $t_4 < t < t_5$): In this interval, the leakage inductance current i_{lk1} increases further with the same slope and antiparallel body diode D_2 starts conducting causing extended zero voltage to appear across commutated switch S_2 to ensure ZCS turn-off. Now, the secondary devices S_3 and S_6 are turned-off. At the end of this interval, current through switch S_1 reaches its peak value. This interval should be very short to limit the peak current though the transformer and switch reducing the current stress and kVA ratings.

The currents through operating components are given by

$$i_{S1} = i_{lk1} = I_{\text{in}} + \frac{2 \cdot V_o}{n \cdot L_{lk\_T}} \cdot (t - t_4) \tag{4}$$

$$i_{D2} = -i_{lk2} = \frac{2 \cdot V_o}{n \cdot L_{lk\_T}} \cdot (t - t_4) \tag{5}$$

$$i_{S3} = i_{S6} = \frac{I_{\text{in}}}{n} + \frac{4 \cdot V_o}{n^2 \cdot L_{lk\_T}} \cdot (t - t_4). \tag{6}$$

Interval 6 (Fig. 4(f); $t_5 < t < t_6$): During this interval, secondary switches S_3 and S_6 are turned-off. Antiparallel body diodes of switches S_4 and S_5 take over the current immediately. Therefore, the voltage across the transformer primary reverses polarity. The current through the switch S_1 and body diodes D_2 also start decreasing.

The currents through operating components are given by

$$i_{S1} = i_{lk1} = I_{sw,\text{peak}} - \frac{2 \cdot V_o}{n \cdot L_{lk\_T}} \cdot (t - t_5) \tag{7}$$

$$i_{D2} = -i_{lk2} = I_{D2,\text{peak}} - \frac{2 \cdot V_o}{n \cdot L_{lk\_T}} \cdot (t - t_5) \tag{8}$$

$$i_{D4} = i_{D5} = \frac{I_{lk,\text{peak}}}{n} - \frac{4 \cdot V_o}{n^2 \cdot L_{lk\_T}} \cdot (t - t_5). \tag{9}$$

At the end of this interval, current through D_2 reduces to zero and is commutated naturally. Current through S_1 reaches I_{in}.

Final values: $i_{lk1} = i_{S1} = I_{\text{in}}, i_{lk2} = i_{D2} = 0, i_{D4} = i_{D5} = I_{\text{in}}/n$.

Interval 7 (Fig. 4(g); $t_6 < t < t_7$): In this interval, snubber capacitor C_2 charges to $2V_o/n$ in a short period of time. Switch S_2 is in forward blocking mode now.

Interval 8 (Fig. 4(h); $t_7 < t < t_8$): In this interval, currents through S_1 and transformer are constant at input current I_{in}. Current through antiparallel body diodes of the secondary switches D_4 and D_5 is at I_{in}/n.

The final values are: $i_{lk1} = i_{S1} = I_{\text{in}}, i_{lk2} = i_{S2} = 0, i_{D4} = i_{D5} = I_{\text{in}}/n$.

Voltage across the switch $S_2 V_{S2} = 2V_o/n$.

In this half HF cycle, current has transferred from switch S_2 to S_1, and the transformer current has reversed its polarity.

B. Buck Mode (Charging Mode) Operation

In the reverse direction, the converter acts as a standard voltage-fed full-bridge center-tapped converter with inductive output filter. The regenerative braking energy can be fed back and recharge the low-voltage storage from high-voltage bus, thus increasing overall system efficiency. Standard phase-shift PWM control technique is employed to achieve ZVS of high-voltage side and ZCS of low-voltage side. At low-voltage side, devices need not be controlled because body diodes of the devices can take over as high-frequency rectifier.

The steady-state operating waveforms of buck mode are shown in Fig. 5. The secondary-side diagonal switch pairs S_3–S_6 and S_4–S_5 operated with identical gating signals phase-shifted with each other by 180° with a well-defined dead time gap. The steady-state operation of the converter during different intervals in a one half HF cycle is explained using the equivalent circuits shown in Fig. 6.

Interval 1 (Fig. 6(a); $t_o < t < t_1$): In this interval, secondary-side switch pair S_3–S_6 and body diode D_2 of primary-side switch are conducting. Power is transferred to the battery from high-voltage dc-link bus through HF transformer. The values of current through various components are: $i_{D1} = 0, i_{D2} = i_{\text{battery}}, i_{S3} = i_{S6} = i_{lk} = i_{\text{battery}}/n$. Voltage across

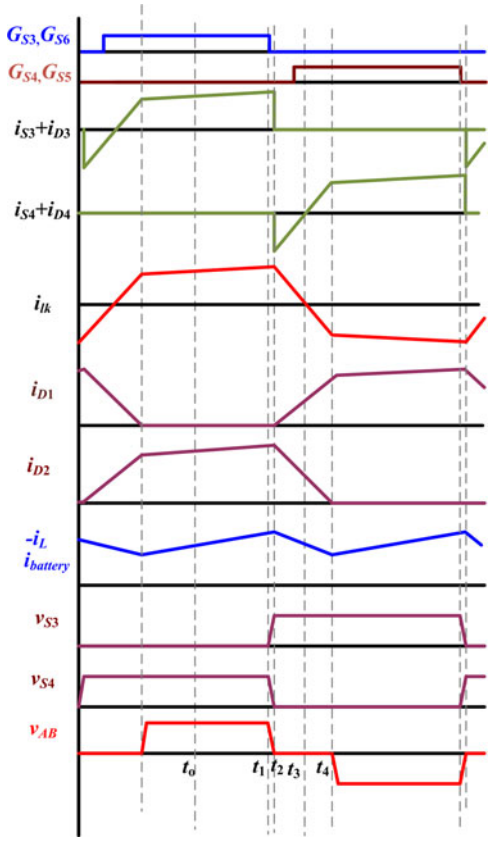

Fig. 5. Operating waveforms of proposed ZCS current-fed push–pull converter in the buck mode.

the diode D_1: $V_{D1} = 2V_o/n$. Voltage across the switches S_4 and S_5: $V_{S4} = V_{S5} = V_o$.

Interval 2 (see Fig. 6(b); $t_1 < t < t_2$): At $t = t_1$, secondary-side switch pair S_3–S_6 is turned-off. i_{lk} charges the snubber capacitor C_3 and C_6 and discharges the snubber capacitor C_4 and C_5 in a short period of time. Simultaneously, the capacitor C_1 discharges very fast. At the end of this interval $t = t_2$, the body diode D_4 and D_5 are conducting. As long as the H-bridge devices S_4 and S_5 are turned ON before i_{lk} changes its direction, ZVS turn-on can be assured. Final values are: $i_{D4} = i_{D5} = i_{lk} = i_{\text{battery}}/n, i_{D1} = 0, i_{D2} = i_{\text{battery}}, V_{D1} = 0; V_{S4} = V_{S5} = 0, V_{S3} = V_{S6} = V_o$.

Interval 3 (see Fig. 6(c); $t_2 < t < t_3$): Now output voltage appears across inductors L_{lk}, causing current to reduce linearly. The currents through various components are given by

$$i_{lk} = \frac{i_{\text{battery}}}{n} - \frac{V_o}{L_{lk}} \cdot (t - t_2) \tag{10}$$

$$i_{D1} = \frac{n \cdot V_o}{2L_{lk}} \cdot (t - t_2) \tag{11}$$

$$i_{D2} = i_{\text{battery}} - \frac{n \cdot V_o}{2L_{lk}} \cdot (t - t_2). \tag{12}$$

Final values are: $i_{D4} = i_{D5} = i_{lk} = 0$, $i_{D1} = i_{D2} = i_{\text{battery}}/2$.

Interval 4 (Fig. 6(d); $t_3 < t < t_4$): In this interval, S_4 and S_5 are turned-on with ZVS. Currents through all the switching

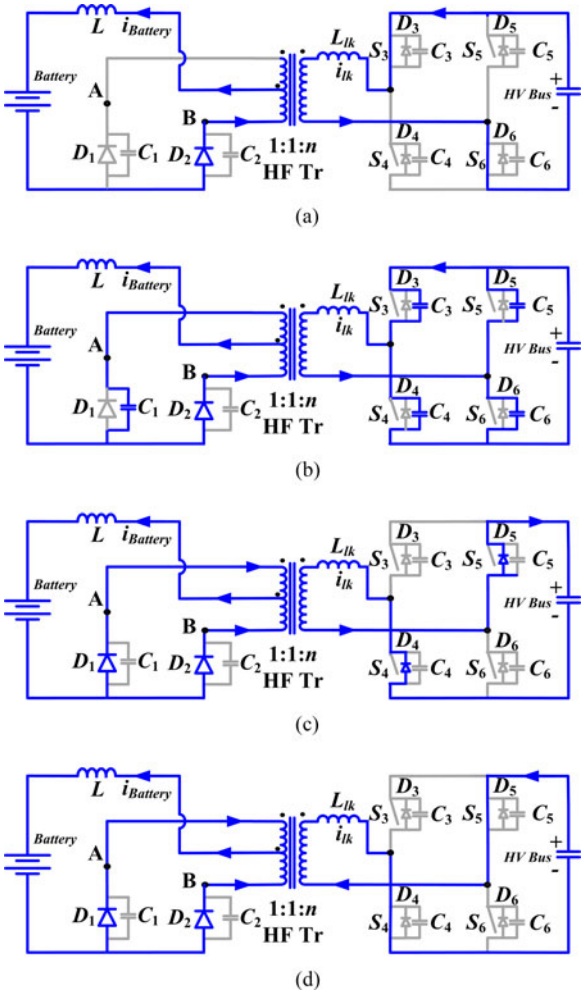

Fig. 6. Equivalent circuits during different intervals of the buck mode operation.

devices continue increasing or decreasing with the same slope as interval 3. At the end of this interval, current flowing through body diode D_2 decreases to zero obtaining ZCS. Final values are: $i_{lk} = -i_{\text{battery}}/n, i_{D1} = i_{\text{battery}}, i_{D2} = 0$.

III. Design of the Converter

In this Section, converter design procedure is illustrated by a design example for the following specifications: input voltage $V_{\text{in}} = 12$ V, output voltage $V_o = 150$ to 300 V, output power $P_o = 250$ W, switching frequency $f_s = 100$ kHz. The design equations are presented to determine the components' ratings. It helps selection of the components as well as to predict the converter performance theoretically.

1) Maximum voltage across the primary switches is

$$V_{P,\text{SW}} = \frac{2 \cdot V_o}{n}. \tag{13}$$

2) Voltage conversion ratio or input and output voltages are related as

$$V_o = \frac{n \cdot V_{\text{in}}}{2 \cdot (1-d)} \tag{14}$$

where d is the duty cycle of primary switches. This equation is derived on the condition that antiparallel diode conduction time (e.g., interval 6) is quite short and negligible with the intention to ensure ZCS of primary switches without significantly increasing the peak current. However, at light-load condition of the converter, fuel cell stack is supplying most of the power to propulsion system and battery is supplying only auxiliary load, and the antiparallel diode conduction time is comparatively large; (14) is not valid any more. Due to the existence of longer antiparallel diode conduction period, the output voltage is boosted to higher value than that of nominal boost converter. For such cases, (14) is modified into the following:

$$V_o = \frac{n \cdot V_{\text{in}}}{2 \cdot (1-d-d')} \tag{15}$$

where d' is given by

$$d' = d - 0.5 - \frac{n \cdot I_{\text{in}} \cdot L_{lk\_T} \cdot f_s}{2 \cdot V_o}. \tag{16}$$

3) Average input current is $I_{\text{in}} = P_o/(\eta V_{\text{in}})$. Assuming an ideal efficiency η of 95%, $I_{\text{in}} = 21.9$ A. Total leakage inductance of the transformer or series inductance L_{lk_T} is calculated using

$$L_{lk\_T} = L_{lk1} + L_{lk2} = \frac{2 \cdot V_o \cdot (d-0.5)}{n \cdot I_{\text{in}} \cdot f_s}. \tag{17}$$

4) The current stress and voltage stress of major components are given in Table I.
5) The selection of transformer turns-ratio is selected to maintain duty cycle $d > 0.5$. By using (14),

$$n < \frac{2 \cdot V_{o,\min}(1-d_{\min})}{V_{\text{in}}}. \tag{18}$$

Therefore, maximum value of $n = 12.5$ for $V_{o,\min} = 150$ V. Fig. 7(a) shows variation of total value of series inductances L_{lk_T} (H) with respect to power transferring ability P (W) for four values of turns-ratio. With the increase of turns-ratio, the value of L_{lk_T} decreases. It is difficult to realize low leakage inductance with high turns-ratio. In addition, higher turns-ratio may lead to more transformer loss because of higher copper loss, higher eddy current from proximity effect, and higher core loss due to larger size. However, increasing the turns-ratio can reduce the maximum voltage across the primary switches, which permits use of low-voltage devices with low on-state resistance [as shown by Fig. 7(b)]. Thus, conduction losses in the primary-side semiconductor devices can be significantly reduced. An optimum turns-ratio $n = 10$, duty ratio $d = 0.8$ are selected to achieve an acceptable tradeoff. Output voltage can be regulated from 150 to 300 V by modulating the duty ratio from 0.6 to 0.8 including battery voltage variation due to its charging and discharging characteristics.
6) Leakage inductance $L_{lk_T} = 8.18\ \mu$H for the given values from (17). Here, series inductors L_{lk1} and L_{lk2} are chosen to be equal to half of L_{lk_T}: $L_{lk1} = L_{lk2} = 4.09\ \mu$H. Value

TABLE I
COMPARISON OF PARAMETERS BETWEEN PUSH–PULL ACTIVE-CLAMPED ZVS AND PROPOSED ZCS CURRENT-FED TOPOLOGIES

Parameters	Active-clamped ZVS	Proposed ZCS
Peak current through transformer	$3I_{in}/2$ (32.9A)	I_{in} (21.9A)
RMS current through transformer	$\frac{I_{in}}{2}\sqrt{\frac{3+8\cdot\frac{T_{DR}}{T_s}}{3}}$ (13.6A)	$I_{tr,rms}=I_{in}\sqrt{\frac{2-d}{3}}$ (13.8A)
Peak current through primary switches	$3I_{in}/2$ (32.9A)	I_{in} (21.9A)
RMS current through primary switches	$\frac{I_{in}}{2}\sqrt{\frac{2+d+8\cdot\frac{T_{DR}}{T_s}}{3}}$ (13.4A)	$I_{P,rms}=I_{in}\sqrt{\frac{2-d}{3}}$ (13.8A)
Peak current through clamping switches	$I_{in}/2$ (11.0A)	
RMS current through clamping switches	$\frac{I_{in}}{2}\cdot\sqrt{(1-d)/3}$ (2.45A)	
Peak current through secondary switches/diodes	$2I_{in}/n$ (4.39A)	I_{in}/n (2.19A)
Average current through secondary diodes	$I_{DR,avg}=P_o/(2V_o)$ (0.42A)	$I_{D,av}=\frac{I_{in}\cdot(7-6d)}{8n}$ (0.6A)
RMS current through secondary switches		$I_{S,rms}=\frac{I_{in}}{2n}\sqrt{\frac{2d-1}{3}}$ (0.49A)
Voltage across primary switches/clamping switches	$\frac{V_{in}}{1-d}$ (80V)	$\frac{2V_o}{n}$ (60V)
Voltage across secondary switches/diodes	V_o (300V)	V_o (300V)

of the boost inductor is given by

$$L=\frac{V_{\rm in}\cdot(d-0.5)}{\Delta I_{\rm in}\cdot f_s}. \tag{19}$$

Unequal design of series inductors L_{lk1} and L_{lk2} is also permitted. For such cases, (19) is modified into the following:

$$L=\frac{(V_{\rm in}+\frac{V_o}{n}-\frac{2\cdot V_o\cdot L_{lk\_\min}}{n\cdot L_{lk\_T}})\cdot(d-0.5)}{\Delta I_{\rm in}\cdot f_s} \tag{20}$$

where $L_{lk\_\min}$ is the minimum value of L_{lk1} and L_{lk2}.

7) The relation between output power and duty cycle is

$$P=\frac{n\cdot v_{\rm in}^2-v_o\cdot v_{\rm in}\cdot(3-4\cdot d)}{n\cdot L_{lk}\cdot f_s}. \tag{21}$$

Push–pull active-clamped current-fed ZVS topology [16], [17] and the proposed push–pull current-fed ZCS topology have been compared in Table I, where $V_{\rm in}=12$ V, $V_o=300$ V, $n=10$, $P_o=250$ W, $f_s=100$ kHz, $I_{\rm in}=21.93$ A, $\frac{T_{DR}}{T_s}=\frac{n\cdot V_{\rm in}}{V_o}=0.2$, duty cycle $d=0.85$ for active-clamped ZVS and 0.8 for proposed ZCS topology. It is clear from Table I that that peak current stress through transformer and secondary-side switches of proposed ZCS converter is considerably lower. More importantly, active-clamped current-fed ZVS topology has reduced boost capacity compared to proposed topology by 20% (not maintaining property of true boost converter). In addition, the voltage across the primary switches of proposed topology is clamped at lower voltage than active-clamped topology that reduced their conduction losses owing to low on-state resistance of low-voltage devices. The efficiency of the proposed converter is higher due to reduced losses associated with clamp circuit and main primary switches.

IV. SIMULATION AND EXPERIMENTAL RESULTS

Proposed converter has been simulated using software PSIM 9.0.4. Simulation results for input voltage $V_{\rm in}=12$ V, output voltage $V_o=300$ V, output power $P_o=250$ W, device switching frequency $f_s=100$ kHz are illustrated in Fig. 8. Simulation results coincide closely with theoretically predicted waveforms. It verifies the steady-state operation and analysis of the converter presented in Section II.

Waveforms of current through the input inductor L and voltage V_{AB} are shown in Fig. 8(a). The ripple frequency of input inductor current i_L is $2\times$ f_s resulting in a reduction in size. Voltage waveform V_{AB} shows that voltage across the primary switches is naturally clamped at low voltage, i.e., $2V_o/n$. Fig. 8(b) shows current waveforms through primary switches S_1 and S_2 and secondary switches S_3 and S_4 including the currents flowing through their respective body diodes, phase shifted with each other by 180° (S_1 versus S_2, S_5 versus S_6). Primary switch currents $[I(S_1), I(S_2)]$ are diverted from one switch (say S_1) to the other one (S_2) causing one switch to rise to $I_{\rm in}$ and the other one to fall to zero. This clearly demonstrates claimed ZCC of primary switches. The negative primary currents correspond to conduction of body diodes before the switches are turned-off, which ensures ZCS turn-off of the primary switches. As shown in current waveforms of S_3 and S_4 in Fig. 8, the antiparallel diodes of switches conduct prior to the conduction of corresponding switches, which verifies ZVS of the secondary-side switches.

Experimental prototype of the proposed push–pull converter, as shown in Fig. 9, is built for the specifications and design given in Section III. Details of the experimental converter are given in Table II. Since the total value of leakage inductance of HF transformer is lower than the desired value given in Section III, two external small size series inductors have been added, which can be avoided in practical industrial converter if transformer

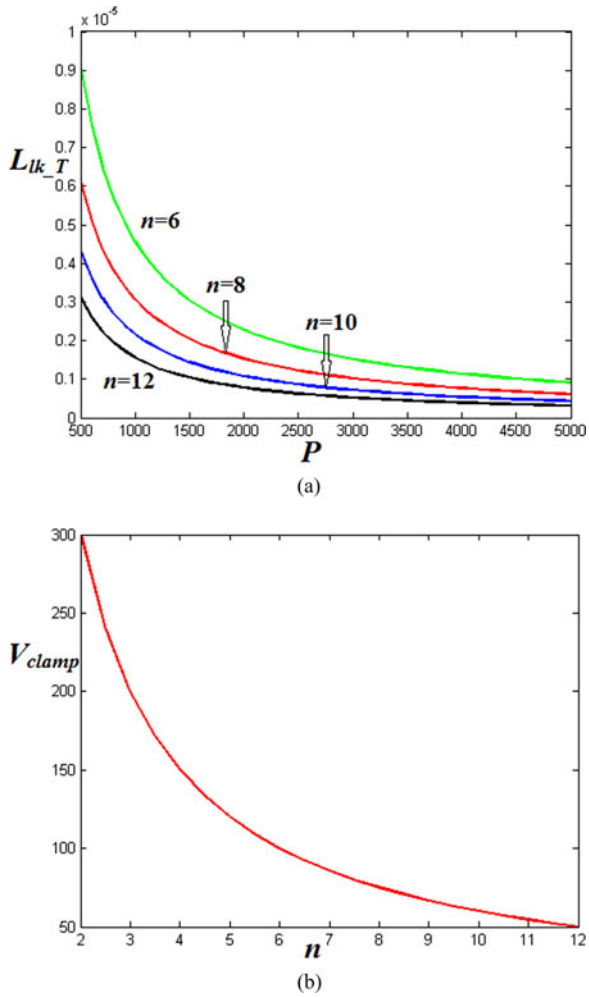

Fig. 7. Variation of (a) Total value of series inductances L_{lk_T} (H) with respect to power transferring ability P (W), and (b) clamped voltage across primary switches V_{clamp} for various transformer turns-ratio n.

TABLE II
MAJOR COMPONENTS' PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Components	Parameters
Primary switches S_1 ~ S_2	IRFB4110GPBF 100V, 180A. $R_{ds,\mathrm{on}}$ = 3.7 mΩ
Secondary switches S_3 ~ S_4	IPP60R125CP 650V, 11A. $R_{ds,\mathrm{on}}$ = 0.125Ω
HF transformer	3C95ETD49 ferrite core; Primary turns N_1=7, Secondary turns N_2=70 Leakage inductances reflected to primary, 264nH and 375nH respectively
External series inductors	TDK5901PC40Z core, 3.5μH and 3.4μH
Input boost inductor L	3C95ETD49 ferrite core, turns N = 12 L=22.5 μH
Input capacitors C_{in}	4.7 mF, 50V electrolytic 2.2μF high-frequency film capacitor
Output capacitors C_o	220uF, 450V electrolytic capacitor 0.68uF, 450V high frequency film capacitor

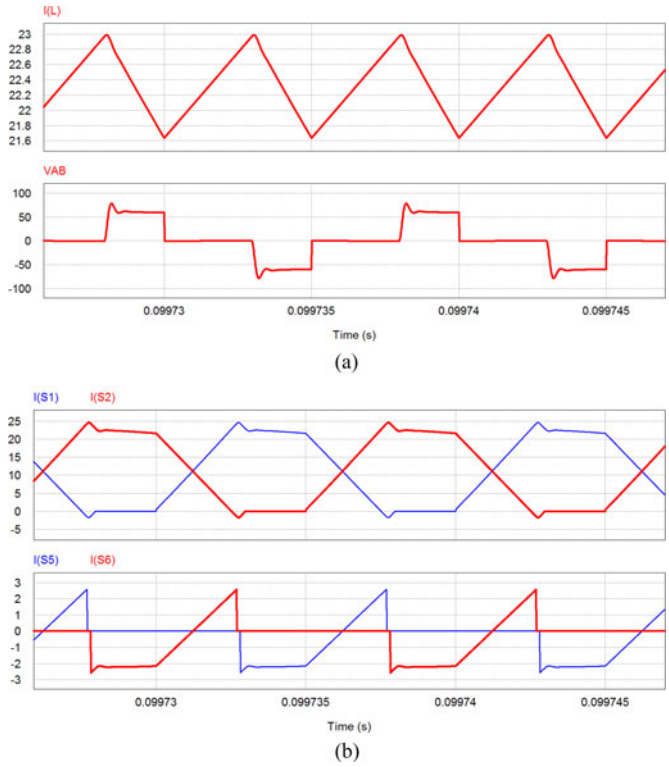

Fig. 8. Simulation results for output power of 250 W at 300 V. (a) Current through input inductor i_L and voltage V_{AB}. (b) Primary switches currents i_{S1} and i_{S2} and secondary switches currents i_{S3} and i_{S4}.

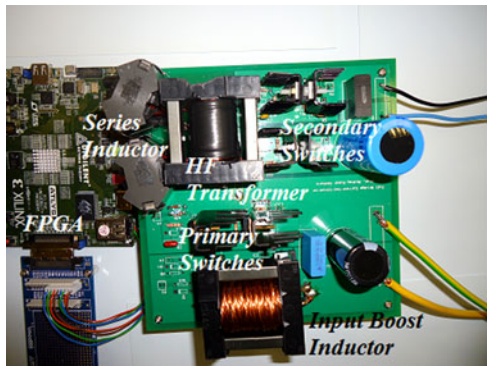

Fig. 9. Photograph of the laboratory prototype.

is designed properly. Also, slight deviation in this value should not affect the performance too much. Gate signals are generated using Xilinx Spartan-6 FPGA design platform.

Experimental results for output power of 250 and 100 W at 300 V are shown in Figs. 10 and 11 respectively. Parts (c) and (d) of Figs. 10–11 show gate-to-source V_{gs} and drain-to-source V_{ds} voltage waveforms across the primary devices, and the device current waveform. This clearly confirms the ZCS of primary devices. Current through the switch naturally goes to zero and antiparallel body diode starts conducting prior to removal of gate signal. It can be clearly noticed from the waveforms that gate voltage V_{gs} falls to zero and thereafter, the switch voltage V_{ds} starts rising. The extended zero voltage across the device is caused by antiparallel body diode conduction as is clear from

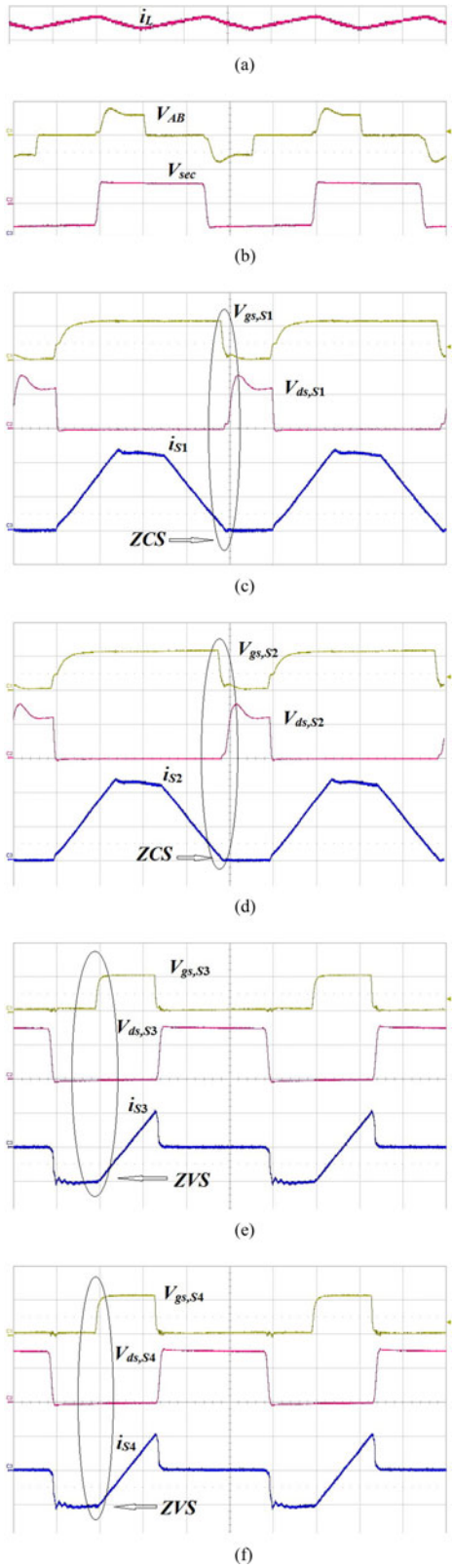

Fig. 10. Experimental results for output power of 250 W at 300 V(x-axis: 2μs/div): (a) Boost inductor current i_L (5 A/div). (b) Voltage v_{AB} (100 V/div) and voltage across secondary of transformer $v_{\rm sec}$ (500 V/div), (c) and (d) Gate-to-source voltage $V_{\rm gs}$ (10 V/div) and drain-to-source voltage $V_{\rm ds}$ (50 V/div) across the primary-side MOSFETs and currents through them (10 A/div). (e) and (f) Gate-to-source voltage $V_{\rm gs}$ (10 V/div) and drain-to-source voltage $V_{\rm ds}$ (200 V/div) across the secondary-side MOSFETs and currents through them (2 A/div).

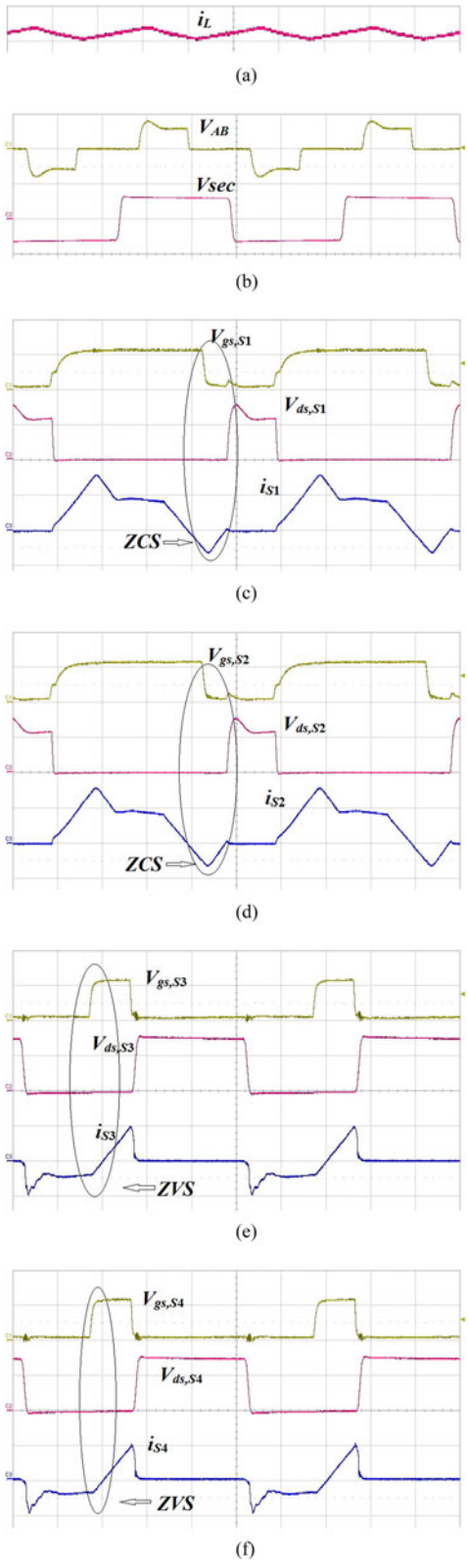

Fig. 11. Experimental results for output power of 100 W at 300 V(x-axis: 2 μs/div): (a) Boost inductor current i_L (5 A/div), (b) voltage v_{AB} (100 V/div) and voltage across secondary of transformer $v_{\rm sec}$ (500 V/div). (c) and (d) Gate-to-source voltage $V_{\rm gs}$ (10 V/div) and drain-to-source voltage $V_{\rm ds}$ (50 V/div) across the primary-side MOSFETs and currents through them (10 A/div). (e) and (f) Gate-to-source voltage $V_{\rm gs}$ (10 V/div) and drain-to-source voltage $V_{\rm ds}$ (200 V/div) across the secondary-side MOSFETs and currents through them (2 A/div).

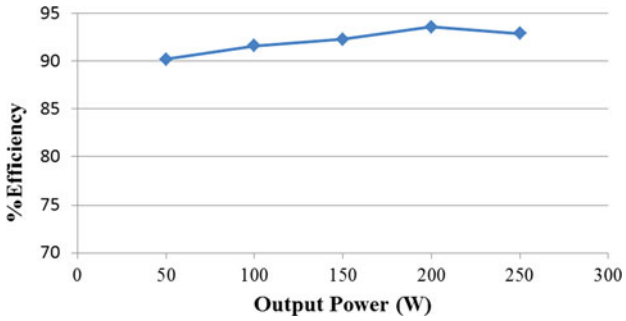

Fig. 12. Plot of efficiency versus output power for different load condition.

switch current waveform. Parts (e) and (f) of Figs. 10–11 obviously show the ZVS turn-on of the secondary switches. Gating signals to secondary switches $V_{\mathrm{gs},S3}$ (Top switch S_3) $V_{\mathrm{gs},S4}$ (Bottom switch S_4) are applied when voltage across them $V_{\mathrm{ds},S3}$ and $V_{\mathrm{ds},S4}$, respectively, is zero already. Besides, its body diode conducts prior to switch conduction confirming ZVS of secondary devices.

In addition, the turn-on procedure of primary switches is also demonstrated in waveforms shown in Fig. 10(c)-(d) and Fig. 11(c)-(d). Before turning ON, the voltage across primary switch is clamped at $2V_o/n = 60$ V. When the switch is gated ON, the current through it is rising at a constant slope from zero. With this limited *di/dt* through primary switch and low clamped voltage across it, the turn-on switching transition loss (due to overlap of switch voltage and current during switching transition time) can be regarded as negligible. Considering ZCS turn-off of the primary switches and ZVS turn-on of the secondary-side switches mentioned previously, the total switching losses are reduced enormously.

Voltages across the primary winding of the HF transformer V_{AB} are illustrated in parts (b) of Figs. 10–11. The high-frequency bipolar voltage waveform clearly states the clamped devices' voltage (less than 100 V). Low on-state resistance can be used due to the naturally low clamped voltage across them resulting in lower conduction loss and higher efficiency. Part (a) of Figs. 12–13 show the boost inductor current waveforms with $2\times$ device switching frequency, which brings a reduction in the size of the inductor.

Fig. 12 shows measured efficiency for different load for the proposed design and the developed laboratory prototype. The peak efficiency of 93.6% for 200 W and full load efficiency 92.9% for 250 W are obtained in forward direction. Loss distribution estimation from the loss model given in [31] is Fig. 13. It is easy to find that conduction losses of primary devices are rather low because of the usage of low-voltage devices. Switching loss of both sides of HF transformer are reduced significantly due to soft switching. A considerable part of total loss is from boost inductor and HF transformer. The percentage of this part of loss can be reduced with the increase of power level and optimized design. Compared with similar topologies with active-clamp circuits or snubber circuits, efficiency can be improved more than 2% for the experimental prototype.

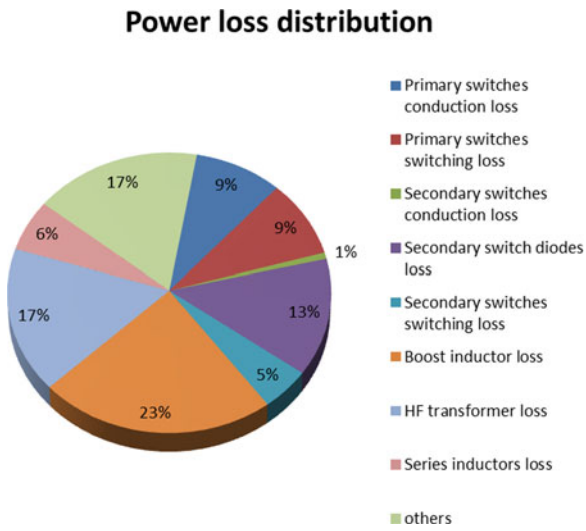

Fig. 13. Loss comparison of proposed converter at full load condition.

V. Summary and Conclusion

This paper presents a novel soft-switching snubberless bidirectional current-fed isolated push–pull dc/dc converter for application of the ESS in FCVs. A novel secondary-side modulation method is proposed to eliminate the problem of voltage spike across the semiconductor devices at turn-off. The above claimed ZCC and NVC of primary devices without any snubber are demonstrated and confirmed by the simulation and experimental results. ZCS of primary-side devices and ZVS of secondary-side devices are achieved, which reduces the switching losses significantly. Soft-switching is inherent and is maintained independent of load. Once ZCC, NVC, and soft switching are designed to be obtained at rated power, it is guaranteed to happen at reduced load unlike voltage-fed converters. Turn-on switching transition loss of primary devices is also shown to be negligible. Hence, maintaining soft switching of all devices substantially reduces the switching loss and allows higher switching frequency operation for the converter to achieve a more compact and higher power density system. Proposed secondary modulation achieves natural commutation of primary devices and clamps the voltage across them at low voltage (reflected output voltage) independent of the duty cycle. It, therefore, eliminates requirement of active-clamp or passive snubber. Usage of low-voltage devices results in low conduction losses in primary devices, which is significant due to higher currents on primary side. The proposed modulation method is simple and easy to implement. These merits make the converter promising for interfacing low-voltage dc bus with high-voltage dc bus for higher current applications such as FCVs, front-end dc/dc power conversion for renewable (fuel cells/PV) inverters, UPS, microgrid, V2G, and energy storage. The specifications are taken for FCV but the proposed modulation, design, and the demonstrated results are suitable for any general application of current-fed converter (high step-up). Similar merits and performance will be achieved.

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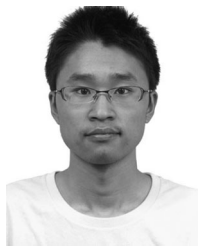

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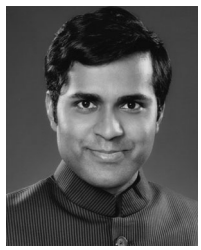

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