Improved Transient Response of Controllers by Synchronizing the Modulator With the Load Step: Application to V^2I_c

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***Abstract*— V^2I_c is a ripple-based control with an excellent performance for load transients and reference voltage tracking because it exhibits a feedforward of the load current and the error of the output voltage. However, if V^2I_c is modulated with constant frequency, constant on-time or constant off-time, its dynamic response is hindered by delays in the response. This paper proposes a technique that synchronizes the clock of the converter to initialize the duty cycle when a worst-case load transient occurs using the current through the output capacitor to detect load transients. It is exemplified on a V^2I_c control but it is applicable to most of controllers as it only acts on the modulator.**

***Index Terms*—Clock synchronization, dynamic voltage scaling, load transient, point of load, V^2I_c.**

I. Introduction

V^2I_c (see Fig. 1), proposed in [1], is a ripple-based control that presents a very fast dynamic response under load perturbations and reference voltage steps [2], [3]. It is composed by a slow loop, where the output voltage is regulated with a linear controller, and a fast loop, composed by the error of the output voltage and the current through the output capacitor. An optional artificial compensating ramp can be added in the fast loop in order to stabilize the converter.

As the current through the output capacitor is the difference between the current through the inductor and the output current, the control exhibits inherently a feedforward of the load current. Whenever the load changes, this disturbance is reproduced in the current through the output capacitor which produces an almost instantaneous change in the control signal and in the duty cycle. This way, the control presents a very fast response under load perturbations. The error of the output voltage is also added in the fast loop and, consequently, a step in the reference voltage causes an instantaneous reaction in the control signal. Therefore, V^2I_c can be used in applications with reference voltage tracking such as in microprocessors with dynamic voltage scaling.

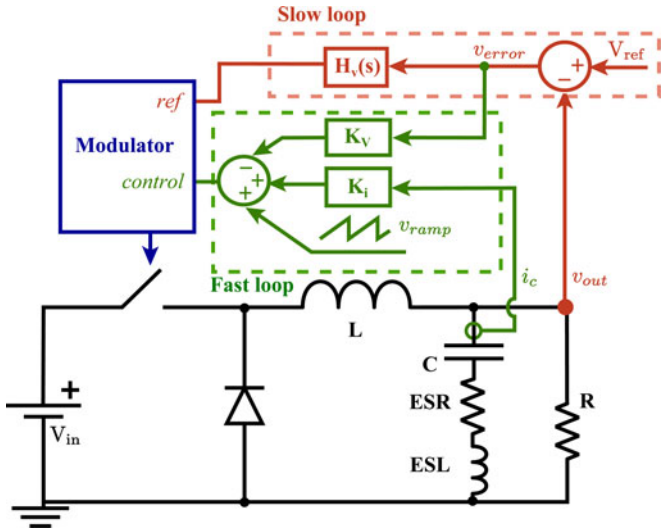

Fig. 1. Control scheme of V^2I_c.

In the literature, a simplified version of V^2I_c control, where the reference voltage is not included in the fast loop, is presented in [4] with constant on-time modulation and no artificial compensating ramp (see Fig. 2). As the reference voltage step acts as a constant offset if it does not change, [1] and [4] with the same modulation have the same transient response under load perturbations.

The current through the output capacitor is estimated with a transimpedance amplifier [5] (see Fig. 3) in order not to increase the impedance of the capacitor. The current sensor is designed so that it behaves like an impedance proportional to the impedance of the output capacitor and, as a result, the measured current is proportional to the current through the output capacitor. Notice that the actual implementation of V^2I_c only needs to sense the output voltage.

Even though V^2I_c control can react very fast under load disturbances, the control is not able to react immediately under certain cases due to constraints in the modulation. For the constant frequency modulation, if a positive load transient occurs during the off-time, the control is unable to react immediately because the on-time is synchronized with the clock and it cannot begin until the next period (see Fig. 4). This causes an additional

Manuscript received December 20, 2013; revised February 25, 2014; accepted March 25, 2014. Date of publication March 28, 2014; date of current version October 15, 2014. This work was supported in part by the Spanish Government Innovation and Science Office (MCINN) under Research Grant DPI-2010-20096, by the "FAST" project, and by the EU Grant FP7-ICT-2011-8 – PowerSWIPE–Project 318529. Recommended for publication by Associate Editor R. Redl.

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Digital Object Identifier 10.1109/TPEL.2014.2314242

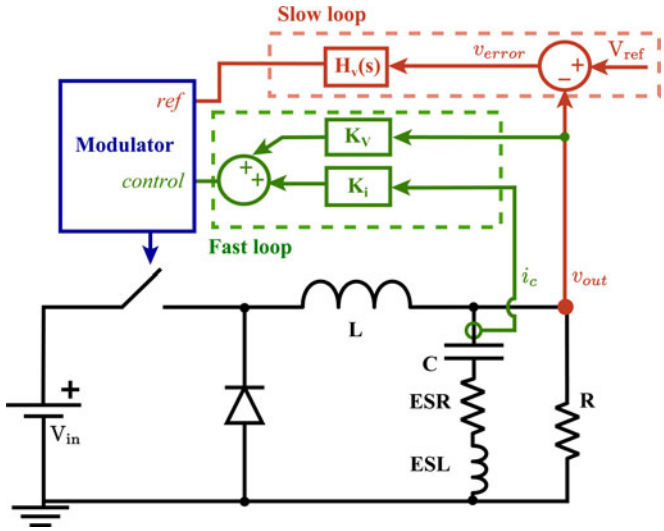

Fig. 2. Control scheme of the simplified $V^2 I_c$ proposed in [4].

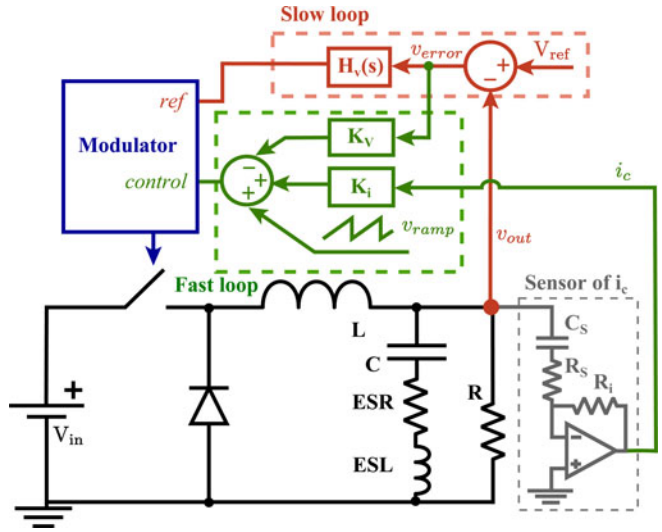

Fig. 3. Control scheme of $V^2 I_c$ with the implementation of the current sensor.

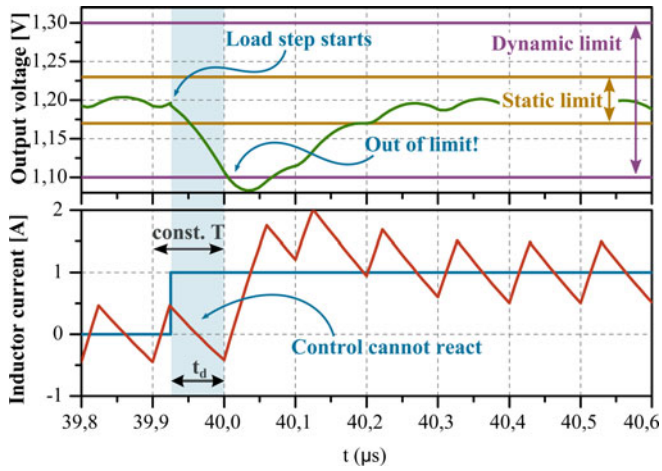

Fig. 4. Dynamic response under worst-case load step of a constant frequency modulation.

drop of the output voltage that does not depend on the dynamic behavior of the control. For the constant on-time modulation, an additional overshoot of the output voltage, that is independent of the control, occurs if a negative load transient occurs during the constant on-time.

As a consequence of this inherent delay, the effectiveness of very fast controls, such as $V^2 I_c$, is hindered as this deviation of the output voltage is independent of the dynamic behavior of the control.

This paper proposes a technique called "**C**lock **P**ulse **S**ynchronization" based on the current through the output capacitor ($\mathrm{CPSI_c}$) in order to counteract the limitations of the modulator. For the case of constant frequency modulation, this technique allows the control to start an on-time when a positive load transient occurs. It is exemplified on a $V^2 I_c$ control but it can be applied to most of controllers as it only acts on the modulator. A wide variety of controls can benefit from the proposed technique:

1) peak current mode and a voltage mode control with forced constant switching frequency;
2) advanced very fast controls that can be modulated with constant switching frequency like the controls proposed in [1], [6]–[12].

The paper is structured as follows. Section II explains the effect in the deviation of the output voltage of the inherent delays of the modulator. Section III explains the proposed technique to overcome the limitations of the modulation and minimize the voltage deviation under load transients. Section IV shows the experimental validation of the proposed technique and Section V summarizes the contributions of the article. The simulation results of the article are obtained from the program Simplis.

II. Effect in the Voltage Deviation of the Inherent Delays in the Switching Action of the Modulators

Even an ideal instantaneous control cannot prevent a certain deviation of the output voltage under a load transient. For a Buck converter, the minimum deviation of the output voltage is given by (1) for the loading case and (2) for the unloading case without considering the ESR and the ESL of the output capacitor [13]

$$\triangle v_{o,\,\mathrm{loading}}^{\min} = \frac{1}{C} \cdot \frac{\triangle i_o^2}{2(V_{in} - v_o)} L \tag{1}$$

$$\triangle v_{o,\,\mathrm{unloading}}^{\min} = \frac{1}{C} \cdot \frac{\triangle i_o^2}{2 v_o} L \tag{2}$$

In (1) and (2), the parameters are the minimum voltage deviation during the loading and unloading transient, $\triangle v_{o,\mathrm{loading}}^{\min}$ and $\triangle v_{o,\mathrm{unloading}}^{\min}$, the load current step, $\triangle i_o$, the input voltage, V_{in}, the output voltage, v_o, the output filter inductor, L, and the output capacitor, C. More accurate formulas can be found in [14].

By analyzing the topology and (1) and (2), it is well-known [14], [15] that the deviation of the output voltage under unloading transients is greater than under loading transients for Buck converters operating with a small duty cycle.

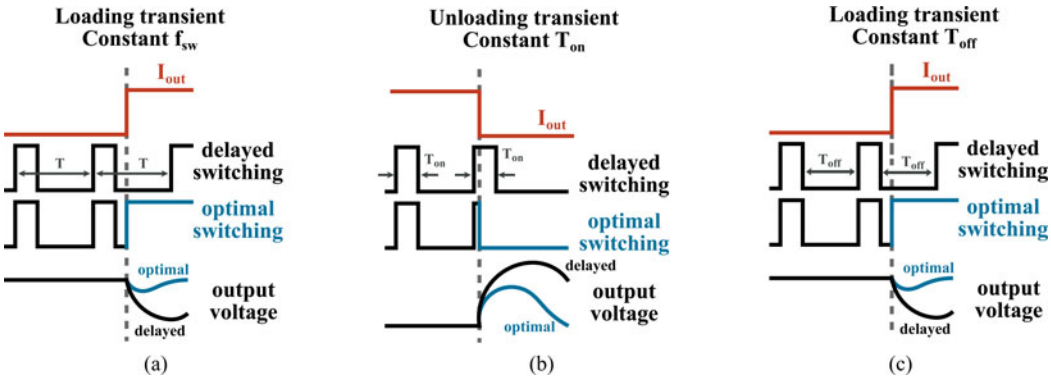

Fig. 5. Conceptual scheme of the delayed switching actions of different modulation techniques and comparison with the optimal switching action. (a) Delayed switching action of constant frequency modulation. (b) Delayed switching action of constant on-time modulation. (c) Delayed switching action of constant off-time modulation.

But these equations are derived assuming that the control is able to react instantaneously after the load transient. However, if constant on-time, constant off-time or constant switching frequency modulations are used, then, there are intrinsic delays that limit the effectiveness of the control. This is because there is an additional voltage deviation that is independent on how fast the control is.

Fig. 5 illustrates these delays and compares the response of the modulation with the optimal response:

1) In the case of constant frequency modulation [see Fig. 5(a)], this would be the case if a positive load step occurs during the off-state begins, as the control is not able to react until the end of the period. In order to overcome this problem, the clock needs to be synchronized with the load disturbance so that an on-time can occur just after the perturbation.

   In [16]–[19], different architectures with pseudo-constant frequency modulation based on a hysteretic modulation with an outer frequency loop are proposed. These architectures, in general, do not exhibit this worst-case transient. However, they have the disadvantage of uncontrolled switching frequencies under perturbations because the frequency loop is slow and takes some time to adjust the switching frequency again. This might affect electromagnetic interference sensitive applications. Also, they do not exhibit noise immunity, which can be achieved with a common pulse width modulation controller with a latch RS.
2) In the case of constant $T_{\rm on}$ modulations [see Fig. 5(b)], the control is not able to react until the end of the constant on-time if a negative load step occurs during the on-state. In order to overcome this problem, the generation of the constant on-time needs to be reset so that an off-time can occur just after the perturbation.
3) In the case of constant $T_{\rm off}$ modulations [see Fig. 5(c)], the control is not able to react until the end of the constant off-time if a positive load step occurs during the off-state. In order to overcome this problem, the generation of the constant off-time needs to be reset so that an on-time can occur just after the perturbation.
4) On the other hand, it is important to point out that ideal hysteretic modulations, which modulate with variable switching frequency, do not exhibit this problem as these modulations do not have time restrictions.

Therefore, for applications with small duty cycles, modulations with constant frequency and constant off-time can be preferable because the worst-case voltage deviation is, in general, smaller. This is because, for these modulations, the additional deviation increases the smaller voltage deviation, caused by the loading transient [see Figs. 5(a) and (c)]. On the other hand, the voltage deviation in modulations with constant on-time increases the larger voltage deviation, caused by the unloading transient [see Fig. 5(b)]. This is in contrast with [20], where a comparison of the small-signal characteristics of several modulations is carried out. In [20], a conclusion is that constant on-time can be preferable in applications with small duty cycles because a higher bandwidth can be achieved. Unfortunately, although the study is very valuable, it does not take into account large-signal behaviors and, therefore, the effect of the delayed switching actions of the modulations is not analyzed.

For a constant frequency control, without considering the ESR and the ESL of the output capacitor, the additional drop of the output voltage due to a time delay because of a positive load step is

$$\triangle V_{\rm delay} = \frac{1}{C}\left(\frac{1}{2}\frac{\triangle i_L}{T_{off}}t_d^2 - \frac{1}{2}\triangle i_L t_d + \triangle i_o t_d\right) \qquad (3)$$

where t_d is the time delay, $\triangle i_L$ is the ripple of the inductor current in steady-state, and $T_{\rm off}$ is the off-time in steady-state.

In the worst case, the control is unable to respond during the whole off-time. Then, $t_d = T_{\rm off}$ and the additional drop of the output voltage is

$$\triangle V_{\rm delay} = \frac{1}{C}\triangle i_o T_{\rm off}\,. \qquad (4)$$

Notice that the worst-case additional drop of the output voltage due to the delay does not depend on the inductor of the power stage.

As a result, for a Buck converter with constant frequency modulation, the minimum worst-case deviation of the output

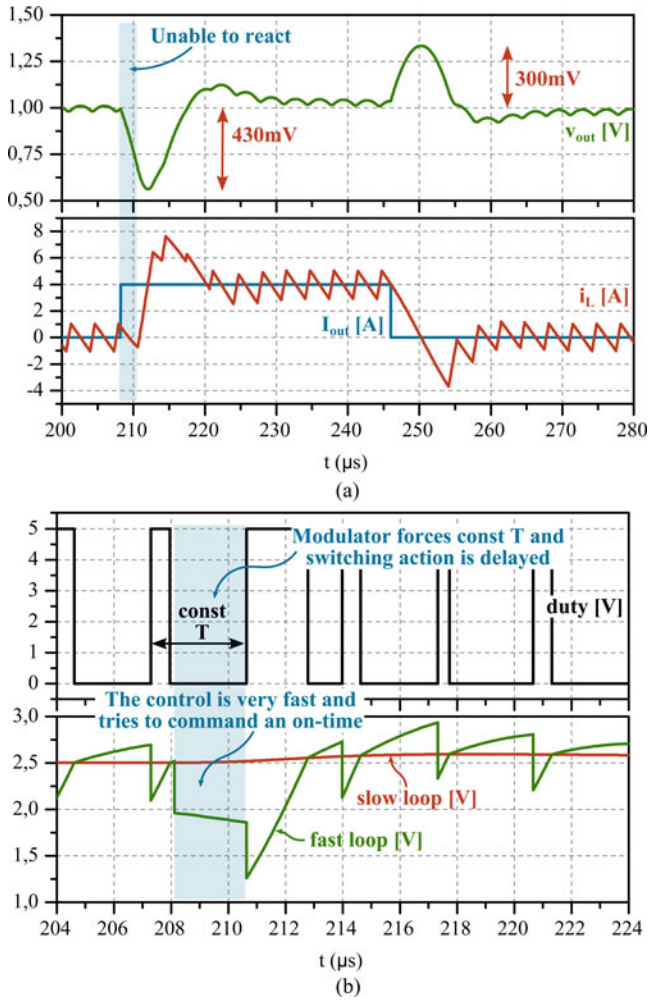

Fig. 6. Load transient response of V^2I_c control with constant frequency modulation. (a) Output voltage deviation under a loading and an unloading transient. (b) Control signals of the loading transient of (a). The slow loop signal and the fast loop signal that create the switching action are shown.

voltage under load transients is given by (5) for the loading case and (6) for the unloading case

$$\triangle v_{o,\text{loading}}^{\min} = \frac{1}{C}\cdot\left(\triangle i_o T_{\text{off}} + \frac{\triangle i_o^2}{2(V_{\text{in}}-v_o)}L\right) \quad (5)$$

$$\triangle v_{o,\text{unloading}}^{\min} = \frac{1}{C}\cdot\frac{\triangle i_o^2}{2v_o}L. \quad (6)$$

This equation is only an approximation that does not take into account the ESR and the ESL of the output capacitor.

Now, by studying (5) and (6), for small duty cycles and constant frequency modulation, the worst-case deviation of the output voltage could occur under the unloading transient.

Fig. 6 shows the worst-case load transients for positive load step and negative load step of a constant frequency V^2I_c peak control. First, notice that, for the unloading transient, the control commands a lengthy off-time so the deviation of the output voltage is the absolute minimum overshoot achievable for this power stage and it is 300 mV. On the other hand, when the positive load step occurs at the beginning of the off-state and the control is unable to react until the end of the period. When a new period starts, the control commands a lengthy on-time to recover from the drop of the output voltage. The drop of the output voltage for this loading transient is 430 mV. Fig. 6(b) shows, for the delayed load transient response of Fig. 6(a), the fast and the slow signals of the control that generate the switching action (in Fig. 1, the slow loop and fast loop signals correspond to the *ref* and the *control* signals that enter the modulator, respectively). Notice that the fast loop signal immediately drops below the slow loop signal when the load disturbance occurs so that control is trying to command an on-time just after the perturbation. But the switching action is delayed until the end of the period because the modulator is forcing a constant switching frequency.

Fig. 6 shows that V^2I_c control performs excellent and achieves the absolute minimum voltage deviation for the power stage and modulation. However, the larger drop is due to the constraint of the modulation, where the control is not able to command the power stage.

Therefore, the potential of the dynamic performance of very fast controls, such as V^2I_c, is obscured by the constraint of the modulation strategy.

III. Clock Pulse Synchronization Based on the Current Through the Output Capacitor (CPSI_c)

Fig. 6 showed that the worst-case load transient of a constant frequency control is when a positive load step occurs at the beginning of the off-state as the control is forced to wait the whole off-state for the clock signal to rise. This causes an additional drop of the output voltage due to the delay in the control response that could be prevented if the next on-time is allowed to begin before finishing the period.

In [21], a technique is described where the clock of the control is reset when there is a change in the operating conditions to improve the dynamic response. The triggering signal for the clock synchronization is the output of the linear controller. However, in ripple-based controllers, the bandwidth of the linear controller is usually low because there is a fast loop that takes the control effort. As a consequence, in common ripple-based controls it is not possible to use the output of the linear controller as the triggering signal. A particular case is a ripple-based control with single feedback path [22], where the linear controller may have a high bandwidth. This technique is used in [23], where the output of the linear controller is used to modulate the ramp in a constant on-time V^2 control with single feedback path. However, as said, this is not applicable in common ripple-based controls. In [24], the ramp is modulated with the output voltage to improve the transient response of a voltage mode control. As the output voltage changes with a limited slope, the response of the control still presents some delay.

This article proposes a technique called "**C**lock **P**ulse **S**ynchronization" based on the current through the output capacitor (CPSI_c).

A. Description of Proposed Technique

Fig. 7 shows the scheme of the CPSI_c technique applied to the V^2I_c control. CPSI_c improves the dynamic response of the control by using the current through the output capacitor as

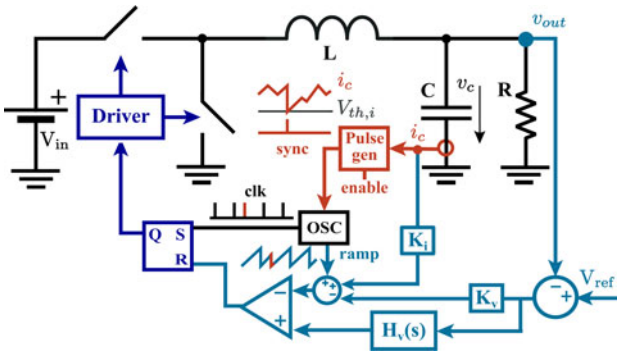

Fig. 7. Proposed clock pulse synchronization technique (in red) on a V^2I_c control.

the triggering signal to synchronize the clock. It provides the control with an instant reaction to the load step as a change in the load current immediately modifies the current through the output capacitor. As V^2I_c control already measures the current through the output capacitor, V^2I_c seems the most appropriate control to use with this technique.

Fig. 8(a) shows a loading transient response of a constant frequency control without $\mathrm{CPSI_c}$. When the loading occurs at the off-time, the control cannot react till the end of the period and, consequently, the drop of the output voltage is very large ($\triangle v_{\mathrm{out}} = 350\,\mathrm{mV}$). Fig. 8(b) shows the very same control and the same loading transient response but including the proposed $\mathrm{CPSI_c}$. When the loading occurs, the current through the output capacitor instantly drops which triggers a pulse that resets the clock of the control and the next on-time begins right after the load transient. In the figure, $V_{\mathrm{th},i}$ is the threshold voltage of the measurement of the current through the output capacitor to trigger the clock synchronization. With $\mathrm{CPSI_c}$, the control is able to react without delay and the drop of the output voltage is dramatically reduced (98% of reduction). Notice that, in both cases, V^2I_c reacts optimally achieving the absolute minimum deviation of the output voltage and that the additional drop is caused by the constraint of the modulation. Note also that $\mathrm{CPSI_c}$ only changes during one period the switching frequency. When the clock is synchronized, the converter returns to switch at the nominal frequency.

If the loading disturbance is equal or smaller than the ripple of the capacitor current, the sudden change of the output current is poorly reflected on the current through the output capacitor. Since the threshold has to be larger than the maximum capacitor current ripple, the clock synchronization would be triggered with a certain delay or even not triggered at all. Fig. 9 shows a case with the same converter of Fig. 8 where a positive load step of 2A does not immediately trigger the clock synchronization. Consequently, the control is unable to respond to the perturbation during a certain time. The current through the output capacitor continues to drop with a slope equal to the slope of the inductor current and finally triggers the clock synchronization. The drop of the output voltage is small, even though there is a delay in the response of the control, because the additional drop is proportional to the load step.

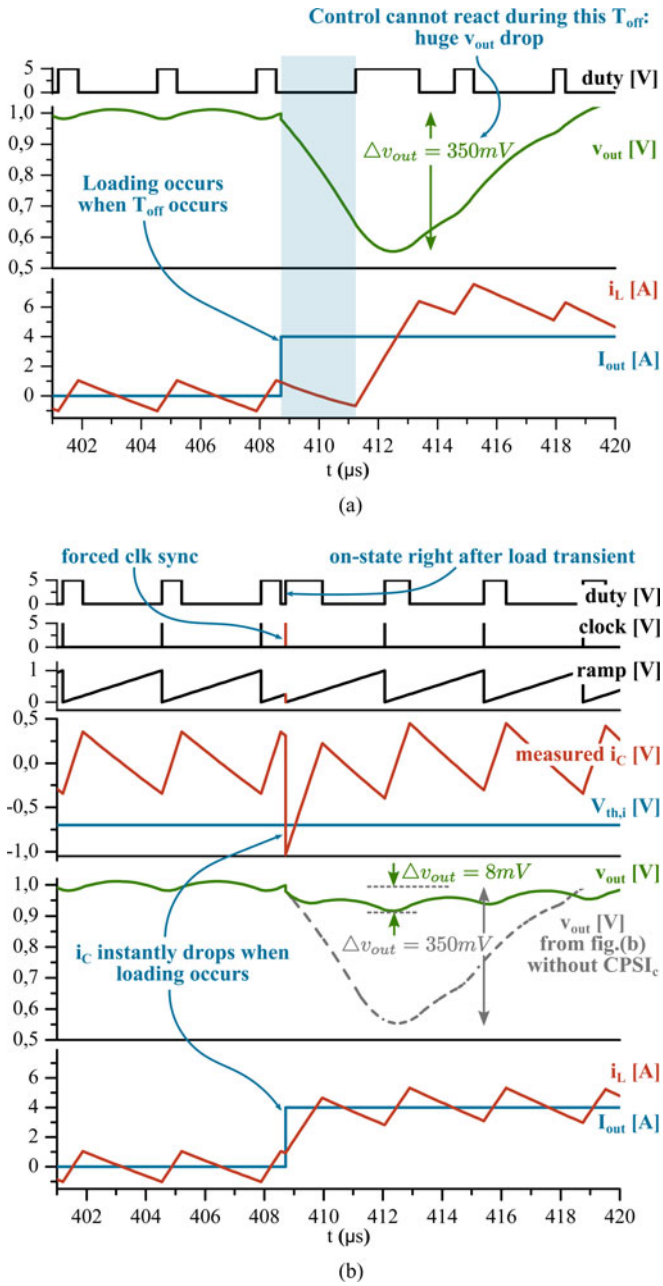

Fig. 8. Loading transient response of the same converter modulated with constant switching frequency (a) without including and (b) including $\mathrm{CPSI_c}$. (a) Loading transient response without including $\mathrm{CPSI_c}$ in the control. (b) Loading transient response including $\mathrm{CPSI_c}$ in the control.

For applications with reference voltage tracking, the current through the output capacitor also changes when a negative reference voltage step occurs. This variation is a consequence of the decrease of the inductor current to discharge the output voltage. Fig. 10(a) shows the dynamic behavior of a V^2I_c control with $\mathrm{CPSI_c}$ working. The control reduces the output voltage by commanding a large off-state. Unfortunately, this causes the current through the output capacitor to drop below the threshold and to synchronize the clock. As a consequence, the control continuously tries to enter an off-state while $\mathrm{CPSI_c}$ tries to enter an on-state. This causes an undesirable very high frequency switching.

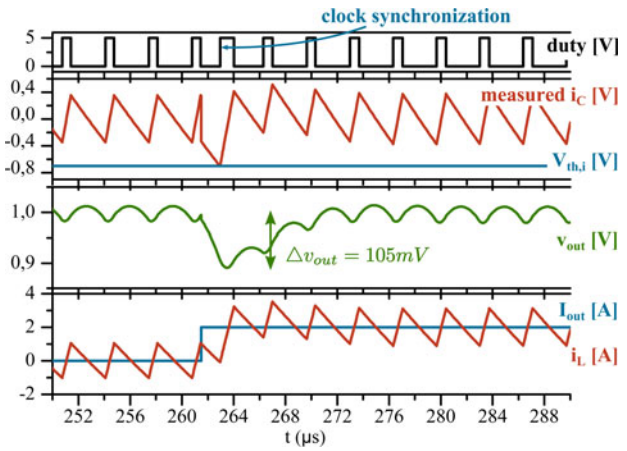

Fig. 9. Loading transient response including $\mathrm{CPSI_c}$ in the control but the clock synchronization is triggered with a delay.

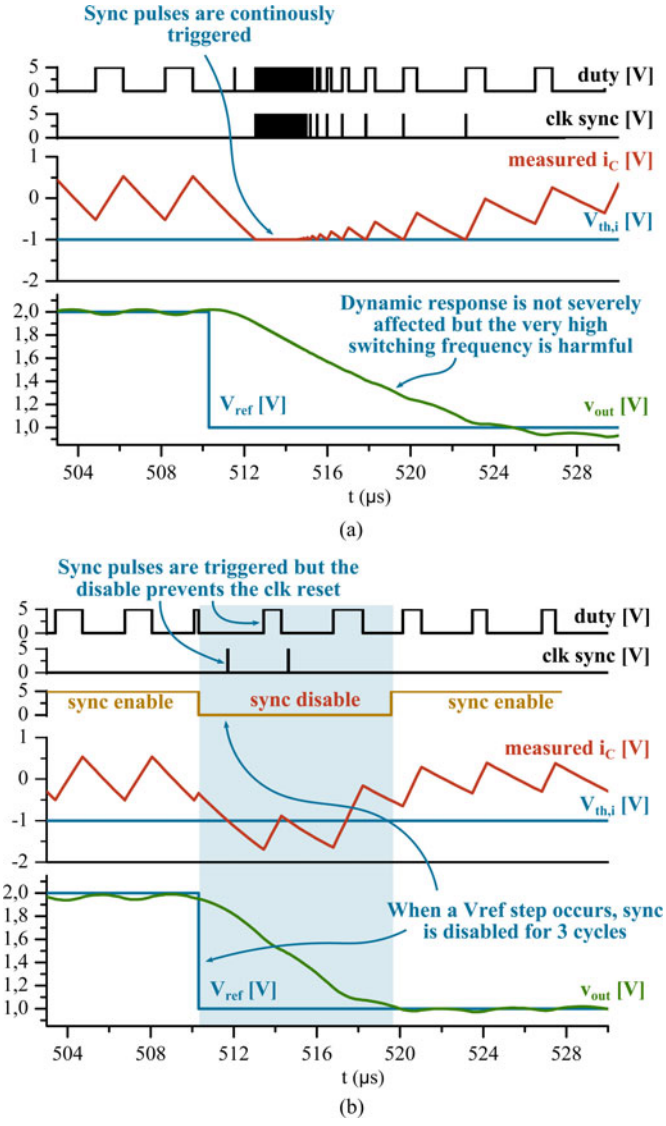

Fig. 10. $\mathrm{CPSI_c}$ is disabled when a reference voltage step occurs. (a) Dynamic response under a negative reference voltage step without disabling $\mathrm{CPSI_c}$. (b) Dynamic response under a negative reference voltage step disabling $\mathrm{CPSI_c}$ during the transient.

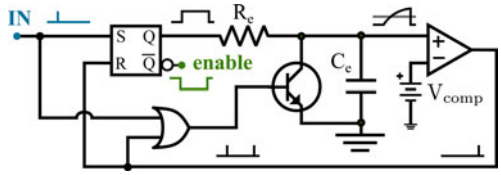

Fig. 11. Circuit scheme to enable/disable the clock pulse synchronization.

In order to overcome this problem in applications with reference voltage tracking, the load could disable $\mathrm{CPSI_c}$ at the same time that it changes the reference voltage. However, this paper proposes also an optional "disable block" that prevents the reset of the clock when this is not desirable. Fig. 11 shows the electrical scheme of the enable signal of the $\mathrm{CPSI_c}$. When there is a pulse in the input, indicating that a reference voltage step has occurred, the enable signal is set to 0 during a certain time. This disable time is defined with R_e, C_e and V_{comp}. R_e and C_e set the time constant of a ramp and V_{comp} set the threshold that is compared with the ramp to enable again $\mathrm{CPSI_c}$. Section III-D provides the design guidelines of these parameters.

Fig. 10(b) shows the response of the converter including $\mathrm{CPSI_c}$ in the control under a negative reference voltage step when the optional disable signal is introduced. The change in the reference voltage is detected and the $\mathrm{CPSI_c}$ block is disabled for three cycles by setting the enable signal to zero. This prevents $\mathrm{CPSI_c}$ from resetting the clock as it would be counterproductive. If reference voltage tracking is not a requirement, then this disable option is not necessary.

B. Alternative Scheme: Derivative of the Capacitor Current as the Triggering Signal

As shown previously, the use of the current through the output capacitor as the triggering signal to reset the clock has two issues:

1) load steps lower than the peak-to-peak current ripple cannot be detected;
2) in applications with reference voltage tracking, $\mathrm{CPSI_c}$ needs to be disabled when the reference voltage step occurs.

Although these issues are not critical, they can be solved by employing the derivative of the current through the output capacitor as the triggering signal to reset the clock.

Fig. 12 shows the proposed scheme of $\mathrm{CPSI_c}$ using the derivative of the current through the output capacitor. The derivative is done by means of a high-pass filter which is composed by a zero at origin and a pole. By placing the pole appropriately, the filter has a derivative action up to the frequency of the pole, that derivates the current ripple, and a proportional action at higher frequencies, that only applies a gain to the sudden change of the capacitor current. The selection of the frequency of the pole is not straightforward and tuning based on simulations is needed. In general, it needs to be higher than the switching frequency but not too high to avoid a severe attenuation of the change of the capacitor current due to the load step.

Fig. 13 shows the transient responses of $\mathrm{CPSI_c}$ with the derivative of the current through the output capacitor as the

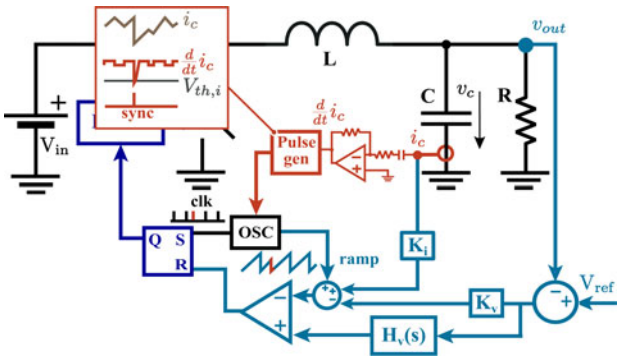

Fig. 12. Proposed clock pulse synchronization technique (in red) on a $V^2 I_c$ control using the derivative of the current through the output capacitor.

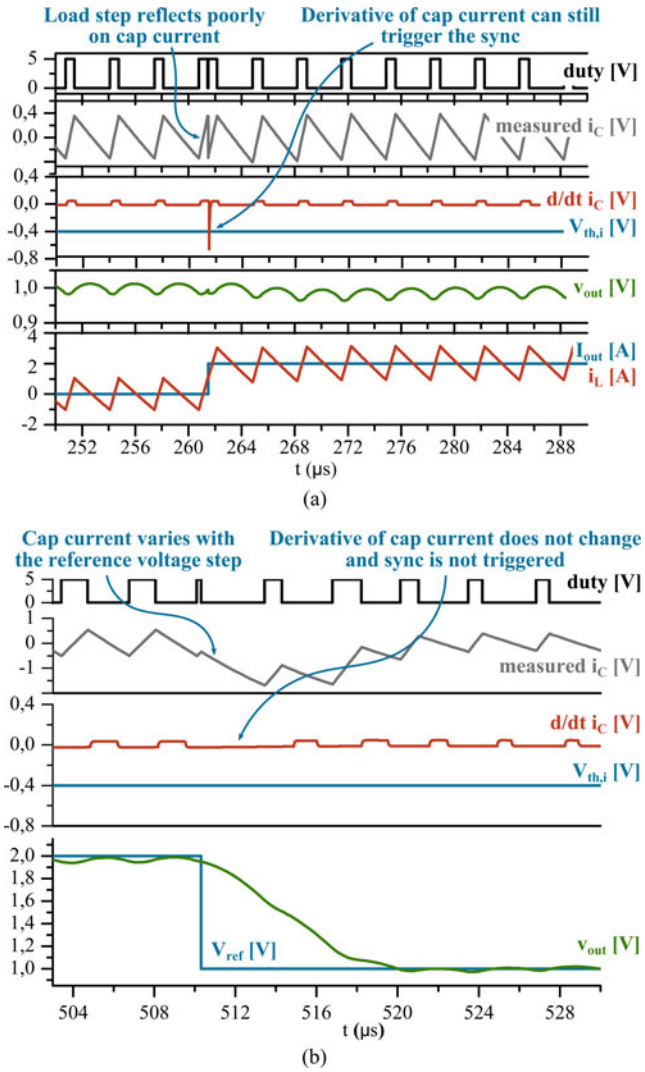

Fig. 13. Transient responses using $\mathrm{CPSI_c}$ with the derivative of the current through the output capacitor as the triggering signal. (a) Transient response under the same light load step as Fig. 9. (b) Transient response under the same negative reference voltage step as Fig. 10.

triggering signal. The frequency of the pole of the high-pass filter is $f_p = 12 f_{sw}$. Fig. 13(a) shows that, even when the load step is small, $\mathrm{CPSI_c}$ is triggered. Fig. 13(b) shows that, with this alternative scheme, $\mathrm{CPSI_c}$ is not triggered when a negative reference voltage step occurs and, consequently, the disable is not needed.

Therefore, it has been validated that the use of the derivative of the current through the output capacitor as the triggering signal instead of the own current solves the two issues of $\mathrm{CPSI_c}$. However, the high-pass filter needs to be carefully designed so that it attenuates sufficiently the ripple of the current but not the sudden change under a load disturbance that is used to trigger the synchronization. Furthermore, in a real-world implementation, the operation amplifier of the high-pass filter needs to be sufficiently fast to handle the large slew rate in the derivative of the current when the load transient occurs.

C. Improvement in the Load Transient Response for Constant Frequency Modulation

In order to design power converters within dynamic requirements, both the deviations of the output voltage under the worst-case positive load disturbance and the worst-case negative load disturbance have to be analyzed. In constant frequency modulation, the overshoot of the output voltage under a negative load disturbance remains the same with and without $\mathrm{CPSI_c}$ because there is no delay. As $V^2 I_c$ reacts very fast, this voltage deviation depends only on the power stage and cannot be reduced. On the other hand, for constant frequency modulation, the drop of the output voltage under a positive load disturbance heavily depends on the constraint of the modulation. Consequently, depending on whether the additional drop of the output voltage is dominant or not, the worst-case deviation of the output voltage can occur under the positive load disturbance or the negative load disturbance.

Equations (5) and (6) showed the minimum deviation for the output voltage for a loading and an unloading transient. By analyzing the equations, it can be concluded that:

1) the capacitance of the output capacitor affects the same way to the contributions of both deviations of the output voltage: due to the load disturbance and the additional drop due to the delay in the response;
2) the lower the inductance, the lower the voltage deviation due to load disturbances. But the additional voltage drop due to the delay in the response remains the same independently of the inductance.

Therefore, converters with low inductance are greater benefited from using $\mathrm{CPSI_c}$ because, for these cases, the additional drop of the output voltage due to the delay is dominant. This is very interesting for the case of high-frequency integrated converters. These converters have a low inductance for integration purposes. Fig. 14 shows a comparison of the minimum required output capacitor needed to comply with the requirements of a specific high-frequency converter. The parameters of the converter are $f_{sw} = 10\,\mathrm{MHz}$, $V_{\mathrm{in}} = 5\,\mathrm{V}$, $v_{\mathrm{out}} = 1.2\,\mathrm{V}$, $i_{\mathrm{out}} = 0\,\mathrm{A} \sim 1\,\mathrm{A}$, $L = 100\,n\mathrm{H}$. The maximum allowed static ripple of the output voltage is $v_{\mathrm{out}} \pm 30\,\mathrm{mV}$ and the maximum allowed voltage deviation during a transient is $v_{\mathrm{out}} \pm 100\,\mathrm{mV}$. Fig. 14(a) shows the unloading and the loading transient of $V^2 I_c$ control without including $\mathrm{CPSI_c}$. When $C = 1.1\,\mu\mathrm{H}$, the output voltage just reaches the lower dynamic limit under the loading,

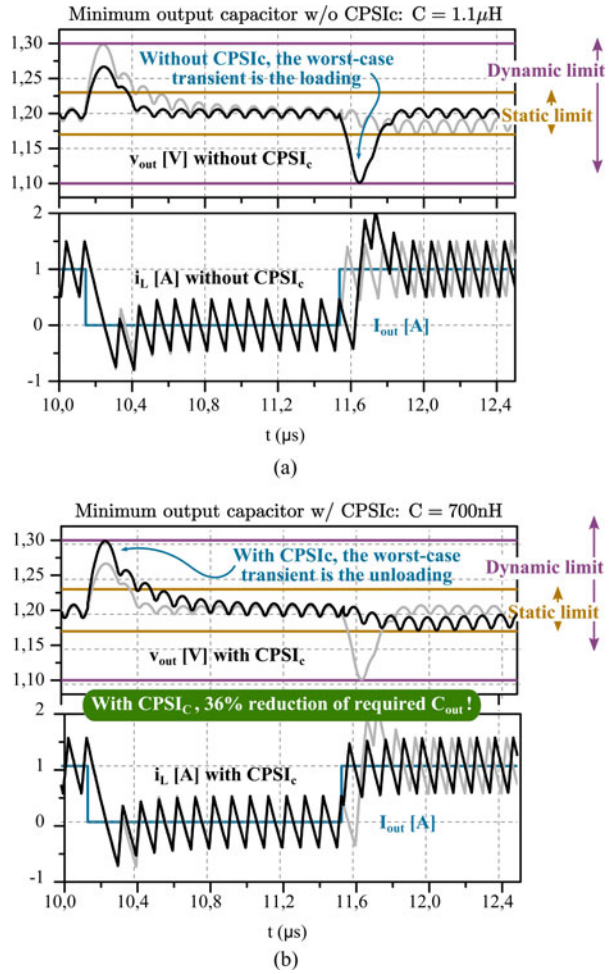

Fig. 14. Comparison of the minimum required output capacitance to comply with requirements without including and including $\mathrm{CPSI_c}$. The load steps are from full load (1 A) to no load (0 A) and vice versa. (a) Without including $\mathrm{CPSI_c}$, the minimum required output capacitance is $1.1\,\mu$H (highlighted in black). The response including $\mathrm{CPSI_c}$ and $\mathrm{C} = 700\,n$H is in the background in grey. (b) Including $\mathrm{CPSI_c}$, the minimum required output capacitance is $700\,n$H (highlighted in black). The response without including $\mathrm{CPSI_c}$ and $\mathrm{C} = 1.1\,\mu$H is in the background in gray.

so this is the minimum required output capacitance. Fig. 14(b) shows the unloading and the loading transient of V^2I_c control including $\mathrm{CPSI_c}$. Now, when $C = 700\,n$H, the output voltage just reaches the upper dynamic limit under the unloading. This means that, when $\mathrm{CPSI_c}$ is included in the control, the required output capacitance can be reduced by a 36%, in this specific example.

In order to study how much reduction of the maximum deviation can be achieved, let us suppose that, when $\mathrm{CPSI_c}$ is not included in the control, the worst-case load transient is the loading transient. Then the worst-case voltage deviation, $\triangle V^{\mathrm{worst}}$, is

$$\triangle V^{\mathrm{worst}}_{w/o\mathrm{CPSIc}} = \triangle v^{\mathrm{min}}_{o,\,\mathrm{loading}} = \frac{1}{C}\cdot\left(\triangle i_o T_{\mathrm{off}} + \frac{\triangle i_o^2}{2(V_{in}-v_o)}L\right). \tag{7}$$

If $\mathrm{CPSI_c}$ is included, then the worst-case load transient for small duty cycles is the unloading transient

$$\triangle V^{\mathrm{worst}}_{w/\mathrm{CPSIc}} = \triangle v^{\mathrm{min}}_{o,\,\mathrm{unloading}} = \frac{1}{C}\cdot\frac{\triangle i_o^2}{2v_o}L. \tag{8}$$

Consequently, the percentage of reduction of the worst-case voltage deviation when $\mathrm{CPSI_c}$ is included is

$$\frac{\triangle V^{\mathrm{worst}}_{w/o\mathrm{CPSIc}}}{\triangle V^{\mathrm{worst}}_{w/\mathrm{CPSIc}}} = \frac{(1-d)v_oT}{\triangle i_oL} + \frac{1}{2}\frac{d}{1-d}. \tag{9}$$

Equation (9) can be used to estimate roughly how much improvement can be obtained by including $\mathrm{CPSI_c}$ in a control with constant frequency modulation. The higher the percentage, the more improvement is obtained. If the percentage of reduction is lower than the unity, then, the worst-case load transient is always the unloading transient. For these cases, $\mathrm{CPSI_c}$ does not offer an improvement in the reduction of the deviation of the output voltage. This equation does not take into account other phenomena that affect the deviation of the output voltage. For example, in general, a step-down load transient at the beginning of the off-time causes the largest deviation of the output voltage [25]. This is because, at that time instant, the energy stored in the inductor is at its peak and delivers a larger excess of energy to the capacitor. Consequently, in order to deeply study the benefit of using $\mathrm{CPSI_c}$, simulations need to be carried out.

Fig. 15 shows the dynamic behavior of V^2I_c under the worst-case load transients without including and including $\mathrm{CPSI_c}$ for different values of L. The load steps are from full load (4 A) to no load (0 A) and vice versa, taking into account that the unloading transient needs to occur at the beginning of the off-time so that worst-case deviation of the output voltage is obtained. The nominal parameters of the Buck converter are detailed as follows: $f_{sw} = 300\,\mathrm{kHz}$, $V_{\mathrm{in}} = 5\,\mathrm{V}$, $v_{\mathrm{out}} = 1\,\mathrm{V}$, $i_o = 4\,\mathrm{A}$, $L = 1.3\,\mu\mathrm{H}$, $C = 30\,\mu\mathrm{F}$, $\mathrm{ESR} = 4.4\,m\Omega$, $\mathrm{ESL} = 650\,p\mathrm{H}$, $K_i = 0.13\Omega$, $K_v = 1$, $V^{pk-pk}_{\mathrm{ramp}} = 0.6\,\mathrm{V}$, $H_v(s) = 38400/s$. The control is designed for an inductance of $L = 1.3\,\mu$H.

It is important to point out that the parameters of the control, designed for $L = 1.3\,\mu$H, remain the same for the different values of L. Notice that, even if the power stage varies, the control still offers an optimal performance, achieving the absolute minimum deviation of the output voltage in all three cases. This robustness of the dynamic response under variations of the power stage is one of the properties of the V^2I_c control.

Fig. 15(a) shows the load transients for $L = 600\,\mathrm{nH}$. Without including $\mathrm{CPSI_c}$, the additional drop of the output voltage due to the delay in the control is dominant. The drop under the loading transient is $400\,\mathrm{mV}$, while the output voltage deviation under an unloading transient is $296\,\mathrm{mV}$. When $\mathrm{CPSI_c}$ is included, the drop of the output voltage under the loading transient is dramatically reduced to $10\,\mathrm{mV}$. As a result, by including $\mathrm{CPSI_c}$, the worst-case deviation of the output voltage is reduced from $400\,\mathrm{mV}$ (loading transient without $\mathrm{CPSI_c}$) to $296\,\mathrm{mV}$ (unloading transient).

Fig. 15(b) shows the load transients for $L = 1.3\,\mu$H. Without including $\mathrm{CPSI_c}$, the additional drop of the output voltage due to the delay in the control is still dominant, albeit it is not much larger than the output voltage deviation in the

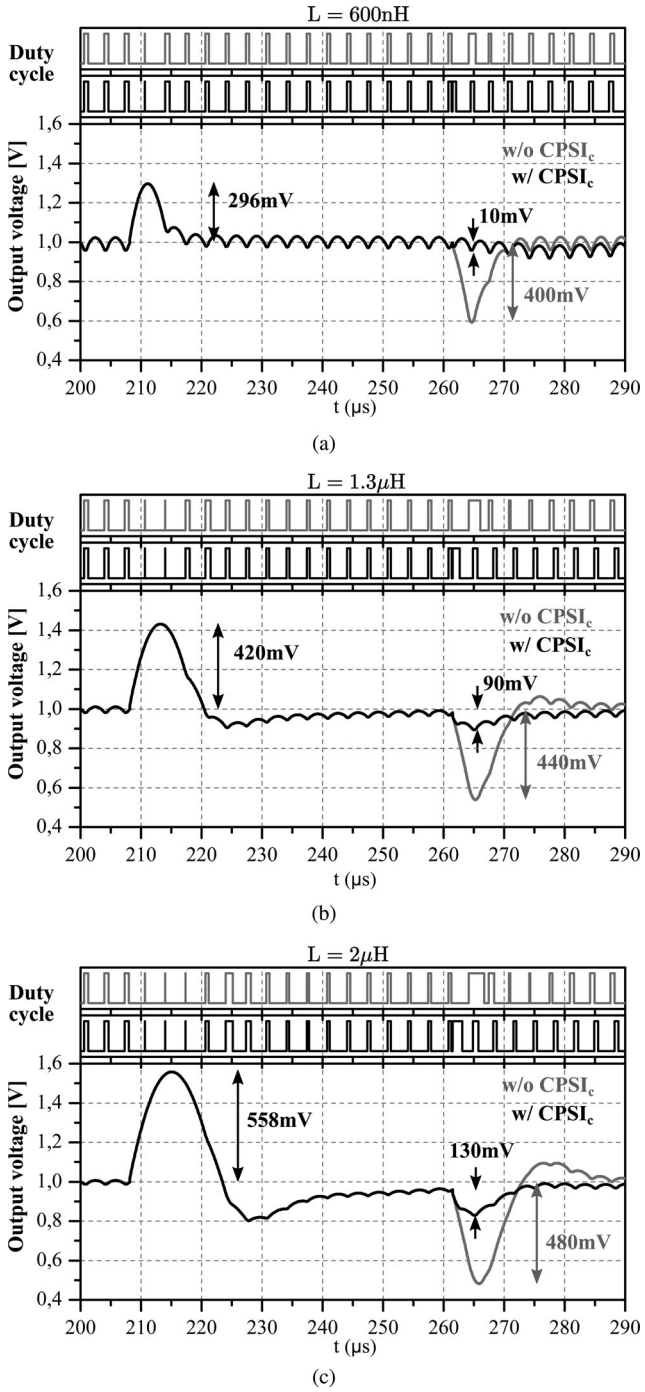

Fig. 15. Worst-case loading transient response of a 300 kHz Buck converter with V^2I_c without including and including $\mathrm{CPSI_c}$ for different values of inductance. The load steps are from full load (4 A) to no load (0 A) and vice versa.

worst-case unloading transients. For the loading transient, the drop is reduced from 440 to 90 mV when $\mathrm{CPSI_c}$ is included. For the unloading transient, the voltage deviation is 420 mV. As a result, by including $\mathrm{CPSI_c}$, the worst-case deviation of the output voltage is reduced from 440 (loading transient without $\mathrm{CPSI_c}$) to 420 mV (unloading transient).

Fig. 15(c) shows the load transients for $L = 2\,\mu$H. When $\mathrm{CPSI_c}$ is included, the drop of the output voltage under the loading transient is reduced from 480 to 130 mV. The output voltage deviation under the unloading transient is 558 mV. As a result, the worst-case deviation of the output voltage is not reduced by using $\mathrm{CPSI_c}$.

TABLE I
REDUCTION OF THE MAXIMUM DEVIATION OF THE OUTPUT VOLTAGE UNDER 4 A LOAD TRANSIENTS ($i_{\mathrm{out}} = 0A \rightarrow 4A$, $i_{\mathrm{out}} = 4\mathrm{A} \rightarrow 0\mathrm{A}$) FOR DIFFERENT VALUES OF INDUCTANCE

Inductance	$\triangle v_{out}^{worst}$ w/o CPSIc	$\triangle v_{out}^{worst}$ w/ CPSIc	$\triangle v_{out}^{worst}$ reduction
$L = 600nH$	$400mV(i_o = 0A \rightarrow 4A)$	$296mV(i_o = 4A \rightarrow 0A)$	26%
$L = 1.3\mu H$	$440mV(i_o = 0A \rightarrow 4A)$	$420mV(i_o = 4A \rightarrow 0A)$	5%
$L = 2\mu H$	$558mV(i_o = 4A \rightarrow 0A)$	$558mV(i_o = 4A \rightarrow 0A)$	0%

Notice in Fig. 15 that, when $\mathrm{CPSI_c}$ is not included, the worst-case voltage deviation occurs under the loading transient due to the delay in the response. When $\mathrm{CPSI_c}$ is included, the voltage deviation under the loading transient is severely reduced and, therefore, the worst-case voltage deviation occurs under the unloading transient. Table I shows a summary of the improvement in the dynamic response for different values of inductance when $\mathrm{CPSI_c}$ is included. It compares the worst-case voltage deviation, $\triangle v_{\mathrm{out}}^{\mathrm{worst}}$, without including and including $\mathrm{CPSI_c}$. It is important to recall that for each case of the comparison, V^2I_c achieves the absolute minimum output voltage deviation both under loading and unloading transients. The table shows that $\mathrm{CPSI_c}$ is more useful when a low inductance is used in the power stage. This is because the lower the inductance, the more dominant is the additional drop of the output voltage due to the delay in the response. For this specific example under load transients of 4 A, if an inductance of $L = 600\,n$H, a reduction of 26% on the maximum deviation of the output voltage can be achieved by using $\mathrm{CPSI_c}$.

D. Design Guidelines

This subsection provides design guidelines about how to apply the $\mathrm{CPSI_c}$ technique in an application with reference voltage tracking. It can be added to an already-designed control to enhance it without perturbing it as $\mathrm{CPSI_c}$ does not affect the dynamic behavior of the control but only improves its response by allowing the switching actions to occur without delay.

1) Description of the System: Fig. 16 shows a detailed scheme of the Buck converter controlled with constant frequency V^2I_c peak control including $\mathrm{CPSI_c}$. The different parts of the scheme are:

1) The V^2I_c control (in the blue area) uses the error of the output voltage, the current through the output capacitor and an artificial ramp generated from the oscillator.
2) The clock and ramp generation (in the gray area) are shown in a simplified scheme where they are generated using a current source. Notice that, because of the OR gate, the ramp and the clock can be synchronized by an external source.
3) The $\mathrm{CPSI_c}$ block (in the red area) generates the pulses that synchronize the clock when needed. In this example, both a decrease of the current through the output capacitor as

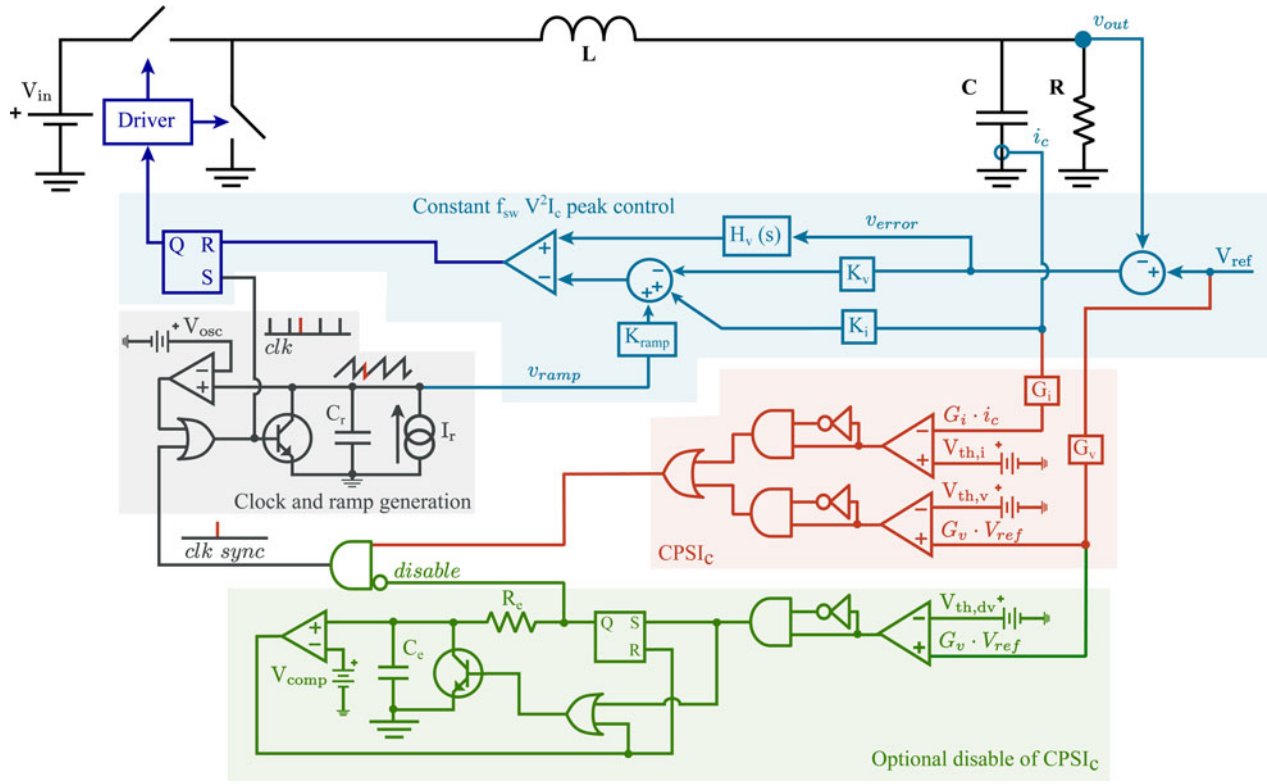

Fig. 16. Detailed scheme of a Buck converter with $V^2 I_c$ control and $\mathrm{CPSI_c}$ technique.

an increase of the reference voltage step can synchronize the clock. This is because, in reference voltage tracking applications, the two scenarios when an immediate on-time is needed are when the system is under a positive load disturbance or under a positive reference voltage step. The current through the output capacitor is monitored with a gain G_i and the reference voltage is monitored with a gain G_v. When the weighted current through the output capacitor decreases below $V_{\mathrm{th},i}$, a pulse is generated that forces the synchronization of the clock. The same applies to the weighted reference voltage when it rises over $V_{\mathrm{th},v}$.

4) The optional disable of $\mathrm{CPSI_c}$ (in the green area) is also included. For this module, when the weighted reference voltage decreases below $V_{\mathrm{th},dv}$, $\mathrm{CPSI_c}$ is disabled during a certain time.

This control scheme can be easily generated with commercial PWM controllers that have the option of external clock synchronization. Specifically, this paper uses in the experimental validation the PWM controller UC3823 from Texas Instruments [26]. Notice that, if the reference voltage remains constant in the application, neither the disable of $\mathrm{CPSI_c}$ nor the monitoring of the reference voltage are needed. Consequently, if no reference voltage tracking is required, the $\mathrm{CPSI_c}$ block only requires one comparator, one inverter logic gate, and one nand logic gate.

In order to design the $\mathrm{CPSI_c}$ scheme shown in Fig. 16, several parameters have to be taken into account for an optimal behavior. The design parameters are: the threshold values that trigger the pulses, the disable time of $\mathrm{CPSI_c}$ and the width of the pulse that synchronizes the clock.

2) Threshold values: The threshold values $V_{\mathrm{th},i}$, $V_{\mathrm{th},v}$, and $V_{\mathrm{th},dv}$ are defined as follows:

1) $V_{\mathrm{th},i}$ is the threshold value of the weighted current through the output capacitor $G_i \cdot i_c$. On one hand, the threshold needs to be below the minimum value of the weighted current through the output capacitor over the operating region. On the other hand, the threshold needs to be sufficiently high so that the most aggressive load steps trigger the clock synchronization. In general, it is preferable to define the threshold as close as possible to the weighted current. Consequently, by analyzing the topology, the threshold $V_{\mathrm{th},i}$ needs to be in the range of

$$-G_i \triangle i_o^{\max} + G_i \frac{\triangle I_{Cpk,pk}^{\max}}{2} < V_{\mathrm{th},i} \lesssim -G_i \frac{\triangle I_{Cpk,pk}^{\max}}{2} \tag{10}$$

where $\triangle I_o$ is the worst-case load step and $\triangle I_{Cpk,pk}^{\max}$ is the maximum current ripple over the operation region.

It is important to point out that the sensor measures the capacitor current by matching the time constant of the output capacitor [5]. Consequently, variations of the output capacitance due to aging, temperature or dc bias may cause a distorted measurement of the current through the output capacitor. The sudden change of the current due to a load disturbance will be still present but the current ripple might be greater than expected. For this reason, the maximum current ripple over the operation region, $\triangle I_{Cpk,pk}^{\max}$, must include also the effect of a distorted measurement because of tolerances of the output capacitor.

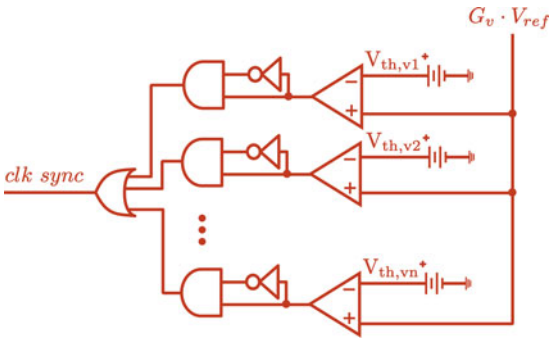

Fig. 17. Clock pulse generation for application with reference voltage tracking of several voltage levels.

Notice that, if the alternative method of the derivative of the capacitor current as the triggering signal is used, the detection of the load step is less sensitive to the measurement of the capacitor current. This is because the ripple is filtered and, therefore, the effect of a distorted measurement is mitigated.

2) $V_{\mathrm{th},v}$ and $V_{\mathrm{th},dv}$ are the threshold values of the weighted reference voltage to trigger the clock synchronization and to disable $\mathrm{CPSI_c}$, respectively. Both threshold values are placed in the middle of the reference voltage step

$$V_{\mathrm{th},v} = V_{\mathrm{th},dv} = G_v \frac{\triangle V_{\mathrm{ref}}}{2}. \tag{11}$$

Notice that, if more voltage levels are required, then more blocks can be added in $\mathrm{CPSI_c}$ to trigger a pulse in each reference voltage step (see Fig. 17).

3) Disable of $\mathrm{CPSI_c}$*:* The disable time (12) is defined with R_e, C_e, and V_{comp}

$$t_{\mathrm{disable}} = R_e C_e \ln \frac{V^+}{V^+ - V_{\mathrm{comp}}} \tag{12}$$

where V^+ is the high output voltage value of the latch RS.

The disable time is designed to be equal to the settling time of the control under the most aggressive negative reference voltage step. For the $V^2 I_c$ control, the settling time is typically about a few clock cycles.

4) Width of Clock Pulse Synchronization: The width of the clock pulse synchronization is equal to the propagation delay of the inverters that are part of the clock pulses generation. The width needs to be sufficiently large so that it completely discharges the capacitor C_r that generates the ramp. For the PWM controller UC3823 [26], the clock pulse synchronization requires a minimum width of 10 ns. If needed, inverters can be placed in series to increase the propagation delay and achieve the target pulse width.

IV. Experimental Validation

This section documents the experimental validation of $\mathrm{CPSI_c}$ on a 300 kHz Buck converter with $V^2 I_c$ control. The parameters of the control are the same as in Fig. 15. The PWM controller UC3823 [26] is used to modulate the $V^2 I_c$ control with constant frequency. This PWM controller allows the external synchronization of the clock signal.

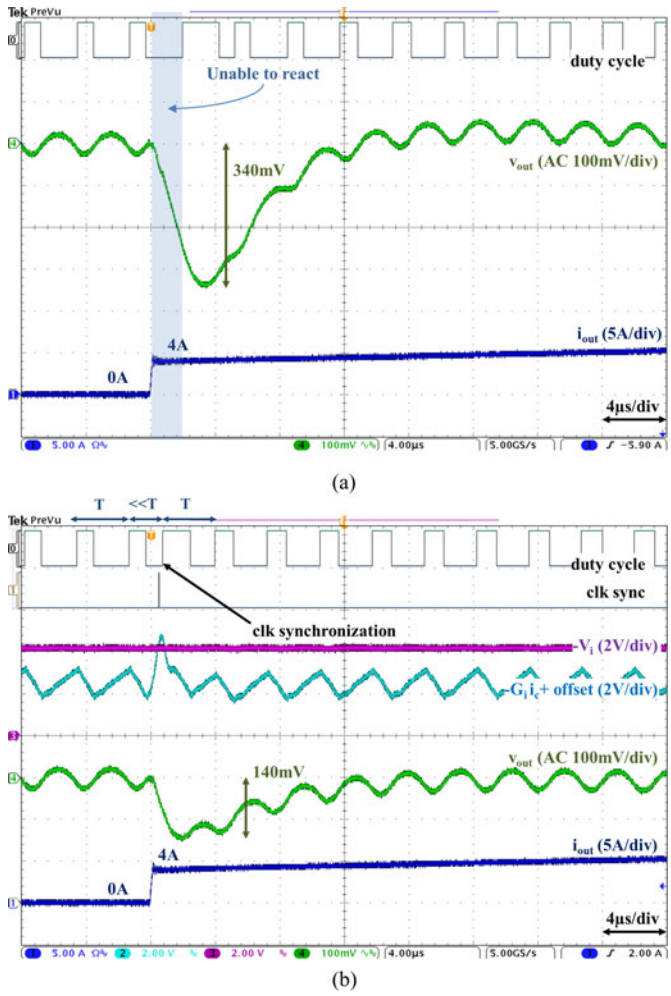

Fig. 18. Experimental validation of $\mathrm{CPSI_c}$ on a 300 kHz Buck converter with $V^2 I_c$ control. Output voltage in green, output current in blue, measurement of the current through the output capacitor in light blue, comparator signal in purple, synchronization pulse (lower digital signal), and duty cycle (upper digital signal) in black. (a) Load step 0 to 4 A without including $\mathrm{CPSI_c}$ in the control. (b) Load step 0 to 4 A including $\mathrm{CPSI_c}$ in the control.

Fig. 18 shows the experimental validation of $\mathrm{CPSI_c}$. When a positive load step from 0 to 4 A occurs in the off-time, the drop of the output voltage is 340 mV [see Fig. 18(a)]. When the same load transient occurs at the same instant of the off-time but including $\mathrm{CPSI_c}$, the drop of the output voltage is 140 mV [see Fig. 18(b)], achieving a 58% reduction. Notice that the measurement of the current through the output capacitor [in light blue in Fig. 18(b)] is inverted as the implemented current sensor inverts the measurement. Notice that the reduction of the drop of the output voltage is not as dramatic as previously shown in simulations. This is because there is still a certain delay in the response due to the implementation of $\mathrm{CPSI_c}$ with discrete components. For example, notice that there is some delay between the pulse that synchronizes the clock and the actual synchronization of the clock. This delay would be reduced if $\mathrm{CPSI_c}$ is integrated in the PWM controller.

Fig. 19 shows the experimental validation of the disable of $\mathrm{CPSI_c}$. It shows that, when the reference voltage step occurs,

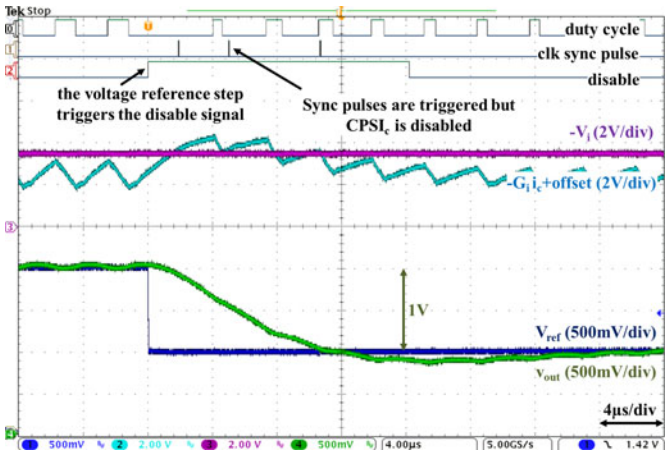

Fig. 19. Experimental validation of the disable of CPSI$_c$ when a negative reference voltage step occurs. Output voltage in green, output current in blue, measurement of the current through the output capacitor in light blue, comparator signal in purple, disable signal (lower digital signal), clock synchronization pulse (middle digital signal), and duty cycle (upper digital signal) in black.

a signal is generated that disable CPSI$_c$ for six clock cycles. During the transient, the current through the output capacitor surpasses the threshold and clock synchronization pulses are triggered. But as CPSI$_c$ is disabled during the transient, the clock is not synchronized.

Fig. 20 shows the experimental validation of the alternative scheme of CPSI$_c$ where the derivative of the current through the output capacitor is the triggering signal. The frequency of the pole of the high-pass filter is $f_p = 12 f_{sw}$. Fig. 20(a) shows that, under a light load step poorly reflected in the cap current, CPSI$_c$ can still be triggered. The derivative of the current does not vary as fast as in simulations when the loading occurs because of the limited slew rate of the operational amplifier. Fig. 20(b) shows that, under a negative voltage reference step, CPSI$_c$ is not triggered even if the threshold is very close to the triggering signal. Consequently, the circuit to disable CPSI$_c$ is not needed.

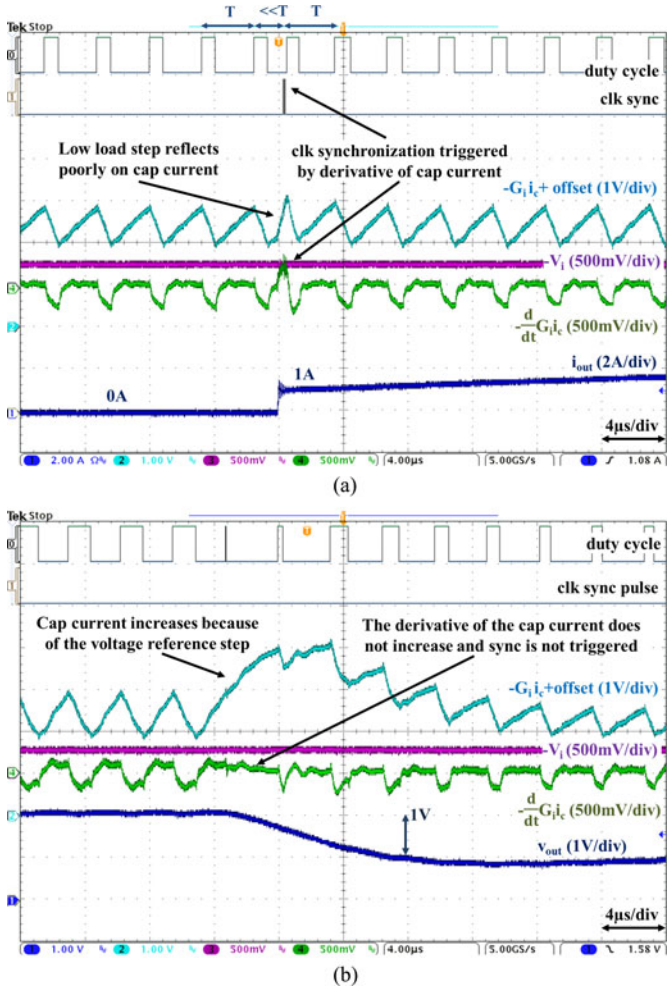

Fig. 20. Experimental validation of CPSI$_c$ using the derivative of the current through the output capacitor as the triggering signal. (a) Output voltage in blue, (b) output current in blue, measurement of the current through the output capacitor in light blue, derivative of the current in green, comparator signal in purple, synchronization pulse (lower digital signal), and duty cycle (upper digital signal) in black. (a) Load step 0 to 1 A. (b) Negative reference voltage step 2 to 1 V.

V. Summary and Conclusions

This paper has presented and validated a method to improve the dynamic response of $V^2 I_c$ with constant frequency modulation called CPSI$_c$ technique. $V^2 I_c$ exhibits an almost optimal transient response under load disturbances and reference voltage tracking. But, if the control is modulated with constant frequency, an additional deviation of the output voltage occurs that is not dependent of the control. This is caused by the delay in the switching action when a load disturbance occurs during the off-time. CPSI$_c$ allows $V^2 I_c$ to react almost immediately, heavily reducing the drop of the output voltage. If no reference voltage tracking is required, the CPSI$_c$ block only needs one comparator, one inverter logic gate and one nand logic gate to generate the pulse.

CPSI$_c$ can be used also in applications that require reference voltage tracking, such in microprocessors with dynamic voltage scaling, although it is needed to disable CPSI$_c$ when a negative reference voltage step occurs. A "disable block" is also presented in the paper and validated experimentally. An alternative scheme that uses the derivative of the current through the output capacitor is also proposed. The benefits of this scheme is that light load steps can be detected, the "disable block" is no longer needed and the detection of the load step is less sensitive to variations of the output capacitance. Finally, the paper provides design guidelines in order to easily incorporate the CPSI$_c$ technique in the design of the controls. Furthermore, it can be easily added to existing controls to enhance their dynamic behavior without perturbing it.

As a result of the work of the paper, several conclusions have been drawn:

1) The dynamic response of controls with constant frequency, constant on-time and constant off-time modulations is hindered by delays in the switching action. Because of this delay, an additional deviation of the output voltage occurs under certain load transients independently of how fast the control is. If this limitation is not avoided, the use of very fast controls with these modulations becomes less practical.

2) For applications with small duty cycles, modulations with constant frequency and constant off-time can be preferable because the worst-case voltage deviation is, in general, smaller. This is because, for these modulations, the additional drop increases the smaller voltage deviation, caused by the loading transient. On the other hand, the voltage deviation in modulations with constant on-time increases the larger voltage deviation, caused by the unloading transient.
3) A synchronization of the clock of the modulation when a loading transient occurs can avoid this delay in constant frequency and in constant off-time modulations. When the clock is synchronized, a new period starts and the switching action starts immediately.
4) Methods of the state of the art rely on changes of the output of the linear controller to trigger the synchronization of the clock of the modulation. Unfortunately, these methods are not effective in common ripple-based controls, which exhibit a very fast dynamic performance. This is because the linear controller of common ripple-based controls is designed with a low bandwidth and, consequently, the output of the linear controller varies slowly. In fact, in some controls, the linear controller is even completely replaced by a constant reference voltage.
5) $\mathrm{CPSI_c}$ uses the current through the output capacitor as the triggering signal. As a change in the load affects immediately this signal, it provides a very quick synchronization. It can be used with ripple-based controls and in applications with reference voltage tracking. Also, it can be used with constant on-time controls by adapting the on-time instead of synchronizing the clock (as seen in [23] and [24]).
6) Buck converters with low inductance get more benefit from $\mathrm{CPSI_c}$. This is especially interesting in very high frequency converters such as integrated converters. As these converters usually have low inductance, $\mathrm{CPSI_c}$ can greatly improve their dynamic performance and reduce the required size of the output capacitor.
7) As $\mathrm{CPSI_c}$ uses the current through the output capacitor, it is valuable to use also the measured current in the control as it provides a feedforward of the output current. For this reason, if designers want to enhance their control with $\mathrm{CPSI_c}$, it seems appropriate to choose the $V^2 I_c$ control in order to achieve a very fast dynamic behavior.

REFERENCES

[1] M. Del Viejo, P. Alou, J. Oliver, O. Garcia, and J. Cobos, "$v^2 i_c$ control: A novel control technique with very fast response under load and voltage steps," in *Proc. 26th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2011, pp. 231–237.

[2] J. Cortes, V. Svikovic, P. Alou, J. A. Oliver, and J. A. Cobos, "Comparison of the behavior of voltage mode, v2 and v2ic control of a buck converter for a very fast and robust dynamic response," in *Proc. Appl. Power Electron. Conf. Expo.*, 2014, pp. 2888–2894.

[3] J. Cortes, V. Svikovic, P. Alou, J. A. Oliver, and J. A. Cobos, "Impact of the control on the size of the output capacitor in the integration of buck converters," in *Proc. 8th Int. Conf. Integr. Power Electron. Syst.*, Feb. 2014, pp. 1–6.

[4] Y. Yian, P.-H. Liu, F. Lee, Q. Li, and S. Tian, "V2 control with capacitor current ramp compensation using lossless capacitor current sensing," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2013, pp. 117–124.

[5] S. Huerta, P. Alou, J. Oliver, O. Garcia, J. Cobos, and A. Abou-Alfotouh, "Design methodology of a non-invasive sensor to measure the current of the output capacitor for a very fast non-linear control," in *Proc. 24th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2009, pp. 806–811.

[6] W. Huang, "A new control for multi-phase buck converter with fast transient response," in *Proc. 16th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2001, vol. 1, pp. 273–279.

[7] M. Siu, P. Mok, K.-N. Leung, Y.-H. Lam, and W.-H. Ki, "A voltage-mode PWM buck regulator with end-point prediction," *IEEE Trans. Circuits Syst. II: Expr. Briefs*, vol. 53, no. 4, pp. 294–298, Apr. 2006.

[8] Y. Y. Mai and P. Mok, "A constant frequency output-ripple-voltage-based buck converter without using large ESR capacitor," *IEEE Trans. Circuits Syst. II: Expr. Briefs*, vol. 55, no. 8, pp. 748–752, Aug. 2008.

[9] Y.-H. Lee, S.-C. Huang, S.-W. Wang, and K.-H. Chen, "Fast transient (FT) technique with adaptive phase margin (APM) for current mode DC–DC buck converters," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 20, no. 10, pp. 1781–1793, Oct. 2012.

[10] M. Agostinelli, S. Fabbro, R. Priewasser, S. Marsili, and M. Huemer, "Pseudo sliding mode control for a positive buck-boost converter IC in 0.13 #x00b5;m CMOS," in *Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2013, pp. 2551–2554.

[11] P.-H. Liu, Y. Yan, F. Lee, and P. Mattavelli, "External ramp autotuning for current mode control of switching converters," in *Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2013, pp. 276–280.

[12] Y. Yan, F. Lee, P. Mattavelli, and P.-H. Liu, "Average current mode control for switching converters," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 2027–2036, Apr. 2014.

[13] R. Redl, B. Erisman, and Z. Zansky, "Optimizing the load transient response of the buck converter," in *Proc. 13th Annu. Conf. Proc. Appl. Power Electron. Conf. Expo.*, 1998, vol. 1, pp. 170–176.

[14] E. Meyer, Z. Zhang, and Y.-F. Liu, "An optimal control method for buck convertersusing a practical capacitor chargebalance technique," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1802–1812, Jul. 2008.

[15] E. Meyer, Z. Zhang, and Y.-F. Liu, "Controlled auxiliary circuit to improve the unloading transient response of buck converters," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 806–819, Apr. 2010.

[16] F. Su, W.-H. Ki, and C.-Y. Tsui, "Ultra fast fixed-frequency hysteretic buck converter with maximum charging current control and adaptive delay compensation for DVS applications," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 815–822, Apr. 2008.

[17] S. Huerta, P. Alou, J. Oliver, O. Garcia, J. Cobos, and A. Abou-Alfotouh, "Nonlinear control for DC #x2013;dc converters based on hysteresis of the current with a frequency loop to operate at constant frequency," *IEEE Trans. Ind. Electron.*, vol. 58, no. 3, pp. 1036–1043, Mar. 2011.

[18] Y. Zheng, H. Chen, and K. N. Leung, "A fast-response pseudo-PWM buck converter with PLL-Based hysteresis control," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 20, no. 7, pp. 1167–1174, Jul. 2012.

[19] B. Labbe, B. Allard, L.-S. Xuefang, and D. Chesneau, "An integrated sliding-mode buck converter with switching frequency control for battery-powered applications," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4318–4326, Sep. 2013.

[20] Y. Yan, F. Lee, and P. Mattavelli, "Comparison of small signal characteristics in current mode control schemes for point-of-load buck converter applications," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3405–3414, Jul. 2013.

[21] T. F. Schiff, "Switching power supply control with phase shift," U.S. 2007/0001655, Jan. 4, 2007.

[22] M. Steyaert, A. Roermund, and H Casier, "Enhanced ripple regulators," in *Analog Circuit Design by R. Redl.* New York, NY, USA: Springer-Verlag, 2009, pp. 255–268.

[23] R. Redl and J. Sun, "Ripple-based control of switching regulators: An overview," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2669–2680, Dec. 2009.

[24] J.-S. Chang, H.-S. Oh, Y.-H. Jun, and B.-S. Kong, "Fast output voltage-regulated pwm buck converter with an adaptive ramp amplitude control," *IEEE Trans. Circuits Syst. II: Expr. Briefs*, vol. 60, no. 10, pp. 712–716, Oct. 2013.

[25] R. Miftakhutdinov, "Analysis and optimization of synchronous buck converter at high slew-rate load current transients," in *Proc. IEEE 31st Annu. Power Electron. Spec. Conf.*, 2000, vol. 2, pp. 714–720.

[26] "Uc3823 data sheet," Texas Instruments. Available: http://www.ti.com/product/uc3823

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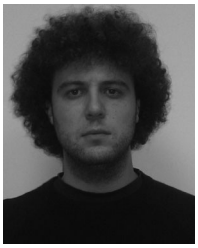

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