Design and Operation of a Hybrid Modular Multilevel Converter

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***Abstract*—This paper presents a hybrid modular multilevel converter (MMC), which combines full-bridge submodules (FBSM) and half-bridge submodules (HBSM). Compared with the FBSM-based MMC, the proposed topology has the same dc fault blocking capability but uses fewer power devices hence has lower power losses. To increase power transmission capability of the proposed hybrid MMC, negative voltage states of the FBSMs are adopted to extend the output voltage range. The optimal ratio of FBSMs and HBSMs, and the number of FBSMs generating a negative voltage state are calculated to ensure successful dc fault blocking and capacitor voltage balancing. Equivalent circuits of each arm consisting of two individual voltage sources are proposed and two-stage selecting and sorting algorithms for ensuring capacitor voltage balancing are developed. Comparative studies for different circuit configurations show excellent performance balance for the proposed hybrid MMC, when considering dc fault blocking capability, power losses, and device utilization. Experimental results during normal operation and dc fault conditions demonstrate feasibility and validity the proposed hybrid MMC.**

***Index Terms*—DC fault, hybrid, modular multilevel converter (MMC), power losses, voltage ripple.**

I. Introduction

THE modular multilevel converter (MMC) has drawn attention due to its advantages of modular design, high efficiency and scalability, and excellent output waveform with low harmonic distortion, etc., [1]–[12].

The basic building block in an MMC is a submodule (SM). The half-bridge-based SM (HBSM) has been the main configuration in the MMC [1]–[7]. However, an HBSM-based MMC (HB-MMC) does not have dc fault blocking capability, thus relies on ac or dc circuit breakers to isolate dc faults [13], [14]. This becomes problematic for both the converter as it has to withstand a high fault current and the connected network since it could take considerable time for the system (especially a multiterminal system) to recover a dc fault [15]. Thyristors connected in antiparallel to the SM terminals can be employed [16], [17] to bypass the short-circuit current and protect the freewheel diodes. However, this method does not isolate a dc fault and additional devices are required for fast fault isolation.

To address the issues of dc faults, the full-bridge-based SM (FBSM) was proposed which has the inherent advantage of dc fault blocking capability. However, the number of SM power devices is doubled compared to the HBSM. This not only increases the costs of high power MMC systems but also results in higher power loss as the current in each SM flows thought two power devices instead of one as in an HBSM. To increase power device utilization, various studies have been performed which use the negative voltage output from the FBSM to increase the modulation index and ac voltage output [8]–[10]. In [8], the concept of using the negative voltage state of the FBSM to increase voltage output was mentioned, but no detailed relationship between the ac and dc voltages and modulation index limit were considered. The relationship among the capacitor voltages, the ac and dc voltages was presented in [9], but the effect of the use of a negative voltage state on energy variation and capacitor voltage ripple are not addressed. In [10], the focus was on eliminating the energy oscillation between the upper and lower arms using a desirable modulation index of 1.414 for a full-bridge-based MMC (FB-MMC). However, for all studies that consider the use of the FBSM negative voltage state, no systematic design and detailed analysis on SM capacitor voltage variation, has been provided.

Voltage ripple and capacitance of the SM capacitors are a crucial factor for the operation, size and cost of MMC systems [18]–[23]. For HB-MMC systems, a method to calculate the capacitance was derived in [18], considering the energy variation and the corresponding voltage ripple. The minimum capacitance in terms of voltage balancing requirements has been investigated in [19]. A method to minimize the required capacitance by injecting harmonics into the circulating current was proposed in [20]. The minimum capacitance and the energy storage requirements with respect to the energy variation were analyzed in [21] and [22], respectively. A detailed analysis on the impact of the circulating current on capacitor voltage ripple is provided in [23]. For an FB-MMC using the negative voltage state, the effect of the number of FBSMs allowed to generate the negative voltage state, on capacitor voltage balancing, has not been investigated.

Voegeli *et al.* [24] illustrate how HBSM can be used as the basic building blocks to form different circuit configurations by varying the connections of the respective output

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terminals in order to provide a space-saving, simple structure, easy to maintain, durable and cost-effective power electronic switching module. For example, an FBSM can be implemented by parallel connection of the dc sides and series connection of the ac sides of two HBSMs, and further parallel and series connection of the ac/dc sides can be made to form different circuit configurations. However, there is no mention of the use of different configurations within the same converter leg.

Considering the mentioned issues, a hybrid MMC consisting of a combination of FBSMs and HBSMs, is proposed in this paper. The hybrid MMC not only has dc fault blocking capability but also uses fewer semiconductor devices and has lower power loss than the FB-MMC. However, in contrast to the conventional MMC in which all the SMs are identical, FBSMs and HBSMs in the hybrid MMC function differently in the charging and discharging periods and therefore, their capacitor voltage ripple and balancing need to be carefully analyzed.

The paper is organized as follows. Section II introduces the basic topology and design principles of the proposed hybrid MMC. The detailed analysis of capacitor voltage ripple and the proposed SM sorting and selecting algorithm are discussed in Section III. Comparison among the different MMC topologies is carried out in Section IV. Section V provides the experimental results to demonstrate the feasibility of the proposal and Section VI draws the conclusions.

II. Hybrid MMC Design Principle

A. Basic Configuration

Fig. 1 shows one leg of the proposed hybrid MMC. Each of the two arms in each leg has N submodules, comprising F FBSMs, notated as $\mathrm{SM_{f(1)}}$ to $\mathrm{SM_{f(F)}}$ and *N–F* HBSMs denoted as $\mathrm{SM_{h(1)}}$ to $\mathrm{SM_{h(N--F)}}$. V_{dc} is the dc-link voltage, L_0 is the arm inductance, C is the SM capacitance, and V_c is the dc voltage across each SM capacitor. The total voltages generated by all the SMs in the upper and lower arms are represented by v_{pa} and v_{na}, respectively. i_{pa} and i_{na} are the upper and lower arm currents, respectively, and i_a is the output ac phase current.

Tables I and II show the switch states for an FBSM and HBSM, respectively. Compared to the HBSM which can generate voltage states V_c and 0, each FBSM can generate a third state of $-V_c$. In the proposed scheme, some of the FBSMs are allowed to generate the $-V_c$ voltage state to increase the ac output voltage.

Assuming the total number of SMs in each arm is N (comprising F FBSMs and *N–F* HBSMs) and the capacitor voltage across all the SMs are balanced at V_c, the range of the generated total arm voltage is from 0 to NV_c for the conventional method without using the $-V_c$ state of the FBSMs. Thus, considering a maximum modulation index m of 1, the dc and peak ac phase voltages are

$$V_{\mathrm{dc}} = NV_c, V_{an\_\mathrm{peak}} = {}^1\!/_2 NV_c = {}^1\!/_2 V_{\mathrm{dc}}. \tag{1}$$

If M FBSMs in the hybrid MMC are allowed to generate the $-V_c$ state in each arm $(M < F)$, the arm voltage range will be extended, between $-MV_c$ and NV_c. Under such conditions, the dc and peak ac phase voltages are

$$V_{\mathrm{dc}} = (N - M)\, V_c$$
$$V_{an\_\mathrm{peak}} = {}^1\!/_2 (N + M)\, V_c = {}^1\!/_2 V_{\mathrm{dc}} + \frac{MV_{\mathrm{dc}}}{N - M}. \tag{2}$$

From (2) the peak ac phase voltage can be extended due to M FBSMs generating the $-V_c$ state.

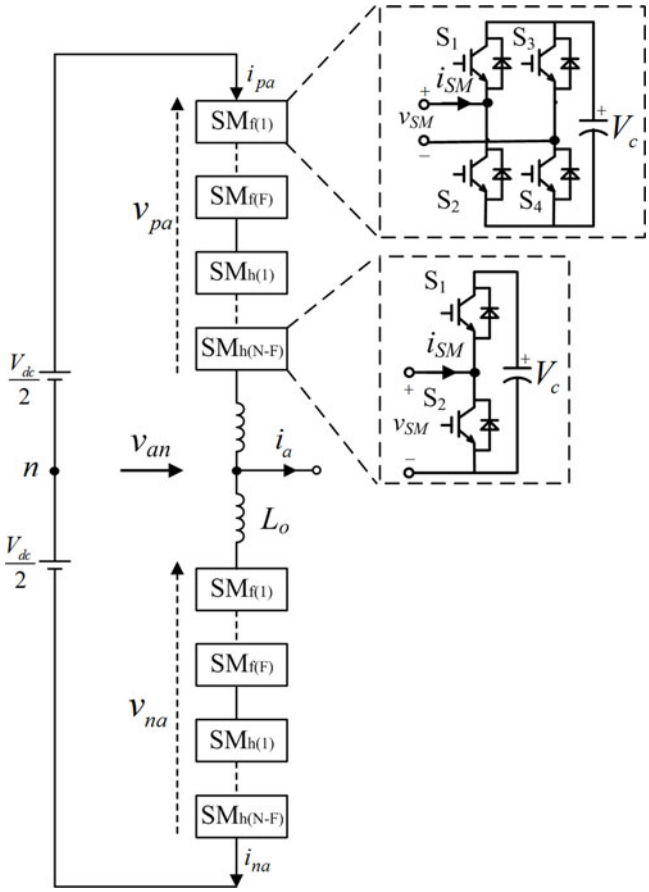

Fig. 1. Basic structure of a hybrid MMC.

TABLE I
Switch States of FBSM

STATE	S_1	S_2	S_3	S_4	v_{sm}	V_c (i_{SM}>0)
1	1	0	0	1	V_C	*charging*
2	0	1	0	1	0	*unchanged*
3	1	0	1	0	0	*unchanged*
4	0	1	1	0	$-V_C$	*discharging*
BLOCK	0	0	0	0	-	-

TABLE II
Switch States of HBSM

STATE	S_1	S_2	v_{sm}	V_c (i_{SM}>0)
1	1	0	V_C	*charging*
2	0	1	0	*unchanged*

B. Capacitor Voltage Balancing Consideration

For satisfactory MMC operation it is necessary to ensure the capacitor voltage in each SM can be balanced. In contrast to FBSMs that can charge and discharge their SM capacitors without having to change the external current direction, HBSM capacitors can only be charged during positive arm current and discharged during negative arm current. As the number of FBSMs generating a $-V_c$ state increases, the relationships among the ac voltage, dc voltage, and dc current also change. Thus, it is necessary to analyze the impact of the number of FBSMs generating the $-V_c$ state on the charging and discharging time for the SM capacitors.

Neglecting converter power loss, the steady-state three-phase ac and dc powers are

$$P_{\rm dc} = V_{\rm dc} I_{\rm dc} = 3/2 V_m I_m \cos\varphi = P_{\rm ac} \tag{3}$$

where V_m and I_m are the peak ac output phase voltage and current, φ is the voltage and current phase angle, and $I_{\rm dc}$ is the dc current.

Substituting $V_m = {}^1\!/_2 m V_{\rm dc}$ into (3) yield

$$I_{\rm dc} = 3/4 m I_m \cos\varphi \tag{4}$$

where m is the modulation index.

Considering the fundamental frequency and dc components, the arm currents are given by

$$\begin{cases} i_p = 1/2 I_m \sin(\omega t - \varphi) + 1/3 I_{\rm dc} \\ i_n = -1/2 I_m \sin(\omega t - \varphi) + 1/3 I_{\rm dc}. \end{cases} \tag{5}$$

Substituting (4) into (5) yields

$$\begin{cases} i_p = 1/2 I_m \sin(\omega t - \varphi) + 1/4 m I_m \cos\varphi \\ i_n = -1/2 I_m \sin(\omega t - \varphi) + 1/4 m I_m \cos\varphi. \end{cases} \tag{6}$$

To ensure sufficient charging and discharging times for the HBSMs, the arm currents must be both positive and negative within one complete period. So the following equation must be satisfied:

$$1/4 m I_m \cos\varphi \le 1/4 m I_m \le 1/2 I_m. \tag{7}$$

Thus, the modulation index m must be less than or equal to 2. According to (2), the following relationship can be derived:

$$1/2 V_{\rm dc} + \frac{M V_{\rm dc}}{N - M} \le V_{\rm dc}, M \le 1/3 N. \tag{8}$$

It can be concluded that for the hybrid MMC, M (the number of FBSMs generating $-V_c$) must not be more than 1/3N in order to ensure sufficient charging and discharging times for the HBSMs to balance their capacitor voltages within each fundamental period.

C. DC Fault Blocking Consideration

If the series voltage formed by all the FBSM capacitors along a fault current path is higher than the ac line-to-line voltage, a dc fault can be blocked once all the IGBTs are switched off. In view of this requirement, the minimum number of FBSMs within each arm can be derived.

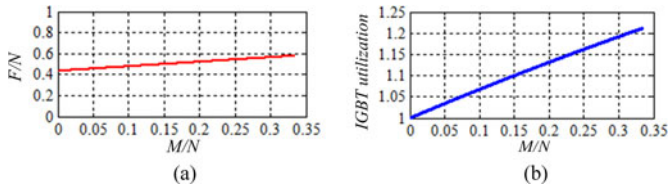

Fig. 2. Impact of M variation on F value and IGBT device utilization.

According to (2), the peak line-to-line ac voltage for the MMC during a dc fault, at maximum modulation index, is

$$u_{\rm max} = \sqrt{3} \times \frac{N + M}{2(N - M)} V_{\rm dc}. \tag{9}$$

Each arm has F FBSMs, thus the arm voltage formed by the FBSMs during dc faults is

$$u_{\rm arm} = F V_c = \frac{F}{(N - M)} V_{\rm dc}. \tag{10}$$

Therefore, the blocking voltage formed by two series arm voltages (one upper arm and one lower arm in different legs) and the ac line-to-line voltage should meet the following criteria:

$$u_{\rm max} = \frac{\sqrt{3}}{2} \frac{N + M}{(N - M)} V_{\rm dc} \le \frac{2F}{(N - M)} V_{\rm dc} = 2 u_{\rm arm}. \tag{11}$$

Thus, to successfully block dc faults, the total number of FBSMs has to meet the following requirement:

$$F \ge \frac{\sqrt{3}}{4}(N + M). \tag{12}$$

According to this analysis, both (8) and (12) need be satisfied when designing the hybrid MMC. Fig. 2(a) shows the minimum allowed *F/N* value, which results in the lowest number of required power device, for the variation of *M/N* from 0 to 1/3. In Fig. 2(b), the normalized maximum IGBT utilization where the value at $M = 0$ is defined as 1 (higher value means better use of the IGBT or for delivering same power, less IGBT would be required), is illustrated. As can be seen, the maximum device utilization increases with the increase of the *M/N* value.

Two specific conditions are considered further as examples for analyzing the circuit and control strategy.

1) $M = 0, F = 1/2N$

In this scenario, the hybrid MMC consists of half HBSMs and half FBSMs. Since $M = 0$, there is no $-V_c$ state used for the FBSMs, the number of HBSMs and FBSMs are same ($\frac{1}{2}N$) and the conventional control strategy for the HB-MMC [2] can be adopted. No further discussion is presented here.

2) $M = 1/3N, F = 2/3N$

In this scenario, the hybrid MMC consists of 1/3N HBSMs and 2/3N FBSMs (i.e., $F = 2/3N$). Among the 2/3N FBSMs, the maximum number of SM generating $-V_c$ state is half of the total FBSMs, i.e., 1/3 of the total number of SMs ($M = 1/3N$). This configuration is now investigated further.

III. Capacitor Voltage Balancing

Due to the use of the negative voltage state for some SMs, the total voltage in each arm can be considered as two

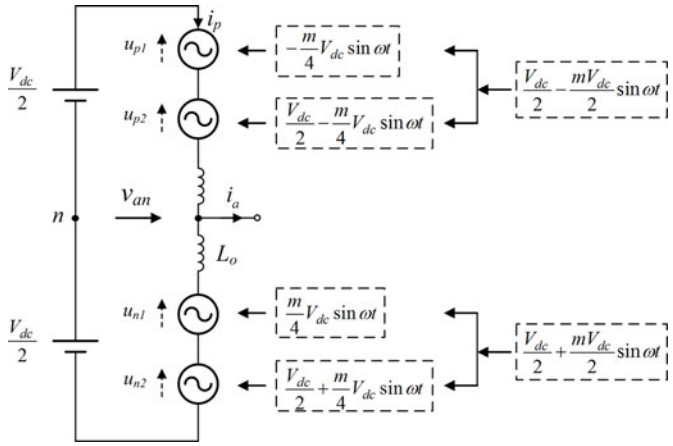

Fig. 3. Equivalent circuit for the hybrid MMC.

series-connected voltage sources as shown in Fig. 3. As shown, u_{p1} and u_n1 refer to the ac voltages having amplitudes of $1/4mV_{\rm dc}$ generated by the M (i.e., $1/3N$) FBSMs utilizing the $-V_c$ state. u_{p2} and u_{n2} are the voltages generated by the remaining *N–M* SMs with the same ac voltage amplitudes of $1/4mV_{\rm dc}$ but with a dc offset of $1/2V_{\rm dc}$.

A. Steady-State Analysis

Since the analysis in the upper and the lower arms in a leg is the same, the following analysis is based on the upper arm.

According to the presented analysis, the total arm voltage can be divided into two parts

$$\begin{cases} u_{p1} = -1/4mV_{\rm dc}\sin\omega t \\ u_{p2} = 1/2V_{\rm dc} - 1/4mV_{\rm dc}\sin\omega t. \end{cases} \tag{13}$$

The instantaneous power into each voltage source is

$$\begin{aligned} p_{p1} &= u_{p1}\times i_p = -\frac{mV_{\rm dc}}{4}\sin\omega t \\ &\quad\times\left(\frac{I_m}{2}\sin(\omega t-\varphi)+\frac{mI_m}{4}\cos\varphi\right) \\ &= -\frac{m^2V_{\rm dc}I_m}{16}\cos\varphi\sin\omega t - \frac{mV_{\rm dc}I_m}{16}\cos\varphi \\ &\quad+\frac{mV_{\rm dc}I_m}{16}\cos(2\omega t-\varphi) \end{aligned} \tag{14}$$

$$\begin{aligned} p_{p2} &= u_{p2}\times i_p \\ &= \left(\frac{V_{\rm dc}}{2}-\frac{mV_{\rm dc}}{4}\sin\omega t\right)\left(\frac{I_m}{2}\sin(\omega t-\varphi)+\frac{mI_m}{4}\cos\varphi\right) \\ &= \frac{V_{\rm dc}I_m}{4}\sin(\omega t-\varphi)-\frac{m^2V_{\rm dc}I_m}{16}\cos\varphi\sin\omega t \\ &\quad+\frac{mV_{\rm dc}I_m}{16}\cos\varphi+\frac{mV_{\rm dc}I_m}{16}\cos(2\omega t-\varphi). \end{aligned} \tag{15}$$

Integrating the instantaneous power in one fundamental period yields the net energy flowing into each voltage source as

$$\Delta E_{p1} = \int_0^{2\pi} p_{p1}dt = -1/8\pi mV_{\rm dc}I_m\cos\varphi \le 0 \tag{16}$$

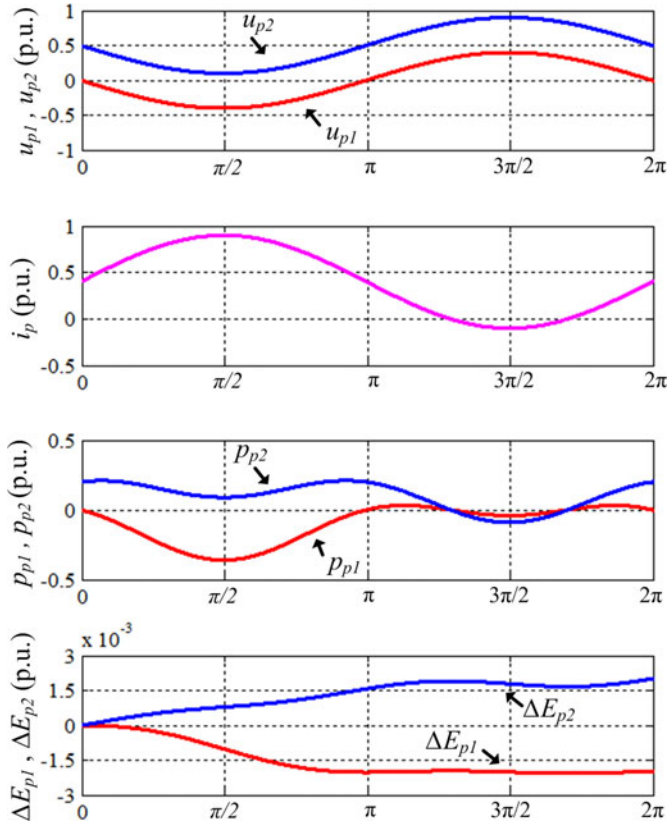

Fig. 4. Transferring energy through u_{p1} and u_{p2}.

$$\Delta E_{p2} = \int_0^{2\pi} p_{p2}dt = 1/8\pi mV_{\rm dc}I_m\cos\varphi \ge 0 \tag{17}$$

$$\Delta E = \Delta E_{p1} + \Delta E_{p2} = 0. \tag{18}$$

From (18), although the net energy transferring in one fundamental period in each arm is zero, the net energy in the two separate u_{p1} and u_{p2} is not zero. Therefore, in order to maintain capacitor voltage balance, it is necessary to exchange energy between u_{p1} and u_{p2} within each fundamental period. For this hybrid MMC configuration, $1/3N$ FBSMs are operated in u_{p1}, and the other $1/3N$ FBSMs are operated in u_{p2}. Thus, if each FBSM can be arranged to operate in both u_{p1} and u_{p2} by specific sorting and selecting algorithms, they can be used as a bridge for transferring energy between u_{p1} and u_{p2}.

B. Modified Sorting and Selection Algorithm

As indicated in (6), increasing m in the proposed hybrid MMC gradually reduces the time intervals when the upper arm current i_p is negative. This affects capacitor voltage balance in the HBSMs due to the reduced discharging time. Thus, in contrast to the conventional capacitor voltage balancing algorithm [2], in which only capacitor voltage and arm current direction are used for SM selection, the selection of SMs in the hybrid MMC has to consider the differences in their behavior, and charging and discharging periods between the FBSMs and HBSMs.

For illustrative purposes, Fig. 4 shows the reference voltages, arm current, and transferred energy in u_{p1} and u_{p2} in one

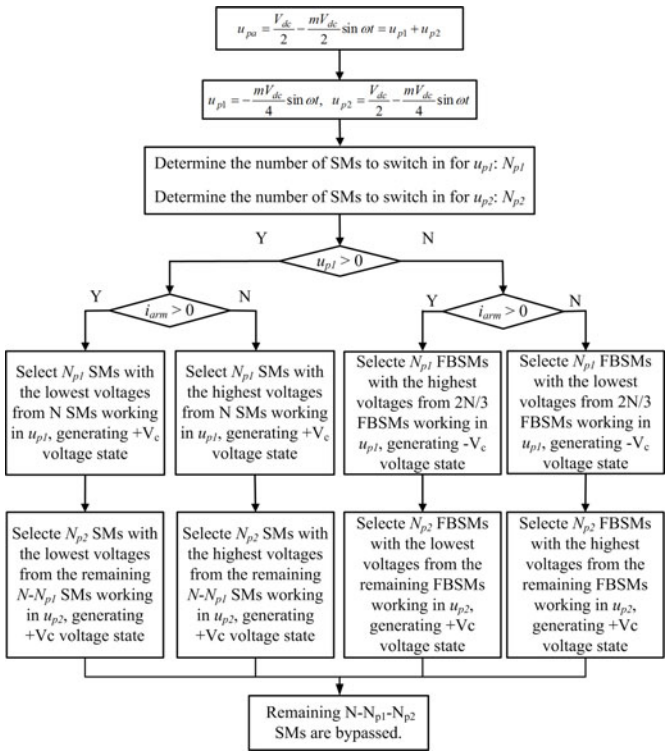

Fig. 5. Modified sorting and selection algorithm for the hybrid MMC.

TABLE III
COMPARISON AMONG THE FOUR TYPES OF MMC

	HB-MMC	FB-MMC	Hybrid MMC	
			$M = 0$, $F = \frac{1}{2}N$	$M = \frac{1}{3}N$, $F = \frac{2}{3}N$
DC link voltage	V_{dc}	V_{dc}	V_{dc}	V_{dc}
Maximum ac voltage	$\frac{1}{2}V_{dc}$	$\frac{1}{2}V_{dc}$	$\frac{1}{2}V_{dc}$	V_{dc}
SMs/per arm	$2n$	$2n$	$2n$	$3n$
IGBTs/per arm	$4n$	$8n$	$6n$	$10n$
Diodes/per arm	$4n$	$8n$	$6n$	$10n$
Power capacity (p.u.)	1	1	1	**2**
Power capacity per IGBT	$1/(4n)$	$1/(8n)$	$1/(6n)$	$1/(5n)$
DC fault blocking	No	Yes	Yes	Yes

complete period for $\varphi = 0$. From Fig. 4, ΔE_{p1} and ΔE_{p2} cannot reach balance in one complete period, as previously illustrated in (16) and (17). In the first half-cycle (0 to π), u_{p1} delivers energy while u_{p2} absorbs energy. Thus, it is necessary to transfer energy between these two voltage sources to ensure their respective net energy flow can remain balanced in one complete period. A modified sorting and selecting algorithm is thus proposed, as shown in Fig. 5.

The basic principles ofthe modified sorting and selection algorithm are summarized as follows.

1) In the first half-cycle period (0 to π), all $2/3N$ FBSMs are sufficient to generate the required reference voltages in u_{p1} and u_{p2} (within 0 ± 0.5 p.u.). Thus, only the $2/3N$ FBSMs are sorted and selected in this period with all the HBSMs producing zero output (i.e., their capacitors are bypassed). When the arm current is positive, the FBSMs having the highest capacitor voltages are selected to operate in u_{p1} producing $-V_c$ output and their capacitors are discharged. The FBSMs having the lowest capacitor voltages are assigned to u_{p2} producing $+V_c$ output and their capacitors are charged. This selection is reversed when the arm current is negative. This ensures the capacitor voltages in all the $2/3N$ FBSMs are balanced.
2) In the second half-cycle period (π to 2π), no $-V_c$ state is required. The sorting process is, thus, carried out within all N SMs where the SMs with the lowest capacitor voltages (for positive arm current) or the highest capacitor voltages (for negative arm current) are selected to operate in u_{p1} and u_{p2} producing $+V_c$ output. All the unselected SMs are bypassed generating zero voltage.

As the FBSMs are switched between u_{p1} and u_{p2} which effectively transfers energy between the two equivalent sources, all the capacitor voltages can be balanced.

TABLE IV
PARAMETERS OF THE DIFFERENT SYSTEMS

Item	HB-MMC	FB-MMC	Hybrid MMC	
			$M = 0$, $F = \frac{1}{2}N$	$M = \frac{1}{3}N$, $F = \frac{2}{3}N$
MMC rated power	5 MW	5 MW	5 MW	**10 MW**
DC voltage	5 kV	5 kV	5 kV	5 kV
AC voltage (L-L rms)	2.5 kV	2.5 kV	2.5 kV	**5 kV**
No. of SMs per arm (N)	2	2	2	3
No. of IGBTs per arm	4	8	6	10
SM capacitor voltage	2.5 kV	2.5 kV	2.5 kV	2.5 kV
Power capacity per IGBT	4.2%	2.1%	2.8%	3.3%
Average Switching frequency per SM (kHz)	1.25	1.25	1.25	FBSM: 1.05 HBSM: 0.40
Conduction Losses	24.0 kW (0.40%)	49.4 kW (0.82%)	36.7 kW (0.62%)	81.6 kW (0.68%)
Switching Losses	13.4 kW (0.22%)	13.4 kW (0.22%)	13.4 kW (0.22%)	38.0 kW (0.32%)
Total conversion losses	37.4 kW (0.6%)	62.8 kW (1.1%)	50.1 kW (0.8%)	119.6 kW (1.0%)

C. Variations on Capacitor Energy Storage

Due to the interactive behavior between the FBSMs and HBSMs, their capacitor voltage ripple is now considered.

For the example in Fig. 4, the maximum discharging energy variation on the FBSM capacitors occurs in the first half-cycle, and can be expressed as where θ_1 refers to the phase angle resulting in maximum discharging energy variation.

The charging energy variation on capacitors in the FBSMs occurs in the second half-cycle before the arm current is negative. Initially, the FBSMs are selected to be charged so as to compensate the discharged energy in the first half-cycle. After compensation is completed, the following charge energy is then assumed to be equally distributed among the $2/3N$ FBSMs and $1/3N$ HBSMs groups. So the maximum charging energy variation in the FBSM capacitors is

$$\Delta E_{fc\max} = 2/3 \times \left| \int_0^{\theta_2} (p_{p1} + p_{p2})\, dt \right| \tag{20}$$

where θ_2 is the phase angle when the arm current becomes negative.

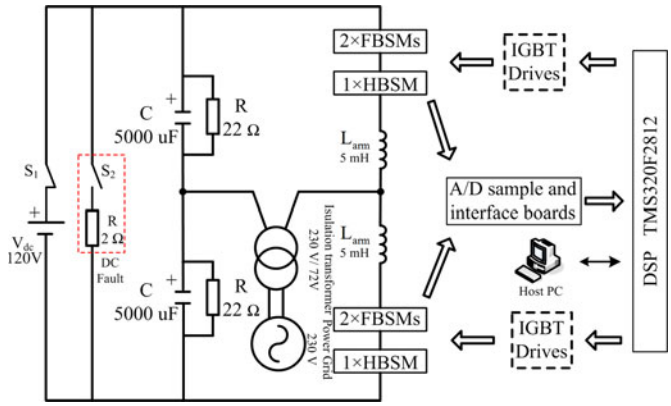

Fig. 6. Schematic diagram of the experimental system.

TABLE V
PARAMETERS OF THE EXPERIMENTAL MMC SYSTEM

Item	Values
MMC rated power	400 W
dc voltage	120 V
ac voltage (phase-ground rms.)	72 V
Number of SMs per arm	3
Number of FBSMs per arm	2
Number of HBSMs per arm	1
DC voltage per SM	60 V
SM capacitor	940 μF
Inductance per arm	5 mH
MMC switching frequency	2.5 kHz

Thus, the maximum energy variation on the FBSM capacitors is calculated as

$$\Delta E_{f\max} = \Delta E_{fc\max} + \Delta E_{fd\max}. \tag{21}$$

For the HBSMs, the total energy flowing in the whole second half-cycle is zero for the capacitor voltages to be balanced. Since HBSMs can be discharged only when $i_{\rm arm} < 0$, if the discharge energy is assumed to be equally distributed among the $2/3N$ FBSM and $1/3N$ HBSM groups, the maximum energy variation on the HBSM capacitors can be estimated by considering one-third of the total discharging energy when $i_{\rm arm} < 0$, i.e.

$$\Delta E_{h\max} = 1/3 \times \left| \int_{\theta_2}^{\theta_3} (p_{p1} + p_{p2})\, dt \right| \tag{22}$$

where θ_2 to θ_3 is the period when the arm current is negative.

According to $\Delta E_{\max} = E_{\max} - E_{\min}$, the maximum energy variation can also be estimated

$$\begin{aligned} \Delta E_{f\max} &= \frac{C_f}{2}\left(u_{fc\max}^2 - u_{fc\min}^2\right) F \\ &= \frac{V_{\rm dc}^2\left(D_{f\max}^2 - D_{f\min}^2\right) F}{2\left(N-M\right)^2} C_f \end{aligned} \tag{23}$$

$$\begin{aligned} \Delta E_{h\max} &= 1/2 C_h \left(u_{hc\max}^2 - u_{hc\min}^2\right) \times (N-F) \\ &= \frac{V_{dc}^2\left(D_{h\max}^2 - D_{h\min}^2\right)(N-F)}{2\left(N-M\right)^2} C_h \end{aligned} \tag{24}$$

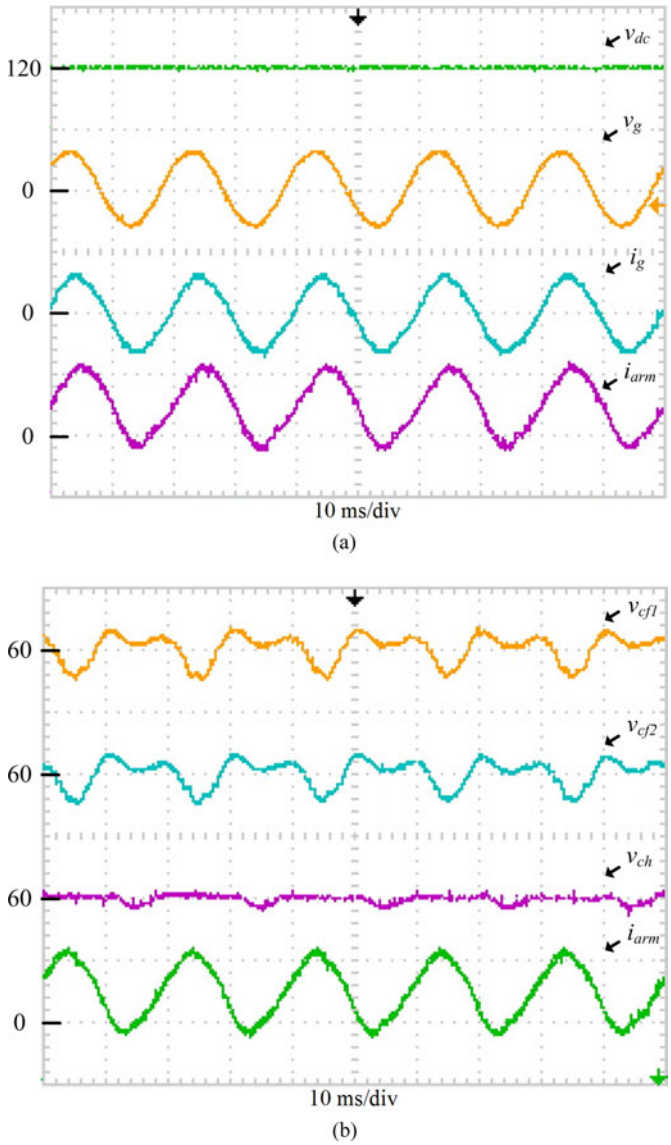

Fig. 7. Steady-state operation as an inverter, $V_{\rm dc}$: dc voltage (120 V/div); v_g: grid voltage (170 V/div); i_g: grid current (12 A/div); $i_{\rm arm}$: arm current (6 A/div); v_{cf1}: capacitor voltage in FBSM1 (10 V/div); v_{cf2}: capacitor voltage in FBSM2 (10 V/div); v_{ch}: capacitor voltage in HBSM (10 V/div).

where $D_{f\max}, D_{h\max}$, and $D_{f\min}, D_{h\min}$ denote the per unit maximum and minimum capacitor voltage for the FBSMs and HBSMs, respectively.

Substituting (21) and (22) into (23) and (24), the capacitance for the FBSMs and HBSMs can be expressed as

$$C_f = \frac{2\left(N-M\right)^2}{V_{\rm dc}^2\left(D_{f\max}^2 - D_{f\min}^2\right) F} \times \Delta E_{f\max} \tag{25}$$

$$C_h = \frac{2\left(N-M\right)^2}{V_{\rm dc}^2\left(D_{h\max}^2 - D_{h\min}^2\right)(N-F)} \Delta E_{h\max}. \tag{26}$$

The required capacitances for the HBSMs and FBSMs are different for the same voltage ripple and are also affected by operating conditions (i.e., $\Delta E_{f\max}$ and $\Delta E_{h\max}$ vary under different operation conditions). Taking the

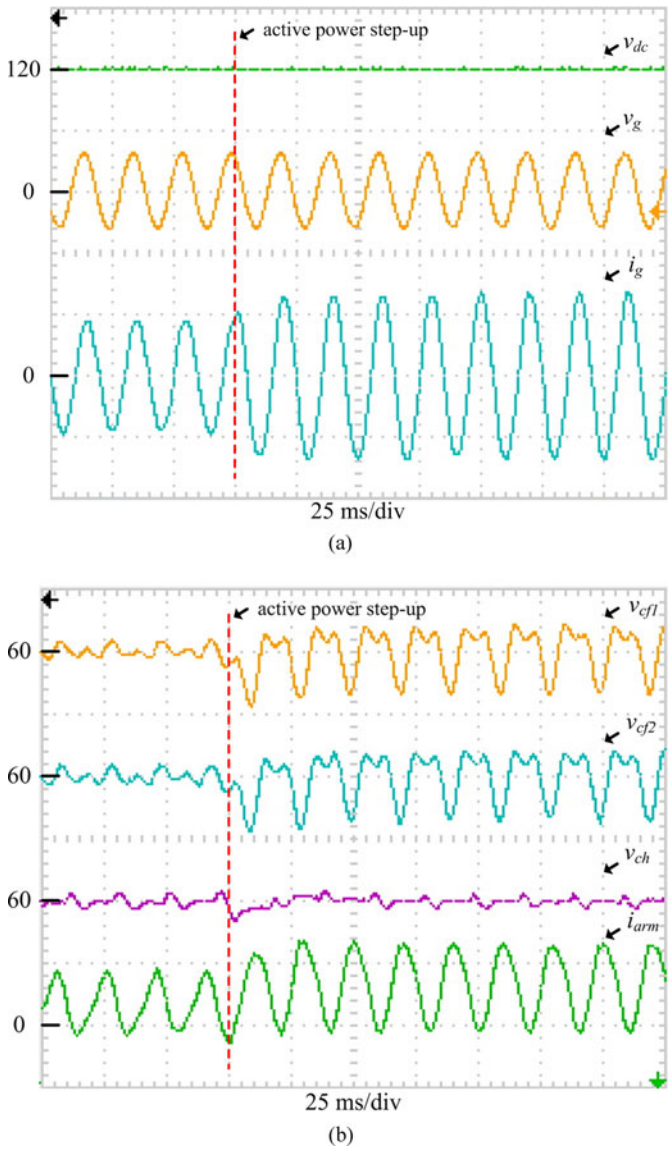

Fig. 8. Dynamic operation as an inverter during active power step, $V_{\rm dc}$: dc voltage (120 V/div); v_g: grid voltage (170 V/div); i_g: grid current (6 A/div); $i_{\rm arm}$: $i_{\rm arm}$ current (6 A/div); v_{cf1}: capacitor voltage in FBSM1 (10 V/div); v_{cf2}: capacitor voltage in FBSM2 (10 V/div); v_{ch}: capacitor voltage in HBSM (10 V/div).

experimental prototype for example, when the capacitance ratio of the FBSM and HBSM is 4.46:1, the maximum capacitor voltage ripples are equal $(N = 3, F = 2, M = 1, m = 1.6, V_{\rm dc} = 120\,{\rm V}, I_m = 7{\rm A}, \varphi = 0)$.

D. Operation Under Reduced DC Voltage

The aforementioned analysis is based on the normal operation with dc voltage controlled under nominal values. However, large disturbances, e.g., faults on ac or dc side can cause severe dc voltage drop. Under such a condition, conventional HB-MMC-based system would lose its control capability and have to be blocked to protect the IGBTs. With the proposed hybrid configuration, the relationship between the ac and dc voltages can be altered by changing the total number of SMs switched in (i.e., N) and the number of FBSMs generating $-V_c$ state (i.e., M). However, the capacitor voltage balance in the FBSMs and HBSMs needs be considered carefully.

The total number of required SMs selected is now N' and the number of FBSMs generating the $-V_c$ state is M'. Assuming the ac system voltage remains the same whereas the dc voltage has dropped from $V_{\rm dc}$ to $V_{\rm dc}$, the dc and ac phase voltages can be expressed as

$$V'_{\rm dc} = kV_{\rm dc} = k\,(N - M)\,V_c = (N' - M')\,V_c \tag{27}$$

$$V_m = \frac{1}{2}\,(N + M)\,V_c = \frac{1}{2}\,(N' + M')\,V_c \tag{28}$$

where k is the ratio between the new and initial dc voltages, and $k < 1$.

According to (27) and (28), the N' and M' are then calculated as

$$\begin{cases} N' = \dfrac{N}{2}\,(1 + k) + \dfrac{M}{2}\,(1 - k) < N \\ M' = \dfrac{M}{2}\,(1 + k) + \dfrac{N}{2}\,(1 - k) > M. \end{cases} \tag{29}$$

It is noted that the N' will have to decrease and M' to increase following the drop of dc voltage. Under the extreme condition of $V'_{\rm dc} = 0$ (i.e., $k = 0$), $M' = N' = (M + N)/2$. For previous design of $M = 1/3N$, $F = 2/3N$, this leads to $M' = N' = 2/3N$. This means the selection is carried out in the FBSMs and all the HBSMs are bypassed indicating the hybrid MMC is capable of operating during zero dc voltage. Under other lower dc voltage conditions, the HBSMs will still be used.

The power on ac and dc sides are given as

$$P'_{\rm dc} = V'_{\rm dc} I'_{\rm dc} = \frac{3}{2} V_m I'_m \cos\varphi' = P'_{\rm ac} \tag{30}$$

where $I'_{\rm dc}$ is the new dc current, I'_m and φ' are the new ac current amplitude and power factor angle, respectively.

The upper arm current is now rewritten as

$$i'_p = \frac{1}{2} I'_m \sin(\omega t - \varphi') + \frac{1}{3} I'_{\rm dc}. \tag{31}$$

Substituting (30) into (31) yields,

$$i'_p = \frac{V'_{\rm dc}}{3V_m \cos\varphi} I'_{\rm dc} \sin(\omega t - \varphi') + \frac{1}{3} I'_{\rm dc}. \tag{32}$$

To ensure sufficient charging and discharging times for the HBSMs, the arm currents must be both positive and negative within one complete period. So the following equation must be satisfied:

$$\frac{V'_{\rm dc}}{3V_m \cos\varphi} I'_{\rm dc} \geq \frac{1}{3} I'_{\rm dc}. \tag{33}$$

Substituting (27) and (28) into (33) gives the required power factor as

$$\cos\varphi' \leq \frac{2k\,(N - M)}{(N + M)}. \tag{34}$$

Equation (33) indicates that the power factor should be reduced following the drop of dc voltage. That means the control system needs use reactive current to ensure enough discharging

period for HBSMs so as to maintain SM capacitor voltage balancing. Again for the proposed design of $M = 1/3N$, this leads to $\cos\varphi' \leq k$ $(k < 1)$.

Thus, the proposed hybrid MMC can continue operating under reduced dc voltage with proper selection of the total number of SMs to be used (i.e., N'), the number of FBSMs generating $-V_c$ (i.e., M'), and the output power factor (i.e., φ'). The previously proposed sorting and selection algorithm is still applicable for maintaining SM capacitor voltage balancing and the system simply operates in the same way as normal condition, e.g., controlling the ac output and circulating current. The maximum energy variations on FBSMs and HBSMs can still be derived from (23) and (24) by replacing N, M, φ with N', M', and φ' from (29) and (34), and the SM capacitor voltage ripple can be estimated accordingly.

IV. Topology Comparison

A comparison among the hybrid MMC systems and the conventional HB-MMC and FB-MMC is carried out. Since the basic building blocks in the hybrid MMC are the same HBSM and FBSM as the conventional MMC, the reliability of the hybrid MMC would be similar to the HB-MMC and FB-MMC.

Table III shows the number of power semiconductors required for the different types of MMC. Taking the required semiconductor devices for the conventional HB-MMC as the bases for comparison, in which *4n* IGBT and *4n* diode are required for each arm, for delivering the same power, the conventional FB-MMC doubles the number of IGBT and diode (i.e., $8n$), whereas the proposed hybrid MMC $(M = 0, F = 1/2N)$ uses 50% more IGBT and diode (i.e., $6n$) and the hybrid MMC $(M = 1/3N, F = 2/3N)$ only has 25% increase in the total number of IGBT and diode (i.e., $5n$) compared to HB-MMC. This indicates that the proposed hybrid MMC system can provide dc fault blocking capability without significant increase on the total semiconductor devices.

To evaluate the power losses of the four MMC configurations, a simple loss calculation method is adopted [5]. The main parameters of the semiconductor module are derived from the datasheet of the 5SNA 1200G450300 [25], and the main parameters of the four MMC systems are shown in Table IV. The carrier frequency is 2.5 kHz for all four MMCs and the actual switching frequency for the SMs are also shown in Table IV.

The conduction losses and switching losses of the four MMC systems are also shown in Table IV. As expected, the conventional HB-MMC is the most efficient among the four MMC types. The proposed hybrid MMCs are shown as more efficient than the conventional FB-MMC due to the reduced switch number, hence conduction loss. The two hybrid configurations also have different features; $M = 1/3N, F = 2/3N$ results in a higher power density but slightly higher power loss than the configuration of $M = 0, F = 1/2N$, since the former needs extra switching for capacitor voltage balancing.

V. Experimental Results

To verify the presented analysis for the hybrid MMC with $M = 1/3N$ and $F = 2/3N$, a prototype single-phase hybrid MMC rated at 400 W was developed and its layout is shown in Fig. 6. Each arm contains two FBSMs and one HBSM. The control system is implemented using a TMS320F2812 DSP and the main parameters are listed in Table V. Two series-connected large dc capacitors are parallel connected across the dc power supply to create the neutral point.

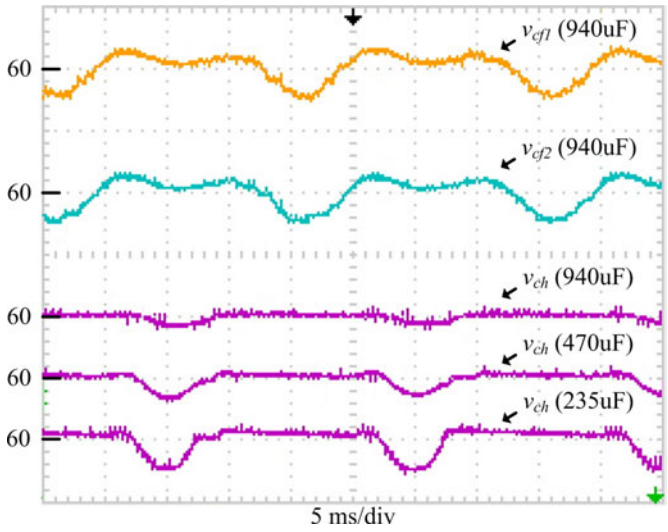

Fig. 9. Relation between capacitor ripple and capacitor value, v_{cf1}: capacitor voltage in FBSM1 (10 V/div); v_{cf2}: capacitor voltage in FBSM2 (10 V/div); v_{ch}: capacitor voltage in HBSM (10 V/div).

Figs. 7 and 8 respective show the steady-state and dynamic performances of the proposed hybrid MMC operating as an inverter in grid-connected mode, i.e., active power flows from the dc to ac. The output current shown in Fig. 7 is almost sinusoidal with low distortion. Voltage ripple on the FBSM capacitors is generally the same, with a peak-to-peak ripple of 11.7%. Maximum voltage ripple on the HBSM capacitors is about 2.7%, being lower than that of the FBSMs due to the same capacitance being used (940 μF). These values are in agreement with the calculated ripple of 11.99% and 2.69% using (23) and (24) for the FBSMs and HBSMs, respectively. The HBSM is bypassed during the first half-cycle period, verifying the previous sorting analysis. All capacitor voltages remain balanced. In Fig. 8, the active power is stepped from 220 to 400 W at 75 ms. The proposed hybrid MMC tracks the current and power changes quickly and smoothly, and the capacitor voltages remain balanced during the transient. The FBSM capacitor voltage ripple is considerably larger after the power step (current increase) due to increased $\Delta E_{f\max}$.

To further validate the relation between voltage ripple and capacitance, Fig. 9 shows the measured voltage ripple for different capacitances. In these tests, the FBSM capacitance is fixed at 940 μF, while capacitance for the HBSMs is varied at 940, 470, and 235 μF, respectively. As shown in Fig. 9, for the same capacitance, the maximum voltage ripples in the FBSMs and HBSMs with 940 μF are approximately 11.7% and 2.7%, respectively. The respective maximum voltage ripple in the HBSM rises to 6.7% with 470 μF and 10.0% with 235 μF. These values are in agreement with the calculated HBSM capacitor voltage

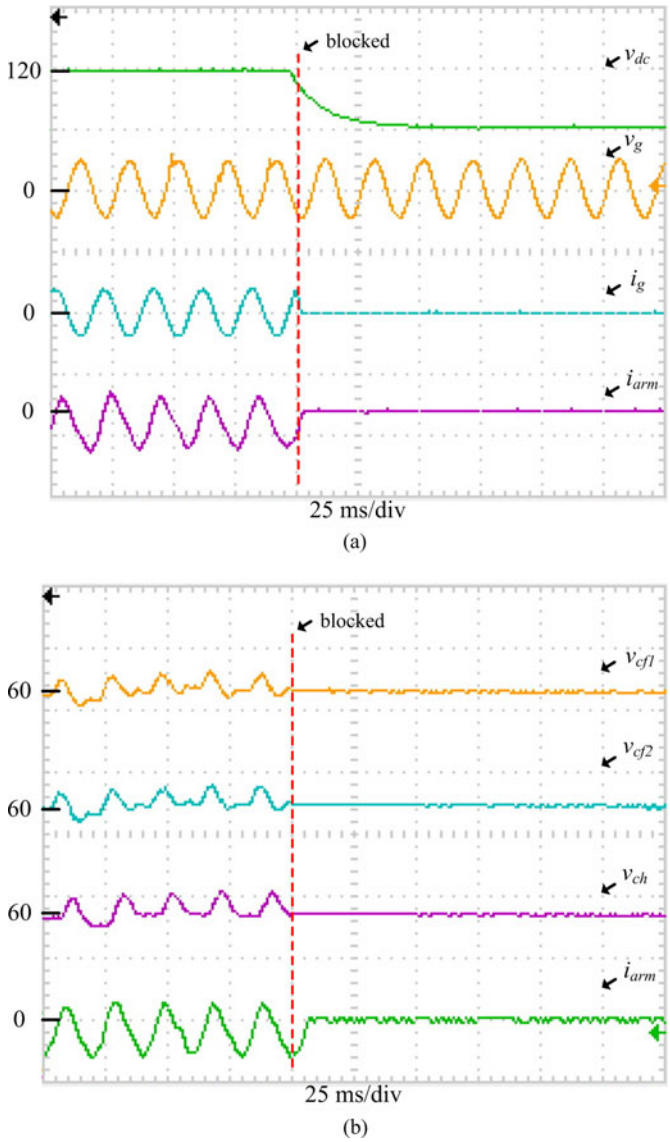

Fig. 10. DC fault, V_{dc}: dc voltage (120 V/div); v_g: grid voltage (170 V/div); i_g: grid current (12 A/div); $i_{\rm arm}$: arm current (6 A/div); v_{cf1}: capacitor voltage in FBSM1 (20 V/div); v_{cf2}: capacitor voltage in FBSM2 (20 V/div); v_{ch}: capacitor voltage in HBSM (20 V/div).

ripples of 2.69%, 5.37%, and 10.75% for 940, 470, and 230 μF, respectively.

Fig. 10 shows the experimental results during a dc line-to-line fault applied on the hybrid MMC system. Initially, the hybrid MMC operates as a rectifier, absorbing active power (-245 W) from the ac grid into the dc side (S_1 is open). A dc fault is emulated by connecting a 2 Ω resistor across the dc link (S_2 is closed). Immediately after the fault, the MMC remains operational until it is blocked when the overcurrent is detected as shown in Fig. 10 where $i_{\rm arm}$ increases rapidly after the dc fault. The capacitors in the selected SMs discharge before converter blocking. The dc voltage collapses quickly. Once the IGBTs are gated off, the fault current flows through the series capacitors in the FBSMs, while the capacitor in the HBSM is bypassed. There is a short charging period for the FBSM capacitors, whereas the HBSM capacitor voltage remains constant after IGBT blocking.

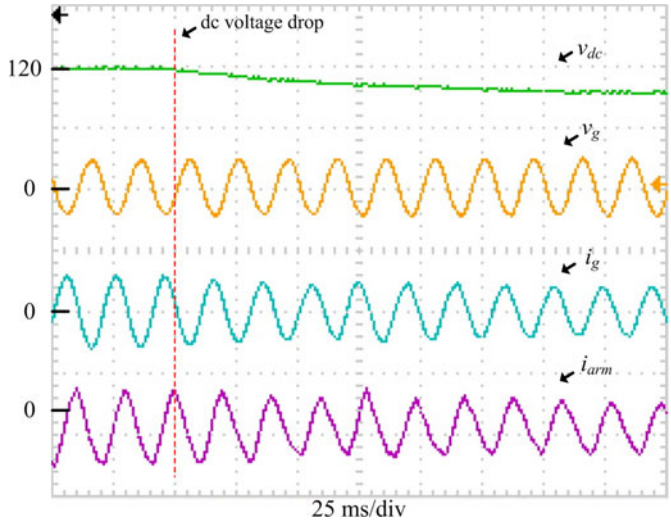

Fig. 11. DC voltage drop, $v_{\rm dc}$: dc voltage (120 V/div); v_g: grid voltage (170 V/div); i_g: grid current (12 A/div); $i_{\rm arm}$: arm current (6 A/div).

Since the total series voltage formed by the FBSMs is higher than the ac voltage, the ac current and arm current quickly reduce to zero and the dc fault is thus blocked.

Fig. 11 illustrates the operation performance of the hybrid MMC during significant dc voltage drop. Initially, the hybrid MMC operates as a rectifier, absorbing active power (370 W) from the ac grid into the dc side with a nominal dc voltage of 120 V. The dc voltage is then reduced from 120 to 70 V (42% drop) for conventional VSC, such large voltage drop would disable the converter operation since the dc voltage is now less than the ac voltage. For the proposed hybrid MMC, the active power is decreased proportionally to 215 W (a reduction of 42%) and a reactive power of 100 VAr is added to ensure sufficient charging period for the HBSMs. Under such condition, the modulation index rises to around 2.9. As shown in Fig. 11, the output ac current is still well controlled under such large dc voltage drop, and the hybrid MMC can regulate the active and reactive power demonstrating excellent operation and flexibility during dc voltage drop.

VI. Conclusion

This paper proposes a hybrid MMC configuration consisting of FBSMs and HBSMs. By adopting the negative voltage state for some of the FBSMs, the output voltage range is extended to increase converter power transmission capability. By considering the relationships between the ac and dc voltages, ac, dc, and arm currents, the ratio of FBSM to HBSM were analyzed in order to maintain capacitor voltage balance and retain dc fault blocking capability. An equivalent circuit for the hybrid MMC is proposed, which considers each arm to be consisted of two individual voltage sources. This model is used to analyze SM capacitor voltage balancing and ripple. A two-stage selection and sorting algorithm is developed to ensure capacitor voltage balancing among the SMs. The proposed hybrid MMC is compared to other topologies in terms of power device utilization and power losses. This comparison shows that the hybrid MMC

has higher device utilization and lower power loss than the conventional FB-MMC. Experiment results during steady state, power step and dc fault verify the theoretical analysis. The proposed hybrid MMC is a possibility for high power transmission application where dc fault blocking capability is required.

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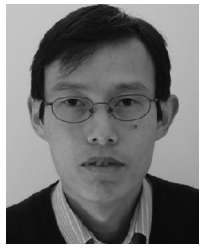

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