Derivation, Analysis, and Comparison of Nonisolated Single-Switch High Step-up Converters With Low Voltage Stress

Jae-Kuk Kim and Gun-Woo Moon

***Abstract*—This paper presents nonisolated single-switch high step-up converters with low voltage stress. Based on the conventional flyback converter, one single-switch high step-up converter is derived. The voltage stresses on the switch and diodes are limited by using a clamping diode and voltage doubler structure. Also, to further reduce the voltage stresses of them, another single-switch high step-up converter is proposed simply by using one additional capacitor and rearranging the components. Thus, lower voltage-rated switch and diodes can be used, which results in higher efficiency. The operational principle, analysis and design considerations of each converter are presented in this paper. The validity of this study is confirmed by the experimental results from 24 V input and 250 V/125 W output prototype.**

***Index Terms*—High step-up converter, low voltage stress, nonisolated, single switch.**

I. Introduction

NONISOLATED high step-up dc–dc converters are widely used as the front-end stage for the renewable energy applications and dc back-up energy system such as the solar arrays, fuel cells, uninterruptible power supply, and high-intensity-discharge (HID) lamps for automobile headlamps [1]–[15]. The high step-up converters have features of large input current and high output voltage. The large input current results from the low input voltage, so low-voltage-rated devices with low on-resistance $R_{\mathrm{ds(on)}}$ are required to reduce the conduction loss. Furthermore, the severe reverse-recovery problem occurs in rectifier diode due to the high output voltage. This can increase the current stress on the switch and voltage stress on the diode.

In general, a conventional boost converter can be adopted to provide a step-up voltage gain with a large duty ratio. However, the conversion efficiency and step-up voltage gain are limited due to the losses of power switch and diode, equivalent series resistance (ESR) of the inductor and capacitor, and reverse-recovery problem of the diode [16], [17]. Therefore, a step-up converter with a reasonable duty ratio is required to achieve high efficiency and high voltage gain.

The converters adopting the transformer, such as flyback, forward, push–pull, half-bridge, and full-bridge types, can be used to obtain high voltage gain by adjusting the turns ratio of the transformer [18]–[31]. Among them, the flyback converter is very widely used in low power applications due to the simple structure which results from single switch, diode, and transformer. However, the primary switch and secondary diode suffer from high voltage stress due to the leakage inductance of the transformer. This limits the use of flyback converter for higher power application.

To relieve the aforementioned problem, one nonisolated single-switch high step-up converter is derived using a clamping diode and voltage doubler structure, based on the conventional flyback converter. Also, to further reduce the voltage stresses of semiconductors, another single-switch high step-up converter is proposed, simply by using one additional capacitor. This paper provides derivation and analysis, including operational principles, features, and design considerations. Finally, it is confirmed that the proposed single-switch converter has higher efficiency under entire load conditions due to the low voltage stress.

II. Derivation and Analysis of Nonisolated Single-Switch High Step-Up Converter

A. Topology Derivation

To achieve high step-up voltage gain, the flyback converter can be used among many transformer-adopted converters in low-power application. Fig. 1 shows the topology derivation of nonisolated single-switch high step-up converter with clamping diode based on the flyback converter. As shown in Fig. 1(a), the flyback converter has simple structure; however, the primary switch and secondary diode can have the high voltage stresses due to the resonance between the leakage inductance of the transformer and the parasitic capacitance of the semiconductors. To reduce the voltage stress on the diode, the voltage doubler rectifier can be adopted as shown in Fig. 1(b). The voltage stresses on the diodes is clamped to the output voltage V_O. Also, the voltage stress on the primary switch can be limited to V_D by using the clamping diode D_P and connecting the primary and secondary ground. Thus, a nonisolated single-switch high step-up converter with low voltage stress can be derived as shown in Fig. 1(c).

Manuscript received September 30, 2013; revised January 14, 2014; accepted March 31, 2014. Date of publication April 9, 2014; date of current version October 15, 2014. This paper was presented in part at the 8th International Conference on Power Electronics—ECCE Asia, Jeju, Korea, 2011. Recommended for publication by Associate Editor D. Vinnikov.

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Digital Object Identifier 10.1109/TPEL.2014.2316324

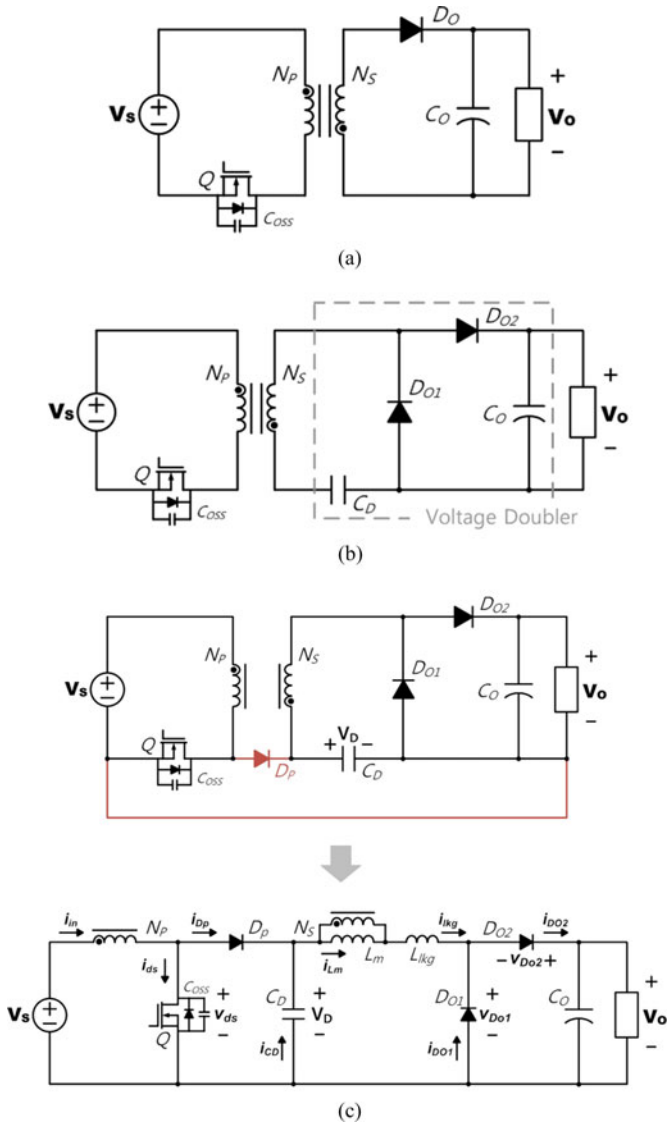

Fig. 1. Topology derivation. (a) Flyback converter. (b) Flyback converter with voltage doubler. (c) Nonisolated single-switch high step-up converter with clamping diode.

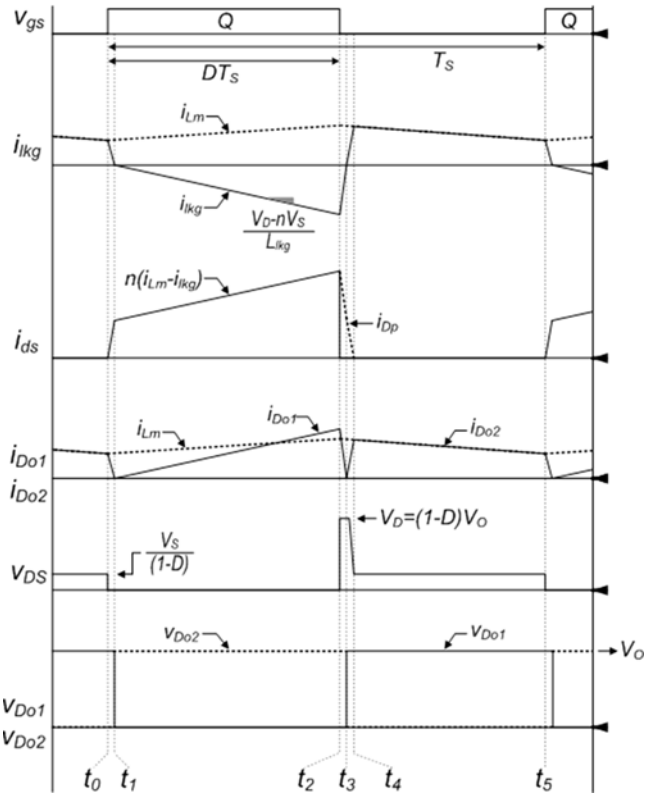

Fig. 2. Key waveforms of the nonisolated single-switch high step-up converter in Fig. 1(c).

B. Operational Principle

Fig. 2 shows the key operating waveforms of the nonisolated single-switch high step-up converter in Fig. 1(c). Each switching period is subdivided into five modes and their operational modes are shown in Fig. 3. The switch Q is operated in a duty ratio of D and in order to illustrate the steady-state operation, several assumptions are made as follows:

1) all parasitic components except for those specified in Fig. 1(c) are neglected;
2) the parasitic capacitance C_{OSS} of the switch Q is small enough;
3) the output voltage V_O and capacitor voltage V_D are constant during a switching cycle;
4) the transformer turns ratio $n = N_S/N_P$.

Mode 1 $[t_0 - t_1]$*:* In mode 1, the switch Q is turned on. The leakage current $i_{lkg}(t)$ decreases with the slope of $(V_D - nV_S - V_O)/L_{lkg}$ and the difference between the magnetizing current $i_{Lm}(t)$ and the leakage current is reflected to the primary current $i_{\rm in}(t)$. $i_{lkg}(t), i_{Lm}(t)$, and $i_{\rm in}(t)$ can be expressed as follows:

$$i_{lkg}(t) = \frac{V_D - nV_S - V_O}{L_{lkg}}(t - t_0) + i_{lkg}(t_0) \quad (1)$$

$$i_{Lm}(t) = \frac{nV_S}{L_m}(t - t_0) + i_{Lm}(t_0) \quad (2)$$

$$i_{in}(t) = n\left(i_{Lm}(t) - i_{lkg}(t)\right) \quad (3)$$

where

$$i_{lkg}(t_0) = i_{Lm}(t_0) = \left(\frac{D^2(nV_S - V_D)}{L_{lkg}(1-D)} - \frac{nDV_S}{L_m}\right)\frac{T_S}{2}.$$

Mode 2 $[t_1 - t_2]$*:* This mode begins when $i_{lkg}(t)$ reaches 0 A. The diode D_{O1} is turned on, and the leakage current flows through it. The diode D_{O2} is turned off, and its voltage stress is clamped to the output voltage V_O. The leakage current $i_{lkg}(t)$ charges the capacitor C_D and can be expressed as follows:

$$i_{lkg}(t) = \frac{V_D - nV_S}{L_{lkg}}(t - t_1). \quad (4)$$

Mode 3 $[t_2 - t_3]$*:* This mode begins when the switch Q is turned off. The clamping diode D_P is turned on, and the voltage stress on the switch is clamped to V_D. The leakage current increases, and the difference between the magnetizing current $i_{Lm}(t)$ and the leakage current is reflected to the primary side through the diode D_P. $i_{lkg}(t)$ and $i_{Lm}(t)$ can be expressed as

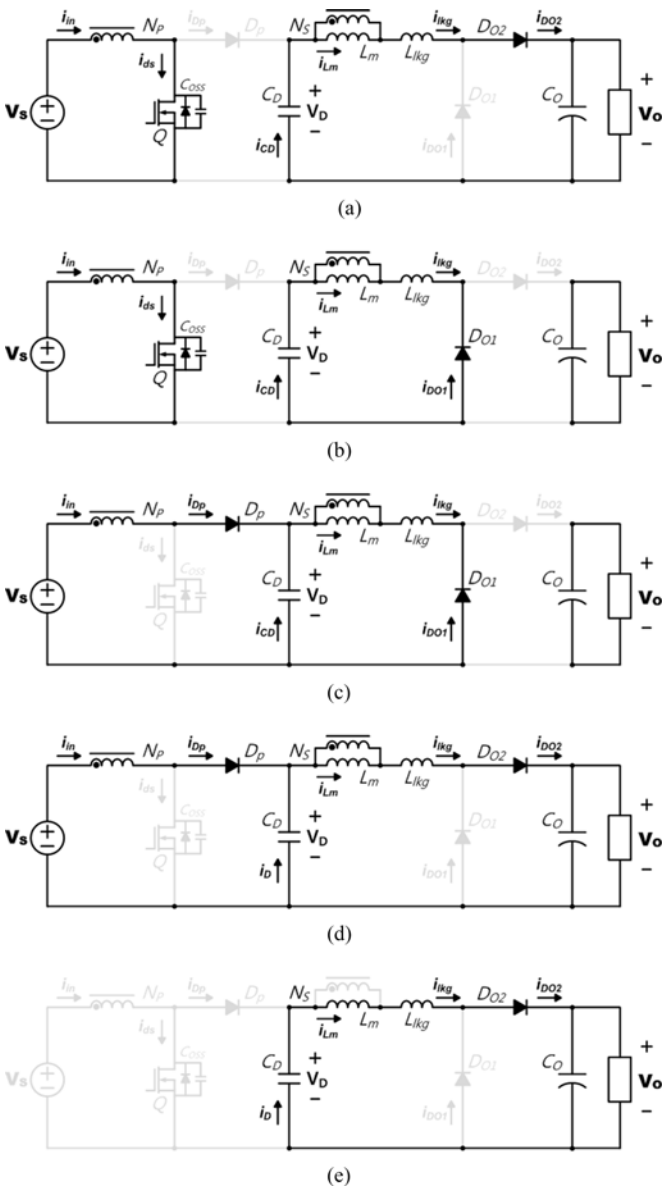

Fig. 3. Operational modes of the nonisolated single-switch high step-up converter in Fig. 1(c). (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (Gray line means nonconducting device.)

follows:

$$i_{lkg}(t) = \frac{n(V_D - V_S) + V_D}{L_{lkg}}(t - t_2) + i_{lkg}(t_2) \quad (5)$$

$$i_{Lm}(t) = \frac{n(V_S - V_D)}{L_m}(t - t_2) + i_{Lm}(t_2) \quad (6)$$

where

$i_{Lm}(t_2) = \frac{nV_S}{L_m}DT_S + i_{lkg}(t_0)$.

Mode 4 [$t_3 - t_4$]: This mode begins when $i_{lkg}(t)$ reaches 0 A. The diode D_{O2} is turned on, and the leakage current flows through it. The diode D_{O1} is turned off, and its voltage stress is clamped to the output voltage V_O. The leakage current $i_{lkg}(t)$ discharges the capacitor C_D and can be expressed as follows:

$$i_{lkg}(t) = \frac{n(V_D - V_S) + V_D - V_O}{L_{lkg}}(t - t_3). \quad (7)$$

Mode 5 [$t_4 - t_5$]: Mode 5 begins when $i_{lkg}(t)$ reaches the magnetizing current $i_{Lm}(t)$, which flows through the diode D_{O2}. Thus, there is no current flowing in the primary side. This mode ends when the switch is turned on.

C. Analysis and Characteristics

To simplify the following analysis, the ripple of the magnetizing inductor current $i_{Lm}(t)$ and the time intervals $t_0 - t_1$ and t_2-t_4 are neglected.

The capacitor voltage V_D can be obtained by the voltage–second balance on the secondary side of the transformer as follows:

$$V_D = (1 - D)V_O. \quad (8)$$

The magnetizing offset current I_{Lm} can be derived by the current–second balance on the capacitor C_D as follows:

$$I_{Lm} = \frac{D^2T_S(nV_S - V_D)}{2L_{lkg}(1 - D)}. \quad (9)$$

Since the average current of D_{O2} is the same as that of the load current I_O, this relation can be expressed as follows:

$$I_O = \frac{V_O}{R_O} = I_{Lm}(1 - D) = \frac{D^2T_S(nV_S - V_D)}{2L_{lkg}}. \quad (10)$$

From (8) and (10), the voltage conversion ratio M can be obtained as follows:

$$M = \frac{V_O}{V_S} = \frac{nD^2}{Q + (1 - D)D^2}, \qquad Q = \frac{2L_{lkg}}{R_OT_S}. \quad (11)$$

From (8) and (11), V_D is expressed as nV_S, with $Q = 0$. At given specifications, to reduce the voltage stress on the switch, the turns ratio should be designed as small as possible. This means that the duty ratio should be designed to be large enough. However, the much larger duty ratio results in the larger input root-mean-square (rms) current $i_{\text{in\_rms}}$ due to the high magnetizing offset current from (10), I_{Lm}=I_O/(1 – D). Also, it is difficult to obtain the desired voltage stress, especially in high step-up applications, because of the limited duty ratio less than 1. In the following section, a new nonisolated single-switch high step-up converter is presented to further reduce the voltage stresses on the switch and diodes.

III. Derivation and Analysis of Proposed Converter

A. Topology Derivation

Fig. 4 shows the topology derivation of the proposed converter from the converter in Fig. 1(c). The doubler capacitor C_D, as shown in Fig. 4(a), acts as clamping voltage source for the switch and voltage doubler capacitor, simultaneously. Although the C_D might be shown in boost output capacitor, the voltage of C_D is not dependent on the boost converter gain, but the voltage

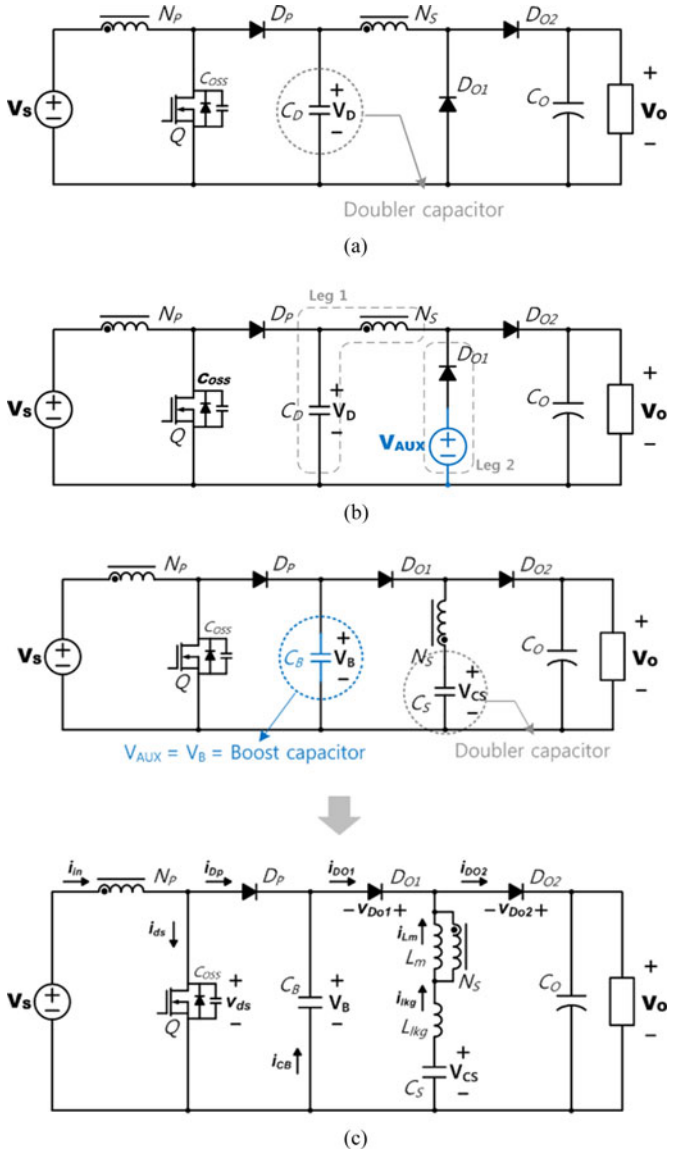

Fig. 4. Topology derivation. (a) Converter in Figs. 1(c). (b) and (a) With an additional voltage source V_{AUX}. (c) Proposed converter.

doubler value $V_D{=}(1-D)V_O$, as analyzed in Section II. To further reduce the voltage stresses on the semiconductors from Fig. 4(a), an auxiliary voltage source V_{AUX} is added, as shown in Fig. 4(b). V_{AUX} can be connected with D_{O1} simply to reduce the voltage stresses on diodes V_O-V_{AUX}. Furthermore, if V_{AUX} is used for the boost output voltage, the switch can have lower voltage stress, which results from the gain of boost converter. That is, the leg 1 composing of D_{O1} and V_{AUX} is replaced with the leg 2 composing of N_S and C_D, as shown in Fig. 4(c). Therefore, the capacitor C_B acts as a boost capacitor with the output voltage of the boost converter, $V_S/(1-D)$ to which the switch is clamped. Also, the output diodes are clamped to $V_O - V_B$ in the proposed converter. Thus, low-voltage-rated devices can be used to reduce the conduction loss. The voltage stresses on the devices will be analyzed in more detail in the following section.

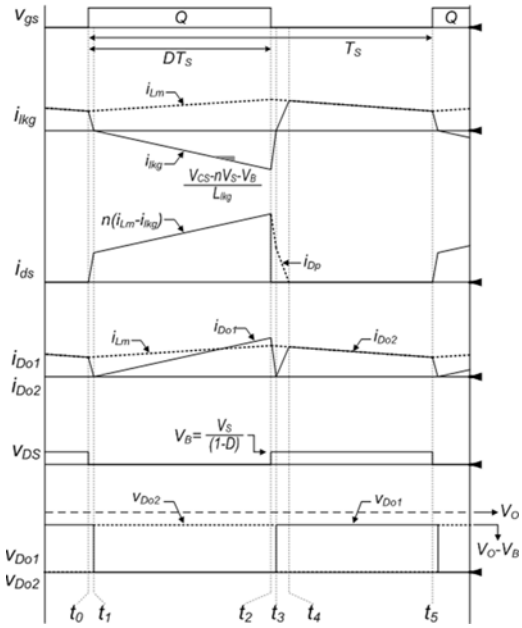

Fig. 5. Key waveforms of the proposed converter.

B. Operational Principle

Fig. 5 shows the key operating waveforms of the proposed converter. Each switching period is subdivided into five modes and their operational modes are shown in Fig. 6. The switch Q is operated in a duty ratio of D and in order to illustrate the steady-state operation, several assumptions are made as follows:

1) all parasitic components except for those specified in Fig. 4(c) are neglected;
2) the parasitic capacitance C_{OSS} of the switch Q is small enough;
3) the output voltage V_O and capacitor voltages V_B and V_{CS} are constant during a switching cycle;
4) the transformer turns ratio $n = N_S/N_P$.

Mode 1 [$t_0 - t_1$]: In mode 1, the switch Q is turned on. The leakage current $i_{lkg}(t)$ decreases with the slope of $(V_{CS} - nV_S - V_O)/L_{lkg}$ and the difference between the magnetizing current $i_{Lm}(t)$ and the leakage current is reflected to the primary current $i_{\mathrm{in}}(t)$. $i_{lkg}(t), i_{Lm}(t)$, and $i_{\mathrm{in}}(t)$ can be expressed as follows:

$$i_{lkg}(t) = \frac{V_{CS} - nV_S t - V_O}{L_{lkg}}(t - t_0) + i_{lkg}(t_0) \quad (12)$$

$$i_{Lm}(t) = \frac{nV_S}{L_m}(t - t_0) + i_{Lm}(t_0) \quad (13)$$

$$i_{in}(t) = n\left(i_{Lm}(t) - i_{lkg}(t)\right) \quad (14)$$

where

$i_{lkg}(t_0) = i_{Lm}(t_0) = \left(\frac{D^2(nV_S + V_B - V_{CS})}{L_{lkg}(1-D)} - \frac{nDV_S}{L_m}\right)\frac{T_S}{2}$.

Mode 2 [$t_1 - t_2$]: This mode begins when $i_{lkg}(t)$ reaches 0 A. The diode D_{O1} is turned on and the leakage current flows through it. The diode D_{O2} is turned off and its voltage stress is clamped to $V_O - V_B$. The leakage current $i_{lkg}(t)$

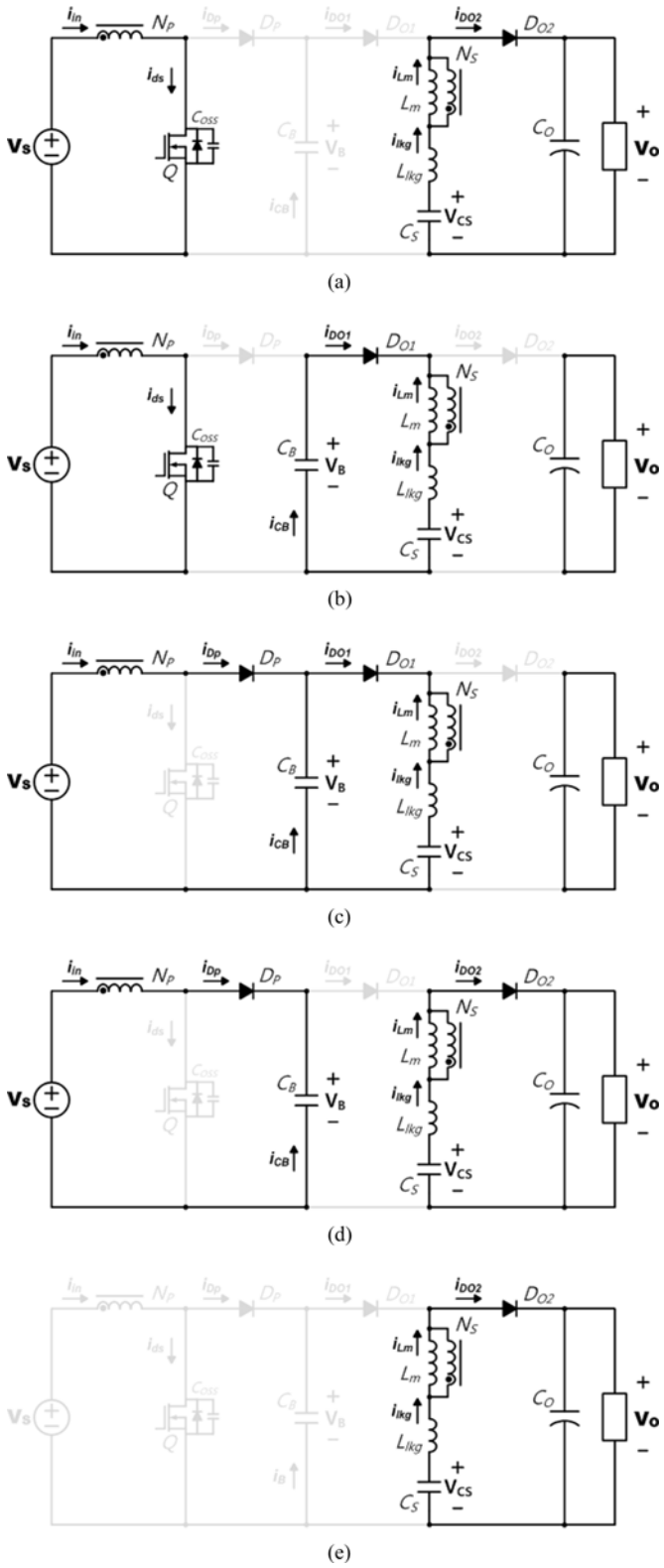

Fig. 6. Operational modes of the proposed converter. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (Gray line means nonconducting device.)

charges the capacitor C_S and can be expressed as follows:

$$i_{lkg}(t) = \frac{V_{CS} - nV_S - V_B}{L_{lkg}}(t - t_1). \tag{15}$$

Mode 3 [$t_2 - t_3$]: This mode begins when the switch Q is turned off. The clamping diode D_P is turned on, and the voltage stress on the switch is clamped to V_B. The leakage current increases and the difference between the magnetizing current $i_{Lm}(t)$, and the leakage current is reflected to the primary side through the diode D_P. $i_{lkg}(t)$ and $i_{Lm}(t)$ can be expressed as follows:

$$i_{lkg}(t) = \frac{n(V_B - V_S) + V_{CS} - V_B}{L_{lkg}}(t - t_2) + i_{lkg}(t_2) \tag{16}$$

$$i_{Lm}(t) = \frac{n(V_S - V_B)}{L_m}(t - t_2) + i_{Lm}(t_2) \tag{17}$$

where

$i_{Lm}(t_2) = \frac{nV_S}{L_m}DT_S + i_{lkg}(t_0)$.

Mode 4 [$t_3 - t_4$]: This mode begins when $i_{lkg}(t)$ reaches 0 A. The diode D_{O2} is turned on and the leakage current flows through it. The diode D_{O1} is turned off, and its voltage stress is clamped to $V_O - V_B$. The leakage current $i_{lkg}(t)$ discharges the capacitor C_S and increases more slowly unlike the converter in Fig. 1(c). This is because the voltage stress on the capacitor C_B is lower than that on the capacitor C_D in Fig. 1(c). $i_{lkg}(t)$ can be expressed as follows:

$$i_{lkg}(t) = \frac{n(V_C - V_S) + V_{CS} - V_O}{L_{lkg}}(t - t_3). \tag{18}$$

Mode 5 [$t_4 - t_5$]: Mode 5 begins when $i_{lkg}(t)$ reaches the magnetizing current $i_{Lm}(t)$, which flows through the diode D_{O2}. Thus, there is no current flowing in the primary side. This mode ends when the switch is turned on.

C. Analysis and Characteristics

To simplify the following analysis, the ripple of the magnetizing inductor current $i_{Lm}(t)$ and the time intervals $t_0 - t_1$ and $t_2 - t_4$ are neglected.

1) Voltage Conversion Ratio: In the proposed converter, by inserting the capacitor C_B, V_B can have the boost output voltage $V_S/(1-D)$. This is because the capacitor C_S serves as a doubler capacitor instead of C_B. The capacitor voltage V_{CS} can be obtained by the voltage–second balance on the secondary side of the transformer as follows:

$$V_{CS} = (1 - D)V_O + DV_B. \tag{19}$$

The capacitor voltage V_{CS} is larger than V_B in the converter in Fig. 1(c). The difference is $DV_S/(1-D)$.

The magnetizing offset current I_{Lm} can be derived by the current–second balance on the capacitor C_S as follows:

$$I_{Lm} = \frac{D^2T_S(nV_S + V_B - V_{CS})}{2L_{lkg}(1 - D)}. \tag{20}$$

Since the average current of D_{O2} is same as the load current I_O, this relation can be expressed as follows:

$$I_O = \frac{V_O}{R_O} = I_{Lm}(1 - D) = \frac{D^2T_S(nV_S + V_B - V_{CS})}{2L_{lkg}}. \tag{21}$$

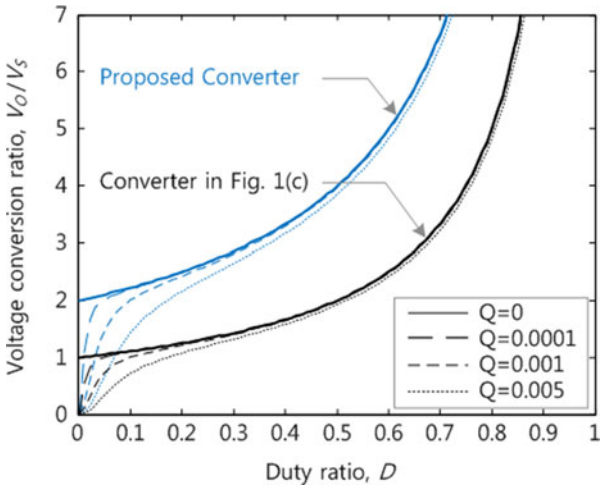

Fig. 7. Voltage conversion ratios at $n = 1$.

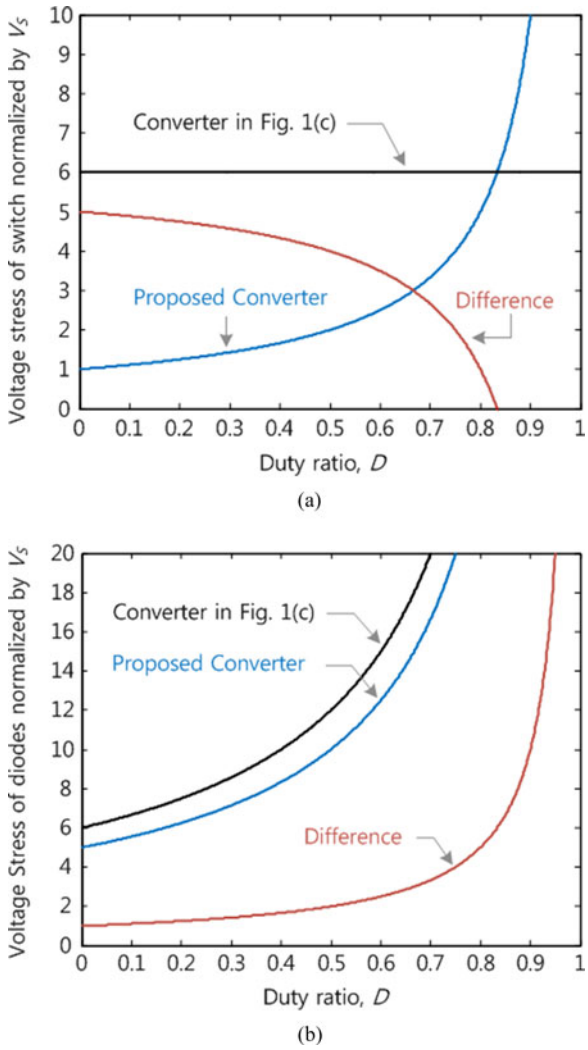

Fig. 8. Voltage stress on the switch and diodes. (a) Switch. (b) Diodes.

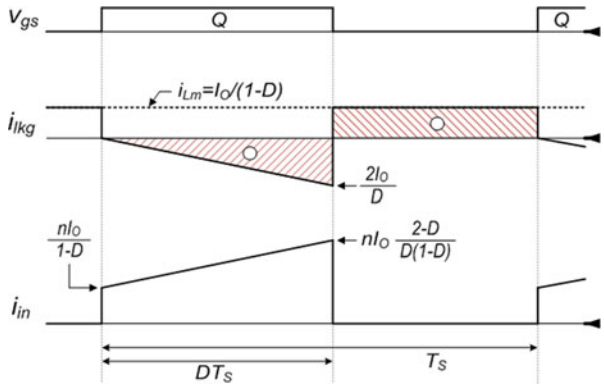

Fig. 9. Simplified current waveforms.

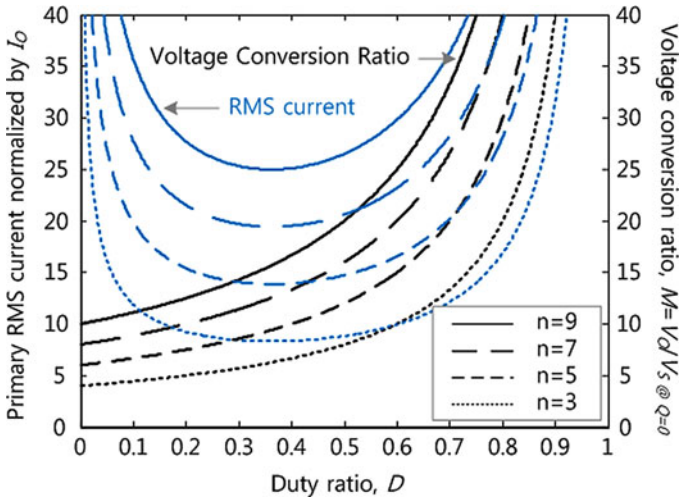

Fig. 10. Voltage conversion ratio and rms value of the primary current.

From (19) and (21), the voltage conversion ratio M can be obtained as follows:

$$M = \frac{V_O}{V_S} = \frac{D^2\,(n+1)}{Q + (1-D)\,D^2}\,, \qquad Q = \frac{2L_{lkg}}{R_O T_S}. \tag{22}$$

Fig. 7 shows the voltage conversion ratios with a function of the damping factor Q and the duty ratio D in the converter in Fig. 1(c) and proposed converter, assuming $n = 1$. As shown in Fig. 7, Q provides a damping effect to the gain curve. As Q is increased, which means L_{lkg}, f_S, and load current are increased, the voltage gain is reduced. Also, it is seen that the proposed converter has higher voltage gain with the same conditions. To have same conversion ratio, the turns ratio of the converter in Fig. 1(c) should be designed as n_c=$n_p + 1$ from (11) and (22), where n_c and n_p is turns ratio of the converter in Fig. 1(c) and proposed converter, respectively.

2) Voltage Stress on the Devices: With the assumption of $Q = 0$, $n_c = 6$, and $n_p = 5$, the voltage stresses on the switch and diodes normalized by V_S are shown in Fig. 8. As shown in Fig. 8(a), the voltage stress on the switch of the converter in Fig. 1(c) is same with the turns ratio n_c, and that of the proposed converter is same with the boost gain $1/(1 - D)$.

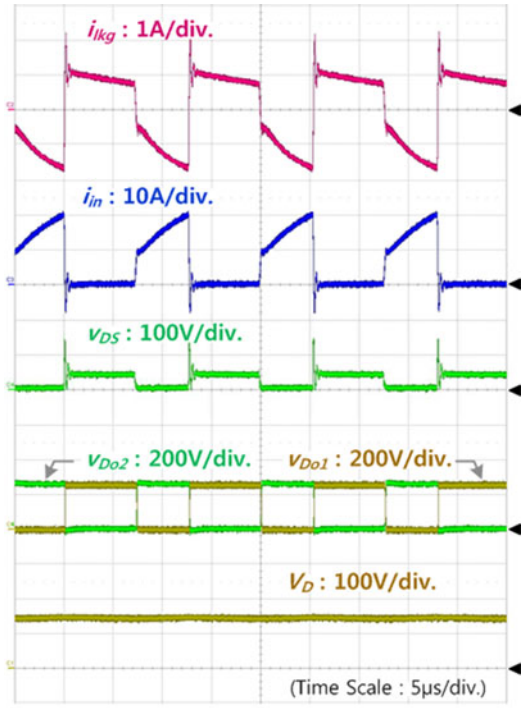

Fig. 12. (a) Key experimental waveforms and (b) dynamic response of the converter in Fig. 1(c).

TABLE I
COMPONENTS LIST

Components	Converter in Fig. 1(c)	Proposed Converter
Switching frequency (f_S)	80kHz	
Switch (Q)	FQA44N30	IRFP150N
Clamping Diode (D_P)	STTH40P03S	STPS40M100C
Doubler Diode (D_{O1}, D_{O2})	BYV29-400	BYV29-300
Transformer	PQ3230	
Leakage inductance (L_{lkg})	32.14μH	28.15μH
Magnetizing inductance (L_m)	2.16mH	1.31mH
Transformer turns (N_P : N_S)	5 : 35	8 : 45
Capacitors (C_D, C_B, C_S)	2.2μF	
Output capacitor (C_O)	82μF	

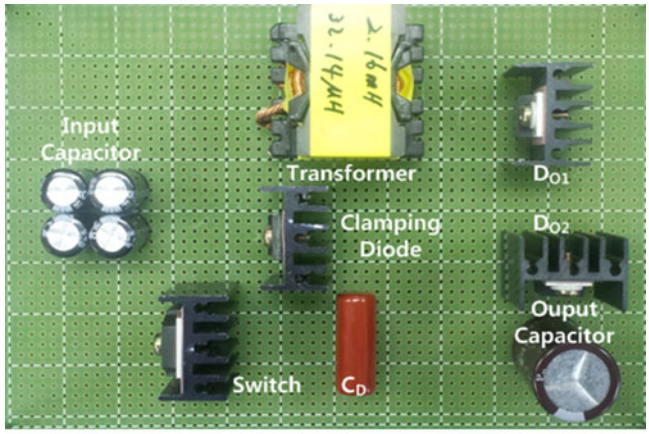

Fig. 11. Prototype photograph of (a) the converter in Figs. 1(c) and (b) the proposed converter.

In the region of $D < 0.83$, the switch in the proposed converter has lower voltage stress and the difference will be larger when D is getting small, especially in high step-up applications that requires very high turns ratio. Also, as shown in Fig. 8(b), the diodes in the proposed converter have lower voltage stress and as the duty ratio increases, the difference is larger.

IV. EXPERIMENTAL RESULTS

A. Design Guideline

In high step-up applications, the switch and primary winding of the transformer is the dominant factor of the conduction loss due to the high input current.

Fig. 9 shows the simplified waveforms of $i_{lkg}(t)$ and $i_{\rm in}(t)$. By using the current–second balance on C_S, the peak values are acquired as shown in Fig. 9. Thus, the rms value of the primary current $i_{{\rm in}\_rms}$ can be obtained as follows:

$$i_{in\_rms} = \frac{nI_O}{1-D}\sqrt{\frac{D}{3}\left\{\left(\frac{2-D}{D}+\frac{1}{2}\right)^2+\frac{3}{4}\right\}} \quad (23)$$

where $n{=}n_c = n_p + 1$.

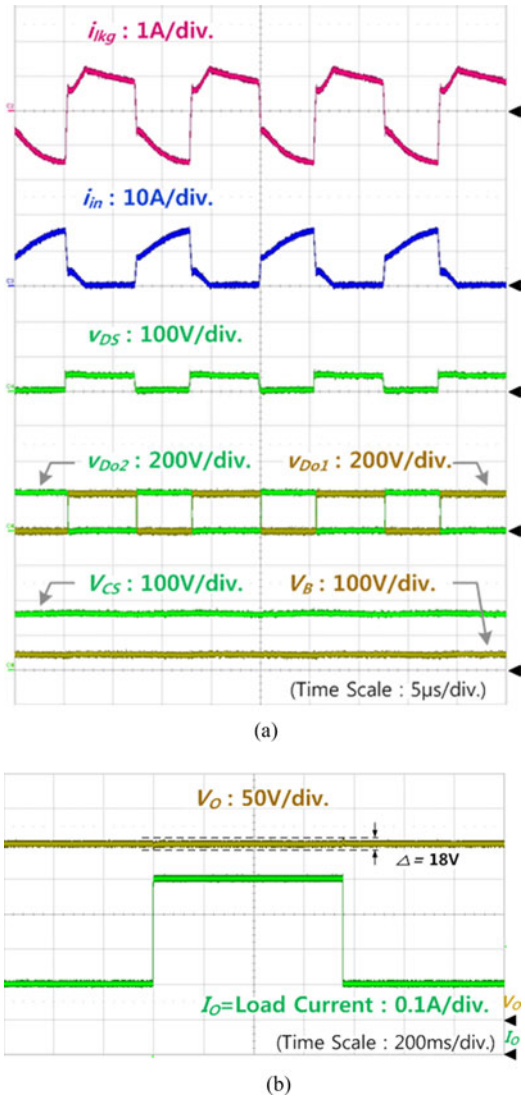

Fig. 13. (a) Key experimental waveforms and (b) dynamic response of the proposed converter.

Fig. 10 shows the voltage conversion ratio at $Q = 0$ and rms value of the primary current normalized by the load current I_O, according to the duty ratio D and turns ratio n. As shown in Fig. 10, the low rms values exist in the duty ratio range about from 0.3 to 0.4. In view of the conduction loss, the duty ratio D can be designed as small as possible to reduce the voltage stress on the switch. However, the switch has the small difference of the voltage stress about 34.2–40 V with the specification of a 24 V input and 250 V/125 W output. Also, the turns ratio should be increased with the smaller duty ratio. Thus, to utilize a 100 V switch with a sufficient margin, the duty ratio can be selected as about 0.4. The voltage gain M is about 10.42, so the turns ratios n_c and n_p of the transformers can be obtained as 6.252 and 5.252 from (11) and (22), respectively, assuming $Q = 0$.

B. Experimental Results

A 24 V input and 250 V/125 W output prototype has been built and tested to verify the operational principle, using the components as shown in Table I. Fig. 11 shows the prototype photograph of the converter in Fig. 1(c) and the proposed converter. Figs. 12 and 13 show the key experimental waveforms at full load condition and dynamic response between 100% and 40% load condition of the converter in Fig. 1(c) and the proposed converter, respectively. As shown in Fig. 12(a), the voltage stresses on the switches and diode D_p are about 140 V8∗∗ and those of the diodes D_{O1} and D_{O2} are the output voltage 250 V. On the other hand, in the proposed converter, the voltage stresses on the switches and diode D_p are about 40 V and those of the diodes D_{O1} and D_{O2} are about 210 V, as shown in Fig. 13(a). Figs. 12(b) and 13(b) show that the output voltage is regulated between 240 and 260 V under dynamic load conditions. Fig. 14 shows the measured efficiency of the converter in Fig. 1(c), the proposed converter, and the flyback converter. The proposed converter has higher efficiency under entire load conditions. This is mainly because the conduction loss can be reduced by using the low-voltage-rated devices.

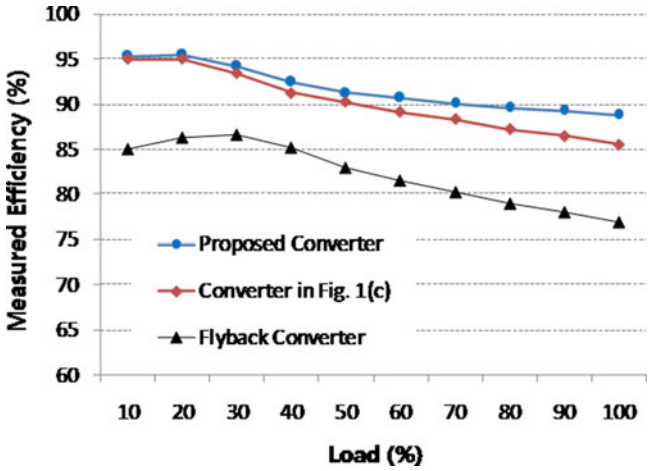

Fig. 14. Measured efficiency of the proposed converter, converter in Fig. 1(c), and flyback converter.

V. Conclusion

Nonisolated single-switch high step-up converters with low voltage stress are presented. The derivation and analysis are illustrated in this paper. The validity of the basic operational principle is verified by the experiment with 24 V input and 250 V/125 W output prototype. The proposed converter features that the switch and diodes have the low voltage stress, so the low-voltage-rated devices is used. From the experimental results, the proposed converter shows higher efficiency under entire load conditions due to the low conduction loss.

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