Analysis and Design of *LLC* Resonant Converters With Capacitor–Diode Clamp Current Limiting

Chi Wa Tsang, Martin P. Foster, David A. Stone, and Daniel T. Gladwin

***Abstract*—This paper presents a design methodology for *LLC* resonant converters with capacitor–diode clamp for current limiting in overload conditions. A new fundamental harmonic approximation-based equivalent circuit model is obtained through the application of describing function techniques, by examining the fundamental behavior of the capacitor–diode clamp. An iterative procedure to determine the conduction point of the diode clamp is also given. The behavior of this type of converter is analyzed and guidelines for designing the current limiting characteristics are discussed. The characterization of a 90 W converter design using the proposed methodology is presented. The converter voltage gain and the voltage–current characteristics under different overload conditions and operating frequencies are predicted using the proposed model, which accuracies are validated against the prototype with good correlation.**

***Index Terms*—Capacitor diode clamp, current limiting, *LLC* resonant converter.**

NOMENCLATURE

A	Resonant tank inductor ratio $(= L_p/L_s)$.
B	Capacitance sharing ratio.
C_s, C_c	Resonant tank capacitors.
C_r	Equivalent resonant capacitance (with inactive diode clamp).
f_s	Switching frequency.
$f_{s(\min)}$	Minimum switching frequency.
$f_{s(\max)}$	Maximum switching frequency.
f_0	Series resonant frequency.
f_n	Nominalized frequency $(f_n = f_s/f_0)$.
I_i	Input current.
$I_{o(\text{rate})}$	Maximum rated output current.
$I_{o(\text{over})}$	Overloading output current.
I_n	Normalized output current $\left(= I_{o(\text{over})}/I_{o(\text{rate})}\right)$.
k_i	Imaginary component used in $M_{g(\text{clmp})}$.
k_r	Real component used in $M_{g(\text{clmp})}$.
L_s, L_p	Resonant inductors.
LIP	Load independent point.
M_g	Normalized gain (with inactive diode clamp).
$M_{g(\max)}$	Maximum normalized gain (with inactive diode clamp).
$M_{g(\min)}$	Minimum normalized gain (with inactive diode clamp).
$M_{g(\text{clmp})}$	Normalized gain (with activated diode clamp).
n	Transformer turn ratio.
Q	Quality factor $\left(= \sqrt{L_s/C_r}/R_{\text{eq}}\right)$.
Q_{rate}	Q-factor at maximum rated load.
Q_{over}	Q-factor at overloading.
Q_n	Normalized Q-factor $(= Q_{\text{over}}/Q_{\text{rate}})$.
R	Real component of Z_c.
R_{l}	Load resistance.
R_{eq}	Equivalent load resistance.
s	Complex frequency $(= j\omega_{\text{s}})$.
t	Time.
T	Switching period.
V_c	Peak voltage across resonant capacitor C_c.
V_i	Input voltage.
$V_{i(\max)}$	Maximum input voltage.
$V_{i(\min)}$	Minimum input voltage.
V_o	Output voltage.
$V_{o(\text{rate})}$	Maximum rated output voltage.
$V_{o(\text{over})}$	Overloading output voltage.
V_n	Normalized output voltage $\left(= V_{o(\text{over})}/V_{o(\text{rate})}\right)$.
X	Imaginary component of Z_c.
Z_1	Resonant tank impedance (with inactive diode clamp).
Z_2	Resonant tank impedance (with activated diode clamp).
Z_c	Equivalent clamping capacitance impedance (with activated diode clamp).
α	Damping factor.
δ	Diode–clamp nonconduction angle.
ω_s	Angular switching frequency $(=2\pi f_s)$.
θ	Angle.

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I. INTRODUCTION

As electronic systems are miniaturized, power supply designers are placed under increasing pressure to reduce the size of their designs, imposing strict requirements on the chosen power supply topology, components, efficiency, and cooling requirements. Size reduction in hard switching converters (e.g., buck converters) can be achieved by increasing the switching frequency, which reduces the size of passive components. The drawback of this approach is the increase in switching losses, ultimately compromising converter efficiency. Resonant converters such as series resonant, parallel resonant, and multiresonant converters [1], [2] overcome this drawback by soft-switching,

where the switching devices are switched under zero voltage (ZVS) or zero current (ZCS). One variation of the multiresonant converter, the *LLC* resonant converter [3]–[12], [15]–[18], has become popular due to its narrow range of operating frequency for wide input voltage and load ranges [13], [14] when operated around the converter's (series) resonant frequency, also referred as the load independent point (LIP). The narrow frequency range is the result of the resonant tank components, L_s and C_r, becoming a virtual short-circuit (zero impedance) at the resonant frequency. The operating frequency is adjusted mainly to compensate for the change in the input voltage with only small adjustments to the frequency to compensate for changes in the load. Unfortunately, due to the low impedance around the LIP, excessive current can flow to the load during transient and overload conditions, and so a current protection mechanism must be included.

For *LLC* resonant converters, current-limiting can be achieved by 1) reducing the MOSFET conduction times, 2) increasing the switching frequency [19], [20], 3) operating at a subharmonic of the switching frequency [21], or 4) by changing the resonant frequency characteristics of the converter by switching in (or out) the resonant tank components [19], [20], [22]–[25]. Although methods (1) to (3) provide adequate protection, a current sensor is needed to detect the overload condition and some action by the controller is required to adjust the MOSFET timings. Method (4), in contrast, does not necessarily require any direct action to be taken by the controller assuming an appropriate circuit can be developed. By way of example, the *LLC* resonant converter presented in [19], [20], and [24] the resonant capacitor is split and connected to the dc-link supply with the common point connected to the resonant circuit. Since diodes are connected in antiparallel across the capacitors when excessive voltages exist across the capacitors the diodes are forced into conduction clamping the capacitor voltages and, hence, allowing a reduction the output current during an overload condition. The advantage of this scheme is that the current limiting occurs as soon as the overcurrent condition appears and is performed autonomously without the need for any feedback mechanism. Although a practical circuit was presented, very little information regarding the behavior of a converter was included. A variation to the capacitor–diode clamp was presented in [25], where, instead of splitting the capacitor and fixing the clamping voltage to the input rail, the capacitor voltage is clamped to the output voltage through a transformer allowing the clamping voltage to be more readily specified and hence allowing the desired current-limiting performance to be obtained. Although a detailed analysis was presented, this scheme requires a controller for the current-limiting, similar to that in methods (1) to (3).

Here, the resonant capacitor of an *LLC* converter is split into clamped and nonclamped portions to allow the desired current limiting performance to be obtained. A fundamental harmonic approximation (FHA)-based equivalent circuit model, which is based on the procedures we presented in [26], is derived for the converter to predict the current limiting characteristic under overloading. The converter characteristics under overload condition is analyzed, a design methodology is described and is used to design a 90 W converter. Experimental measurements taken from a prototype converter validate both the model and design methodology.

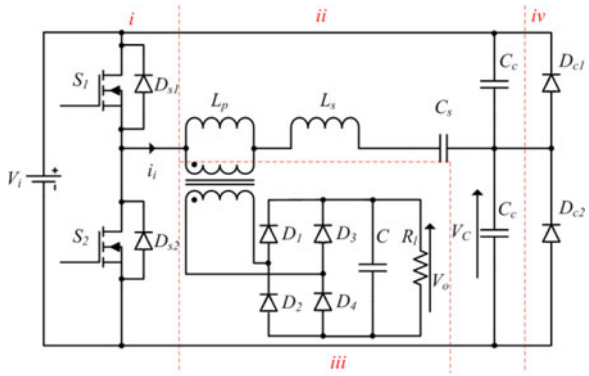

Fig. 1. Half-bridge *LLC* resonant converter with capacitor–diode clamp.

The paper is organized as followed: Section II gives details of the converter and its operation with and without the diode clamp. Section III describes the derivation of the FHA equivalent circuit models and the nominalized gains of the converter under the difference diode–clamp conduction states. Section IV investigates the converter overloading characteristics with the different clamping capacitance. A prototype converter is designed in Section V, and experimental results are compared with the prediction by the model. Section VI concludes the findings of the work.

II. Circuit Operation

A half-bridge *LLC* resonant converter with the proposed capacitor–diode clamp is shown in Fig. 1. It consists of four main functional parts: 1) a dc chopper formed by two complementary switched MOSFETs S_1 and S_2, converting the dc input voltage, V_i, into a square waveform (n.b. D_{s1} and D_{s2} are the body diodes of the MOSFETs which are critical for ZVS), 2) a resonant tank formed by resonant inductors and capacitors L_p, L_s, C_c, and C_s allowing the fundamental component of the square waveform to pass through, 3) transformer, bridge rectifier, and output filter formed by diodes $D_1 - D_4$ and capacitor C, converting the ac waveform produced in (2) into the isolated dc output, and 4) diodes D_{c1} and D_{c2} which clamp the voltage, V_C, to the input voltage rail for current-limiting purpose.

Under normal operation (i.e., below the current limit), the voltage V_C operates within the two clamping voltage levels, 0 and V_i, as shown in Fig. 2(a). The clamping diodes D_{c1} and D_{c2} do not conduct during the switching period and hence, the circuit can be simplified to Fig. 3(a), thus the two capacitors, C_c, are effectively connected in parallel such that $2C_c$ is connected in series with C_s which together form the resonant capacitor C_r found in the standard *LLC* resonant converter. With these capacitors, C_s can be found by

$$C_s = \frac{2C_cC_r}{2C_c - C_r}. \tag{1}$$

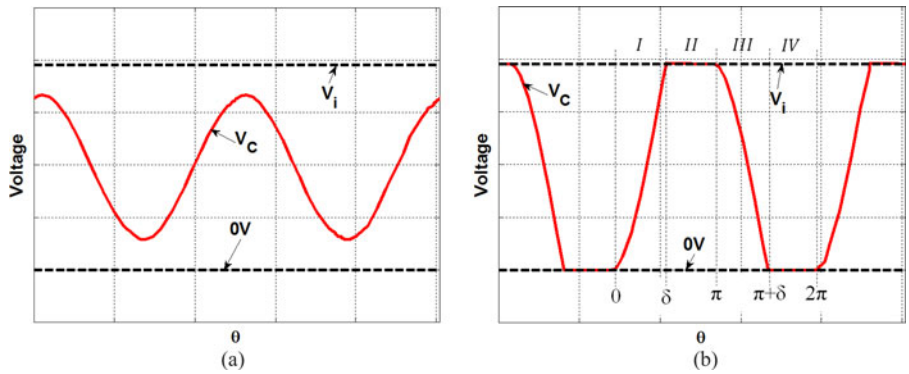

Fig. 2. Resonant capacitor voltage waveforms. (a) Normal operation and (b) overloading operation.

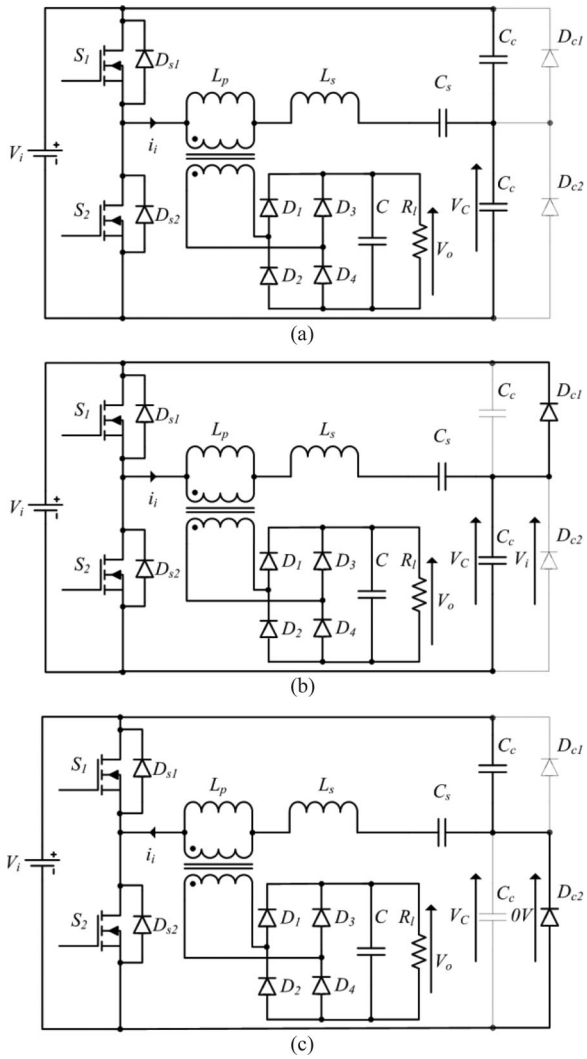

Fig. 3. Equivalent circuit under different diode–clamp conduction states. (a) non-conduction, or $\pi < \theta \leq \pi + \delta$ (b) conduction state 1, $\delta < \theta \leq \pi$, and (c) conduction state 2, $\pi + \delta < \theta \leq 2\pi$.

The range of C_s, and hence C_c, is controlled by the capacitance sharing ratio B as given in (2). This can take on values in the range $0 \leq B \leq 1$, with $B = 1$ being the extreme where no capacitance is clamped by the diode D_{c1} and D_{c2} and $B = 0$ being where the whole resonant capacitor is clamped. The effect of the capacitor ratio B to the current limiting performance will be detailed in Section IV

$$B = \frac{C_r}{C_s}. \tag{2}$$

Under overload conditions (i.e., the predesigned load current is exceeded) V_C exceeds the input voltage rail for some portion of the switching period causing D_{c1} and D_{c2} to conduct momentarily and so clamping V_C to the voltage rails. Since V_C is constant during the clamping intervals, capacitors C_c do not participate in the resonance which, from an FHA perspective, is equivalent to an increase of the capacitor values. The effect of this is to reduce the resonant frequency of the tank and so there is an apparent increase in the switching frequency to resonant frequency ratio $(f_n = f_s/f_0)$, thereby reducing the current flow in the circuit. The conduction state for each diode can be determined as follows:

1 D_{c1} conducts when $V_C > V_i$, clamping the V_C to V_i.

2 D_{c2} conducts when $V_C < 0$ V, clamping the V_C to 0 V.

In either case, the clamping diode ceases conduction when the resonant circuit input current $I_i = 0$ A. Thus, V_c takes on a cosinsoidal shape otherwise assuming the resonant circuit current is sinusoidal. The quasi cosine-square waveform of V_C under current-limited operating conditions is shown in Fig. 2(b), with the diode conduction states (1) and (2) found in intervals II and IV, respectively, and nonconduction states in intervals I and III indicated on the graph. The circuits for the converter with D_{c1} and D_{c2} conducting are shown in Figs. 3(b) and (c), respectively.

III. Equivalent Circuit Model

When the diode clamp is inactive, the converter static behavior can be predicted using a variety of methods, including FHA [27], describing function [28] and state-plane techniques [29] depending on the required modeling accuracy. Although the methods presented in [28] and [29] can predict the static behaviors more accurately across the wide range of switching frequencies, they can be difficult to use when multiple operating modes are encountered and therefore the equivalent circuit models derived here are based on FHA which has been shown to provide reasonable prediction accuracy when the converter is operating in the vicinity of the LIP [30].

With FHA one assumes the resonant current can be approximated to a sinusoidal current since the resonant circuit operates similar to a band-pass filter responding only to the fundamental component of the input voltage and attenuating the higher frequency components. With this assumption, the input current i_i can be defined as in (3), with a peak value of I_i when the converter is operating at a frequency of f_s. To simplify the analysis that follows, angles are again used to remove the time dependences such that $2\pi f_s t = \theta$:

$$i_i = I_i \sin(\omega_s t) = I_i \sin(2\pi f_s t) = I_i \sin(\theta). \tag{3}$$

A. Diode–Clamp Inactive

By FHA techniques similar to those applied in [1] and [27], the magnitude of the input current (I_i) and output voltage (V_o) can be calculated using (4) and (5), respectively, (n.b. in the following analysis, the nonideality of diodes and of components parasitic resistances are neglected)

$$I_i = \frac{2V_i}{\pi Z_1} \tag{4}$$

$$V_o = \frac{\pi I_i \left(R_{\rm eq} || sL_p\right)}{4n} \tag{5}$$

where $Z_1 = R_{\rm eq}||sL_p + sL_s + 1/(sC_s) + 1/(2sC_c)$, is the input impedance of the resonant circuit and the load, $s = j\omega_s$, is the complex frequency and $R_{\rm eq} = \left(8n^2 R_l\right)/\pi^2$ is the equivalent resistance presented by the rectifier, output filter and load reflected through a transformer with a primary to secondary turn ratio n.

In order to study the converter's general behavior, irrespective of the resonant tank components selection, the nominalized gain M_g is commonly obtained. This is obtained by substituting (4) into (5), and rearranging in terms of $(2nV_o)/V_i$, then normalizing against the three parameters, inductor ratio $A = L_p/L_s$, loaded quality factor $Q = \sqrt{L_s/C_r}/R_{\rm eq}$ and normalized switching frequency (against the series resonant frequency) $f_n = f_s/f_o$. The result is given in

$$M_g = \frac{2nV_o}{V_i} = \frac{Af_n^2}{Af_n^2 + f_n^2 - 1 + j(f_n^3 QA - f_n QA)}. \tag{6}$$

With the capacitor C_c excited by the sinusoidal input current, its voltage as shown in Fig. 2(a), at any given instant can be found by (7). Substituting $\omega_s t$ for θ (where $\omega_s = 2\pi f_s$ being the angular switching frequency and t is time), the capacitor branch voltage v_c at any θ can also be found by (8)

$$v_C(t) = \frac{1}{2C_c} \int I_i \sin(\omega_s t)\, dt = -\frac{I_i}{2\omega_s C_c} \cos(\omega_s t) + V_n \tag{7}$$

$$v_C(\theta) = -\frac{I_i}{2\omega_s C_c} \cos(\theta) + V_n \tag{8}$$

where V_n is the initial condition for a given conduction state starting at $\theta = n$.

Due to the dc blocking property of capacitors, the dc component of the dc chopper (half-bridge) is superimposed onto v_c as in

$$v_C(\theta) = -\frac{I_i}{2\omega_s C_c} \cos(\theta) + \frac{V_i}{2}. \tag{9}$$

B. Diode–Clamp Activate

In this section, a describing function is developed to represent the effects of the diode–clamp/capacitor combination by an equivalent impedance Z_c. This impedance is then combined with an FHA analysis similar to that described in the previous section providing a complete model of the converter when the diode clamp is active (i.e., overload condition). The derivation of Z_c is given in the three steps as follows.

Step 1: A piecewise equation describing the capacitor voltage v_c [see Fig. 2(b)] representing the circuit conduction states is obtained assuming a sinusoidal resonant current.

Since there are two intervals during a single cycle when the diode clamp is inactive, two separate values for the initial condition V_n are needed to be found. In interval I $(0 < \theta \leq \delta)$, the capacitor voltage, v_c, is zero at the beginning, by substituting the known quantities in (8), the initial condition is found in

$$0 = -\frac{I_i}{2\omega_s C_c} \cos(0) + V_0$$

$$V_0 = \frac{I_i}{2\omega_s C_c}. \tag{10}$$

For the interval III $(\pi < \theta \leq \pi + \delta)$, v_c has been charged to V_i and now begins discharging toward 0 V. By applying similar arguments as before, the initial condition for this interval is also found in

$$V_i = -\frac{I_i}{2\omega_s C_c} \cos(\pi) + V_\pi$$

$$V_\pi = V_i - \frac{I_i}{2\omega_s C_c}. \tag{11}$$

Combining the initial conditions found in (10) and (11) with (8) and accounting for the two clamping levels, the piecewise description of the capacitor voltage is given in

$$v_{\rm C}(\theta) = \begin{cases} \dfrac{I_i}{2\omega_s C_c}(1 - \cos(\theta)) & 0 < \theta \leq \delta \\ V_i & \delta < \theta \leq \pi \\ V_i - \dfrac{I_i}{2\omega_s C_c}(1 + \cos(\theta)) & \pi < \theta \leq \pi + \delta \\ 0 & \pi + \delta < \theta \leq 2\pi \end{cases} \tag{12}$$

The diode–clamp nonconduction angle, δ, is found by evaluating the change in capacitor voltage over the diode–clamp nonconduction period. At the end of the first interval, the capacitor voltage has charged to V_i, therefore, substituting $v_{\rm C}(\delta) = V_i$ into (12) and rearranging provides

$$\delta = \cos^{-1}\left(1 - \frac{2\omega_s C_c V_i}{I_i}\right). \tag{13}$$

Step 2: The fundamental component of v_c is determined via Fourier analysis.

A describing function for v_c is now developed based on the piecewise equation that has just been developed. The Fourier series representation of a repetitive waveform is defined in (14) where $f(t)$ is the original time-domain signal $v_c(t)$, a_0 is the dc component, a_n and b_n are harmonic components of the

waveform and T is the period of one cycle

$$\begin{aligned} f(t) &= a_0 + \sum_{n-1}^{\infty} \left(a_n \cos(n\omega_s t) + b_n \sin(n\omega_s t)\right) \\ a_0 &= \frac{1}{2\pi} \int_{-T/2}^{T/2} f(t)\, dt \\ a_n &= \frac{1}{\pi} \int_{-T/2}^{T/2} f(t) \cos(n\omega_s t)\, dt \\ b_n &= \frac{1}{\pi} \int_{-T/2}^{T/2} f(t) \sin(n\omega_s t)\, dt. \end{aligned} \tag{14}$$

For ac equivalent circuit analysis, the dc component, a_0, is ignored and since the converter's behavior is dominated by the fundamental component, the Fourier series can be simplified to a describing function as shown

$$\begin{aligned} f(\theta) &= a_1 \cos(\theta) + b_1 \sin(\theta) \\ a_1 &= \frac{1}{\pi} \int_0^{2\pi} f(\theta) \cos(\theta)\, d\theta \\ b_1 &= \frac{1}{\pi} \int_0^{2\pi} f(\theta) \sin(\theta)\, d\theta \end{aligned} \tag{15}$$

$$\begin{aligned} v_C(\theta) &= \left[\frac{2}{\pi} V_i \cos(\delta) + \frac{I_i}{2\pi\omega_s C_c}(1 + \cos(\delta)(\cos(\delta) - 2))\right] \\ &\quad \times \sin(\theta) + \left[-\frac{2}{\pi} V_i \sin(\delta) - \frac{I_i}{2\pi\omega_s C_c}\Big(\delta + \sin(\delta) \right. \\ &\quad \left. \times (\cos(\delta) - 2)\Big)\right] \cos(\theta) \end{aligned} \tag{16}$$

$$\begin{aligned} Z_C &= \left[\frac{2V_i}{\pi I_i} \cos(\delta) + \frac{1}{2\pi\omega_s C_c}(1 + \cos(\delta)(\cos(\delta) - 2))\right] \\ &\quad + j\left[-\frac{2V_i}{\pi I_i} \sin(\delta) - \frac{1}{2\pi\omega_s C_c}(\delta + \sin(\delta)(\cos(\delta) \right. \\ &\quad \left. - 2))\right]. \end{aligned} \tag{17}$$

By substituting (12) into (15), the fundamental component of v_c is found in (16).

Step 3: An equivalent impedance for diode–capacitor combination is found by dividing the expression obtained in step 2 by the sinusoidal input current $i_i = I_i \sin(\theta)$.

The equivalent impedance of the diode–capacitor combination is obtained by applying the transform $\cos(\theta) = j\sin(\theta)$ and then dividing by resonant current as in (17).

By substituting the Z_c into the FHA model provides (18) where the effect of the diode clamp is now accounted for allowing the magnitude of the resonant tank current under clamping (i.e., overload) to be found. The output voltage can be found by

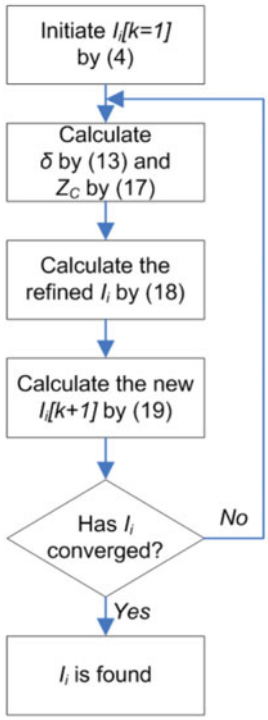

Fig. 4. Flowchart describing the interactive procedure for finding the load current during overloading conditions. Half-bridge *LLC* resonant converter with capacitor–diode clamp.

substituting (18) into (5)

$$I_i = \frac{2V_i}{\pi Z_2} \tag{18}$$

where $Z_2 = R_{\text{eq}} || sL_p + sL_s + 1/sC_s + Z_c$, where s and R_{eq} are as defined in previous section.

C. Diode–Clamp Conduction Point

Since (18) cannot be solved analytically owing to the dependence on I_i for determining both δ and Z_c, an iterative procedure similar to that employed in [26] is used: the value for the resonant tank current is first estimated using (4) by assuming the diode clamp is inactive. Once a value for I_i has been obtained, the nonconduction angle, δ, and capacitor–diode clamp equivalent impedance, Z_c, are found by (13) and (17), after which a refined value for I_i is found by (18). The refinement of δ, Z_c, and I_i are achieved through an iterative loop, flowchart shown in Fig. 4, until they converge. To ensure satisfactory convergence, a damping factor should be used to determine the new resonant tank current value, $I_i[k+1]$, in a similar manner to the technique commonly employed with Newton's method [31]

$$I_i[k+1] = I_i[k] + \alpha\left(I_{\text{DC}}[k+1] - I_i[k]\right) \tag{19}$$

where $I_i[k+1]$ and $I_i[k]$ is the new value and old value of resonant tank current, respectively, $I_{\text{DC}}[k+1]$ is the present refined resonant tank current predicted by (18) and α is the damping factor with a value between 0 and 1.

D. Nominalized Gain With Active Diode Clamp

Similar to the inactive diode–clamp case (i.e., normal noncurrent limited operation), the converter gain with an active diode clamp, $M_{g(\mathrm{clmp})}$, is obtained through substituting (18) into (5) and rearrange in terms of $(2nV_o)/V_i$ as in (20), after which substituting $s = j\omega$, $Z_c = R + jX$ (where R and X are the real and imaginary part of Z_c in (17), respectively), and introducing the $j\omega C_r$ term into both the numerator and denominator as in (21)

$$M_{g(\mathrm{clmp})} = \frac{2nV_o}{V_i} = \frac{R_{\mathrm{eq}} || sL_p}{R_{\mathrm{eq}} || sL_p + sL_s + \frac{1}{sC_s} + Z_c} \tag{20}$$

The final step involves substituting the following normalizing factors $L_p = AL_s, L_sC_r = 1/\omega_0^2, f_n = \omega/\omega_0, L_s/R_{\mathrm{eq}} = Q/\omega_0$, and $B = C_r/C_s$, to obtain:

$$M_{g(\mathrm{clmp})} = \frac{f_n^2 A}{f_n^2 A + f_n^2 - B + k_r + j\left(f_n^3 AQ - f_n AQB + k_i\right)} \tag{22}$$

where $k_r = \omega C_r\left(f_n AQR + X\right)$ and $k_i = \omega C_r\left(-R + f_n AQX\right)$, are terms accounting for the change in the effective impedance of the C_c caused by the diode clamp when it is active and it is assumed that the values for R and X have converged.

Without the diode clamp (i.e., normal operation), $R = 0$, and B can either be one or zero: when $B = 0, X = -1/\left(2\omega C_c\right), k_r = -1$, and $k_i = -f_n AQ$, and when $B = 1, X = 0, k_r = 0$, and $k_i = 0$. In both cases, (22) can be simplified to (6).

IV. Analysis of Converter Operating Characteristic

Before giving detailed discussion on the characteristic of the capacitor–diode clamp, the converter normal loading operation is briefly described.

Assuming the capacitor–diode clamp has been designed such that it only becomes active when the load current exceeds the maximum rated load current, the converter can be treated as standard *LLC* resonant converter up to the maximum load condition. When the standard *LLC* converter is operated at the series resonant frequency, f_0, its voltage gain, M_g, is fixed and is unaffected by changes in the load (i.e., operation at the LIP). Thus, one popular method for designing *LLC* converters [27], [32] is to select the transformer turn ratio, n, such that the voltage gain at the series resonant frequency under the nominal operating condition is unity, $M_g\left(f_0\right) = 1$. The resonant tank components are then selected through the normalized variables A and Q using (6) to accommodate the M_g requirement for changes the in input voltage over a given frequency range. In practice small changes in frequency are also required to compensate for inevitable voltage drops caused by changes in the load.

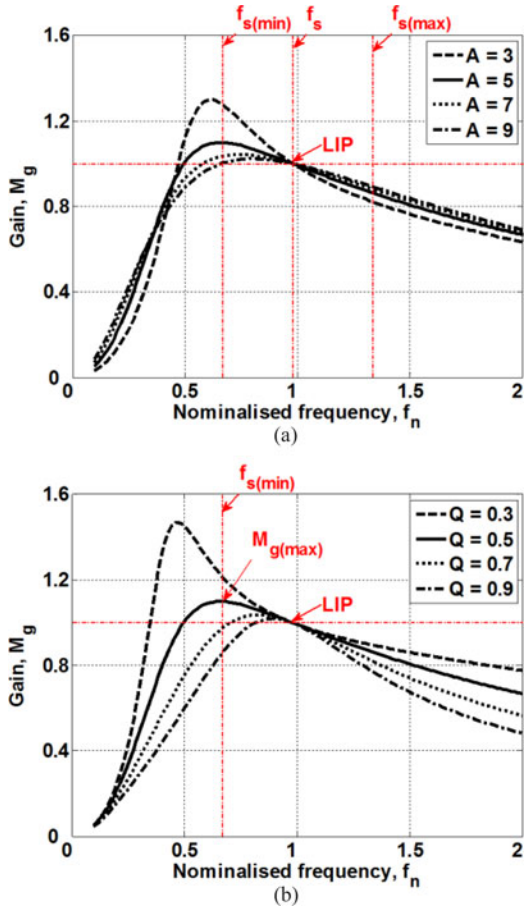

Fig. 5. Converter gain characteristics. (a) $Q = 0.5, 3 \leq \mathrm{A} \leq 9$, and (b) $0.3 \leq \mathrm{Q} \leq 0.9, \mathrm{A} = 5$.

With the nominal input voltage, $V_{i(\mathrm{nom})}$, at the LIP, the converter gain from (6) with $3 \leq A \leq 9$ and $0.3 \leq Q \leq 0.9$ are plotted in Figs. 5(a) and (b), respectively. Fig. 5(a) shows that a smaller A leads to higher gain while Fig. 5(b) shows that smaller Q leads to higher gain as well the increasing the frequency range. If A is selected to be 5, the maximum Q that satisfies the gain requirement, $M_{g(\max)}$, can be identified with Fig. 5(b).

Since $Q(= \sqrt{L_s/C_r}/R_{\mathrm{eq}})$, and L_s and C_r are fixed at the design stage, the change in gain characteristic due to the change in Q is equivalent to the change in load condition, R_{eq}. If the converter gain curve under full rated load condition (with $Q = 0.3$) is the horizontal dashed line in Fig. 5(b), then, the gain curve with three times overloading is identical to that in the dash-dotted line (i.e., $Q = 0.9$). With the focus of this particular analysis on the converter's overloading characteristic, the Q is normalized against Q_{rate} which is the Q-factor at the rated load

$$M_{g(\mathrm{clmp})} = \frac{j^2\omega^2 L_pC_r}{j^2\omega^2 L_pC_r + \frac{j^3\omega^3 L_sL_pC_r}{R_{\mathrm{eq}}} + j^2\omega^2 L_sC_r + \frac{j\omega L_pC_r}{C_sR_{\mathrm{eq}}} + \frac{C_r}{C_s} + \frac{j^2\omega^2 RL_pC_r}{R_{\mathrm{eq}}} + Rj\omega C_r + \frac{j^3\omega^2 C_rXL_p}{R_{\mathrm{eq}}} + j^2X\omega C_r} \tag{21}$$

(i.e., $Q = 0.3$ becomes $Q_n = 1$) as in

$$Q_n = \frac{Q}{Q_{\rm rate}}. \tag{23}$$

A. Capacitor Diode–Clamp Characteristics

This section compares voltage gain under normal and overload conditions when operating in the vicinity of LIP.

In the case where the diode clamp is inactive, with $A = 5$ and $Q_{\rm rate} = 0.5$, the converter voltage gain characteristic for $1 \le Q_n \le 10$ and $0.5 \le f_n \le 1.5$ is calculated using (6) and is plotted in Fig. 6(a). As expected there is little change in the gain around the LIP $(f_n = 1)$ for increasing Q_n.

Assuming the resonant capacitor (calculated for the above A and $Q_{\rm rate}$) is now split into the two clamping capacitors $C_c\,(=1/\,(2C_r))$ and is clamped by $D_{\rm c1}$ and $D_{\rm c2}$ to the input voltage under overload. The voltage gain $M_{g(\rm clmp)}$ under the same ranges of f_n and Q_n is calculated by (22) (with the k_r and k_i for each operating point calculated by the procedure highlighted in Fig. 4) and is plotted in Fig. 6(b). The results show that in the diode–clamp inactive region (to the right of the diode–clamp active–inactive boundary solid black line), the gain is unaffected, whereas in the diode–clamp active region the gain around the LIP $(f_n = 1)$ is dramatically reduced for increasing Q_n and thereby reducing the current under overloading conditions. Fig. 6(b) also shows the peak gain with $f_n = 0.6$ is reduced below the required $M_{g(\rm max)}$, and so load regulation at the rated load $(Q_n = 1)$ may no longer be achievable with low input voltages.

Therefore, to retain regulation (that is to achieve the required $M_{g(\rm max)}$) for the rated load condition, the diode–clamp active region must be reduced. This can be achieved by increasing C_c, by choosing a larger value for B, which reduces the voltage V_c for the same load current and, thus, a larger current is required to activate the diode clamp.

Using (22), the voltage gain characteristic with B of 0.25, 0.5, and 0.75 are plotted in Figs. 7(a), (b), and (c), respectively. The figures show that as B increases, the diode–clamp active region reduces. With $B \ge 0.5$, the $M_{g(\rm max)}$ is retained for this particular example, allowing normal regulation at the full rated load condition. The penalty with the higher B is the diode clamp becomes less effective in reducing the voltage gain, hence overload current.

The design task involves the selection of the lowest B that retains the $M_{g(\rm max)}$ operating point while providing the maximum gain reduction when operating with overload conditions $(Q_n > 1)$.

To validate the accuracy of the proposed model, the gain characteristics of the resonant converter under different operating conditions are simulated in SPICE and are compared against Figs. 6 and 7. The converter gain characteristics from Figs. 6(a) and (b) with $Q_n = 1, Q_n = 5$, and $Q_n = 10$ are plotted in Figs. 8(a) and (b), respectively, alongside results obtained from SPICE (indicated by the markers) which show a good level of correlation.

For completeness, the converter gain characteristics from Fig. 7(a), (b), and (c) with $Q_n = 1, Q_n = 5$, and $Q_n = 10$ are also compared to SPICE, Fig. 9. The results depicted in Figs. 8 and 9 validate the proposed model over a wide range of operating conditions.

B. Converter Voltage–Current (V-I) characteristics

To illustrate how the reduction in voltage gain by the action of diode clamp leads to the reduction in overload current, the converter voltage gain M_g under different Q_n and f_n, for the different B, are first normalized against the unclamped rated full load gain (i.e., $B = 1, Q_n = 1$) at the corresponding f_n, after which the converter normalized voltage V_n and normalized current I_n for $1 \le Q_n \le 10$ are calculated by Ohm's law and plotted in Figs. 10(a)–(e).

Fig. 10(a) shows operation with no clamping action $(B = 1)$, the voltage V_n at the LIP for different values of Q_n is unaffected and is equal to unity as expected. Thus, 10 times overloading $(Q_n = 10)$ leads to 10 times increase in the current I_n when operating at $f_n = 1$. Fig. 10(b) shows that with the resonant capacitance fully clamped $(B = 0)$, the reduction in $M_{g(\rm clmp)}$ by the diode clamp in Fig. 6(b) leads to the reduction of V_n to 0.29, and I_n to 2.9 (at the LIP with $Q_n = 10$). The figure also shows there is a range of f_n where the $V_n < 1$. This means regulation is not achievable for low input voltages as discussed in Section IV-A. The $V_n I_n$ characteristic for $B = 0.25$, 0.5, and 0.75 are also plotted in Figs. 10(c), (d), and (e), respectively. Fig. 10(d) and (e) shows that for $B \ge 0.5$, regulation is achieved at all f_n. Comparing Figs. 10(c)–(e), I_n at the LIP with $Q_n = 10$ is increased from 3.1 to 6.9. Thus, the attenuation of overload current is inversely proportional to the capacitor ratio, B. Fig. 10 shows that with a suitably chosen value for B the overload current can be limited without the need for any external control action.

V. Design Example

To validate the accuracy of the equivalent circuit model and analysis in the previous sections, an *LLC* resonant converter with power rating of 90 W (36 V, 2.5 A), $V_i = 390$ V $\pm 4\%$ and $f_{\rm o} = 147$ kHz is selected.

Following the design procedure in [27] and with the converter operating at the LIP under the nominal input voltage of 390 V, the transformer turn ratio n is selected to be 5.5, the minimum gain for the minimum input voltage is calculated to be 1.09. With the inductor ratio, A, selected to be 5 (for narrow range of operating frequency), the maximum quality factor that satisfies the required gain is $Q = 0.52$. This leads to the selection of the following resonant tank components: $L_s = 236\ \mu$H, $L_p = 1.2$ mH, and $C_r = 5$ nF with the minimum and maximum operating frequencies are 100 and 152 kHz, respectively. The value for C_c that provides the optimum current limiting performance is found by the model to be 3.6 nF. The C_s is calculated to be 17 nF and the B is 0.3 from (2).

With the resonant tank components above, the capacitor branch voltage v_c under full load and 10 times overloading at the nominal input voltage of 390 V are plotted in Figs. 11(a) and

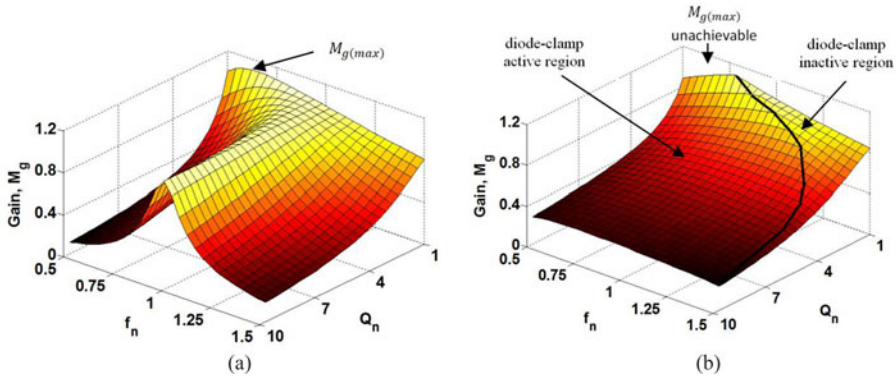

Fig. 6. Converter gain characteristics with A $= 5$ and $Q_{\rm rate} = 0.5$. (a) B $= 1$ and (b) B $= 0$.

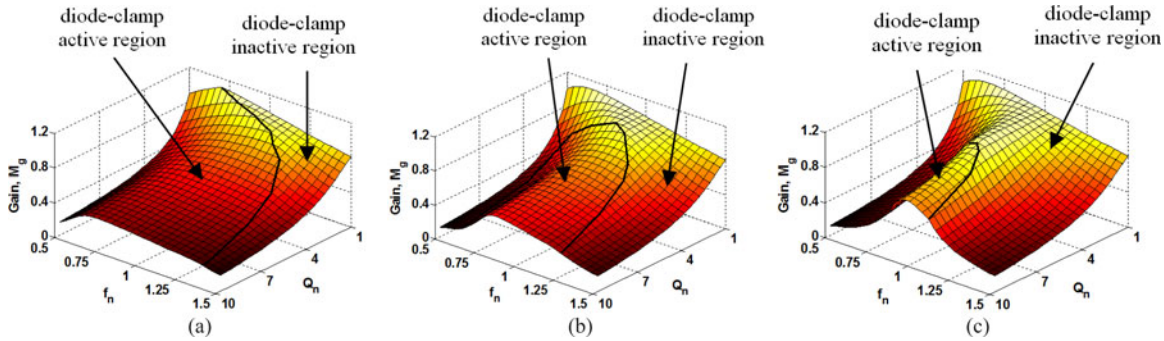

Fig. 7. Converter gain characteristics with $A = 5$ and $Q_{\rm rate} = 0.5$. (a) $B = 0.25$, (b) $B = 0.5$, and (c) $B = 0.75$.

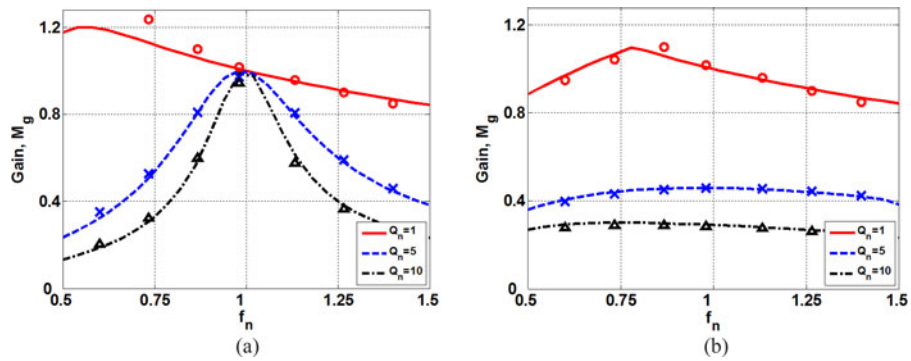

Fig. 8. Converter gain characteristics with $A = 5$ and $Q_{\rm rate} = 0.5$. (a) $B = 1$ and (b) $B = 0$.

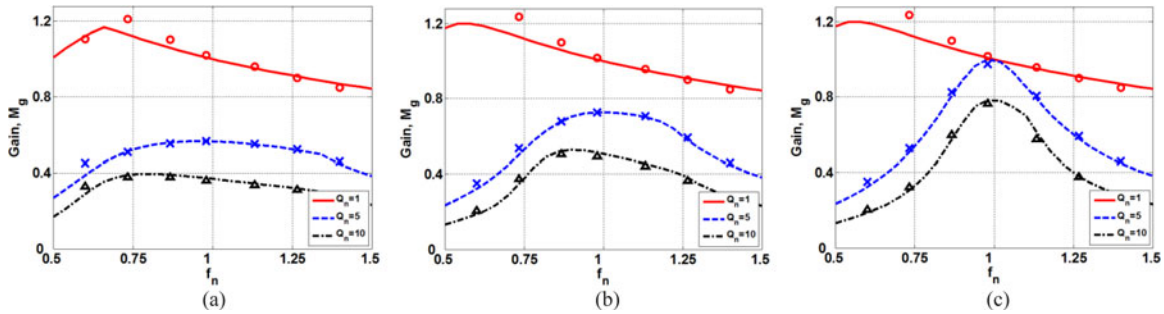

Fig. 9. Converter gain characteristics with $A = 5$ and $Q_{\rm rate} = 0.5$. (a) $B = 0.25$ and (b) $B = 0.5$ (c) $B = 0.75$.

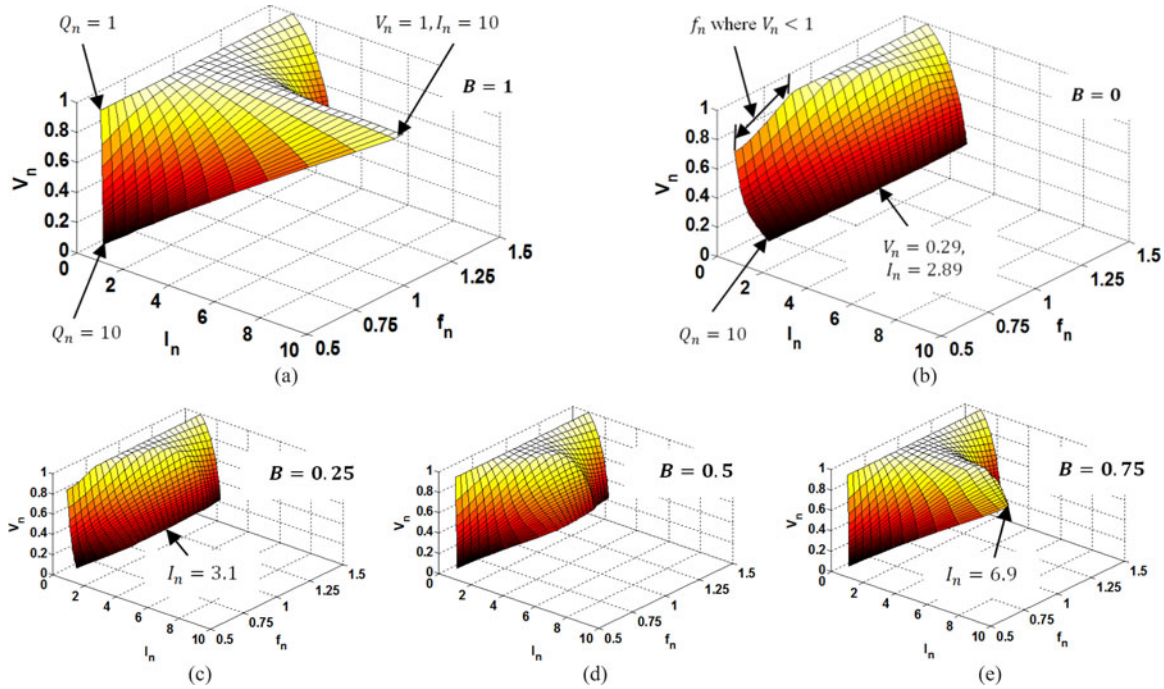

Fig. 10. Converter *V–I* characteristics. (a) $B = 1$, (b) $B = 0$, (c) $B = 0.25$, (d) $B = 0.5$, and (e) $B = 0.75$.

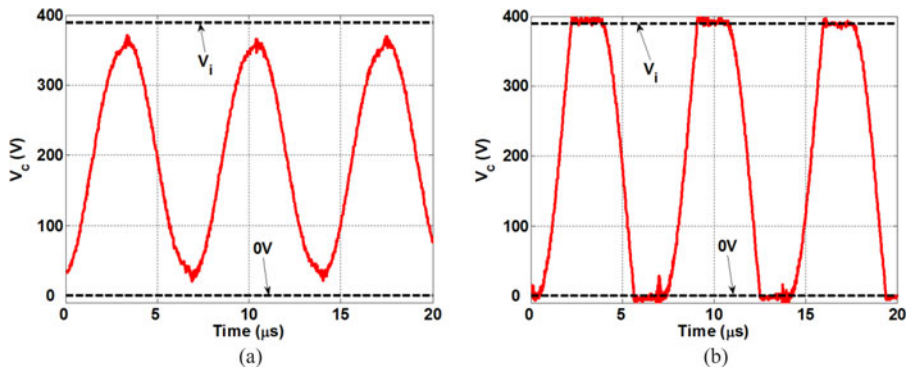

Fig. 11. Measured resonant capacitor voltage waveform v_c. (a) Normal operation and (b) overloading operation.

(b), respectively. Fig. 11(a) shows that under the full load condition, the peak-to-peak value of v_c is below the input voltage and therefore the diode clamp is inactive. The voltage waveform across capacitor C_c at 10 times overloading is clamped between the 0 and V_i as shown in Fig. 11(b). From Fig. 11(b), the conduction angle (n.b. $\delta = 2\pi f_s t$) is found to be 91°, in comparison to the value of $\delta = 95°$ found by the procedure in Section III-C, showing an error of 4%.

The voltage gains of the prototype converter under the full rated load and five and 10 times overload conditions are calculated from (22) and shown in dash-line, dot-line, and dash-dot-line, respectively, in Fig. 12(a). When $B = 0.3$, the gain under full load condition is unaffected. The practical gains under the same load conditions are plotted in circle, square, and triangle in Fig 12(a), respectively, showing a good match to the theoretical result.

The converter's *V-I* characteristic, from full rated load to 10 times overload conditions, under the $f_{s(\min)}, f_s$, and $f_{s(\max)}$ are plotted in dash-line, dot-line, and dash-dot-line, respectively, in Fig. 12(b) (n.b. V_i is select according to $f_s \left(V_{i(\max)} \geq V_i \geq V_{i(\min)} \mapsto f_{s(\min)} \leq f_n \leq f_{s(\max)}\right)$ to maintain the desired output voltage at the maximum rated load under different f_s). At 10 times overload, the current is limited by the diode clamp to 8 A for the three input voltages. The measured practical *V–I* characteristics under the three input voltages from the prototype converter are plotted in circle, square, and triangle, respectively, in Fig. 12(b). The trends agree well with the model predictions.

For completeness a comparison is made between current limiting provided by the diode–clamp protected converter operating at a fixed frequency and frequency controlled converter using SPICE simulations, see Fig. 13. The *V–I* characteristic of the converter without the diode clamp and operating at fixed frequency ($f_n = 147\,\text{kHz}$) at the nominal input voltage highlights the requirement for overload protection [W/O clamp (SPICE)]. In order for the converter without the diode clamp to provide

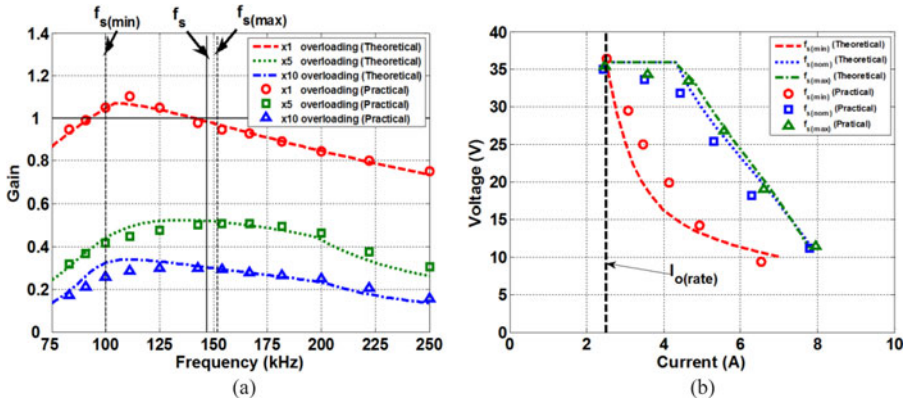

Fig. 12. Comparison of the theoretical and practical results. (a) Voltage gain characteristics. (b) *V–I* characteristics.

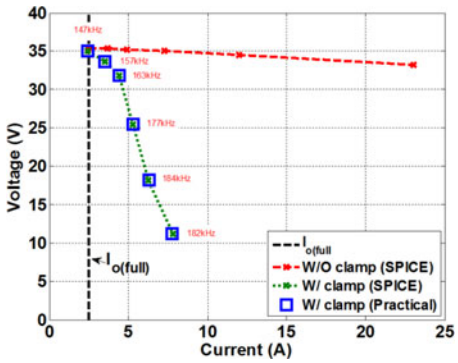

Fig. 13. Comparison between diode–clamp and frequency current limit protected converters.

the similar level of protection to a diode–clamp protected converter (W/ clamp) the switching frequency has to be somewhat increased [W/O clamp (SPICE)]. With 10 times overloading, the switching frequency has to be increased from 147 to 182 kHz. The practical results from Fig. 12(b) have been included for comparison and show excellent agreement with SPICE.

VI. Conclusion

An FHA equivalent circuit model describing the behavior of the *LLC* resonant converter with the capacitor–diode clamp has been derived using describing function techniques, where the equivalent impedance of the diode/capacitor, Z_c, are first obtained using a three step process, after which it is combined with the FHA to allow the resonant current to be found. An iterative procedure for determining the conduction point of the diode clamp has also been detailed. A resonant capacitance sharing ratio B has been introduced to allow the best current-limiting performance to be analyzed. The presented analysis has shown that in order to obtained the best current limiting characteristic in overload condition, the clamped portion of the resonant capacitors C_c must be selected such that the current clamp starts operating as soon as the maximum load current under the minimum input voltage, is exceeded. A 90 W converter and its diode clamp was designed with $A = 5, Q_{\rm rate} = 0.52$, and $B = 0.3$. Using the proposed equivalent circuit model, converter static gain characteristics and the VI characteristics between the rated load and 10 times overloading are predicted using the new nominalized gain equation $M_{g(\rm clmp)}$. When compared with the experimental measurements taken from the prototype, the overall trend of the practical results follow that of the prediction, at 10 times overloading, output current was successfully reduced from 25 to 8 A.

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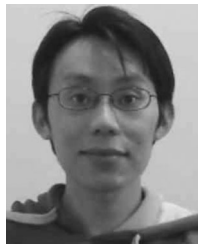

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