A Simple Average Current Control With On-Time Doubler for Multiphase CCM PFC Converter

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***Abstract*—This paper proposes a new modulated carrier control method for an interleaved continuous conduction mode (CCM) power factor correction (PFC) boost converter. The proposed method allows precise sinusoidal line current shaping for a PFC boost converter operating in CCM. This is accomplished by simply comparing modulated carrier signal with switch current, such that inner current loop compensation design and rectified line voltage sensing are not required. The proposed control method greatly simplifies current sensing and control circuitry of multiphase converters since average current control is available by just sensing the switch current for each module. This also enables simple current balancing between parallel converters by employing modulated carrier signals with same amplitude. The principle of the control method is presented. The performance of the proposed control method is experimentally verified on a 600-W PFC converter. The measured power factor remains above 94.9% down to 20% of a full load for 110-$V_{\rm rms}$ and 220-$V_{\rm rms}$ line voltages. The line current harmonics also meet the IEC61000-3-2 Class D standard.**

***Index Terms*—Boost converter, current balancing, interleaving, modulated carrier control, power factor correction (PFC).**

I. Introduction

As power grid harmonic pollution has attracted growing attention, standards regulating line current harmonic content and power factor have become more stringent causing power factor correction (PFC) to be indispensable for off-line power supplies. To achieve a high power factor in single-phase off-line switched power supplies for high-power applications above 300 W, a continuous conduction mode (CCM) boost converter has been the most preferable topology. However, the conventional single-phase CCM boost PFC encounters limitations on high efficiency and high power density attainment due to increased conduction loss and bulky passive components [1].

To overcome the limitations, an interleaving technique is very often employed [1]–[15]. The major advantage of interleaving is that it increases an effective current ripple frequency without sacrificing switching loss and also partially cancels input and output current ripples. Moreover, it can effectively reduce both common mode (CM) and differential mode (DM) noise by canceling noise harmonics [3]–[6]. As a result, the overall size of energy storage inductor and electromagnetic interference (EMI) filter can be drastically reduced.

However, current balancing between interleaved PFC modules operating in CCM has been a critical issue since current imbalance due to a discrepancy between device parameters and control parameter tolerance can result in more thermal stress on a particular phase so that it may mistrigger overcurrent protection. For single-phase PFC control, a current sensing resistor can be placed on the return path. Multiphase interleaved PFC control, however, does not allow for such simple resistive current sensing because the return path is common for all modules. As a result, sensing the individual inductor currents is challenging to balance average current between modules. To address this issue, various implementations of interleaved PFC control have been proposed [9]–[12]. The method proposed in [9] senses three currents: total input current for line current shaping and two individual switch currents for current balancing. It has a relatively complex implementation which requires a line voltage sensing and a multiplier. The method proposed in [10] senses only two switch currents when a power MOSFET is on. Inductor currents during remaining switching cycle are synthesized based on input and output voltage and are regulated with average current feedback loop. However, this sophisticated method employs an analog multiplier which complicates the control integrated circuit (IC). The technique presented in [11] proposed a digital signal processor (DSP) based control for current sharing of multiple PFC modules. The controller senses individual inductor currents and implements duty ratio for each module for proper current sharing. A disadvantage of this technique is that a DSP is inevitably needed to determine the duty cycles of the switches. The current balancing method proposed in [12] only needs the sum of two switch currents, but it requires a complicated control circuitry that contains high speed analog-to-digital converters and a DSP.

To simplify the existing PFC control circuitry based on the analog multiplier or DSP, low-cost control strategies for PFCs operating in CCM were proposed in [17] and [18], and several variations have been proposed in [19]–[43]. Since these methods do not require line voltage sensing, multiplier in average current control (ACC), and current loop compensation design consideration, some of them have been successfully commercialized as ICs [36]–[39]. However, most of these methods necessarily

Manuscript received November 21, 2013; revised February 4, 2014 and March 31, 2014; accepted April 2, 2014. Date of publication April 17, 2014; date of current version October 15, 2014. This work was supported by the Industrial Infrastructure Program for Fundamental Technologies, funded by the Ministry of Knowledge Economy (MKE), Korea. Recommended for publication by Associate Editor C. N. M. Ho.

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Digital Object Identifier 10.1109/TPEL.2014.2318033

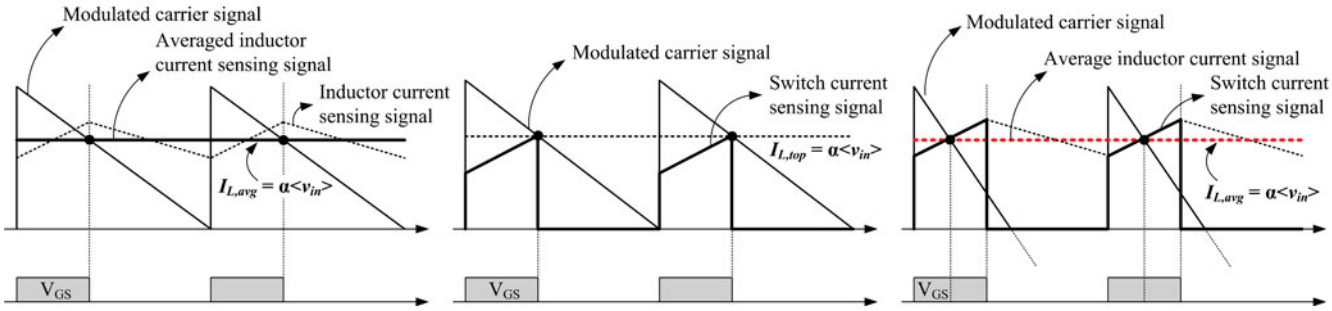

Fig. 1. Control method comparison: (a) modulated carrier control with averaged inductor current, (b) modulated carrier control with peak detector, and (c) proposed modulated carrier control.

require entire inductor current or averaged inductor current information rather than switch current to obtain unity power factor as shown in Fig. 1(a), which is not preferable for interleaved PFC. Furthermore, as [39]–[41] utilize the peak value of inductor or switch current under a small current ripple assumption to determine duty ratio, the envelop of the inductor current is controlled to follow line voltage shape so that they experience a line current distortion due to current error as illustrated in Fig. 1(b). Although Maksimovic *et al*. [18] can realize ACC only with switch current information, it complicates the analog control circuit implementation due to its nonlinear carrier signal. In addition, since line voltage feed-forward, which eliminates dependency of the voltage loop gain on the line root-mean-square (rms) voltage, becomes unavailable, the work in [19], [23], and [26] suffer from output voltage regulation issue.

In this paper, a new modulated carrier control method [16], [43] for an interleaved boost PFC converter is proposed. The proposed method is accomplished by simply comparing switch current sensing signals with linear carrier signals which is comparable to one-cycle-based control method [23]. This allows precise sinusoidal line current shaping for a CCM boost PFC converter so that it eliminates the line voltage sensing, the analog multiplier, and the current loop compensation design. In addition, the proposed method adopts a modified carrier signal and an on-time doubler to realize an ACC. Since the on-time doubler enables the average inductor current to follow sinusoidal line voltage by extracting the average current information from the sensed switch current as described in Fig. 1(c), it is advantageous to multiphase interleaved PFC converters. While conventional control needs the entire inductor current information for ACC or complex control algorithm, the proposed method realizes an effective ACC only with switch current waveforms. Thus, it greatly simplifies the current sensing and control circuitry for multiphase CCM PFC converters by reducing the amount of components needed for current transformer current sensing. It also enables simple current balancing between multiphase converters by employing carrier signals with the same amplitude, which is proportional to the output of the voltage controller.

This paper is organized as follows. The next section presents basic principle of the proposed modulated carrier control scheme for the interleaved CCM boost PFC converter. Section III defines condition for CCM operation and examines current distortion in discontinuous conduction mode (DCM) operation. Section IV gives small-signal analysis for output voltage compensation design. Section V discusses implementation of the proposed method and presents experimental results to validate the performance with 600-W laboratory prototype.

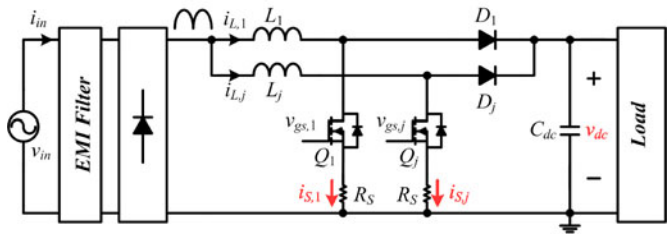

Fig. 2. Power circuit of an interleaved boost PFC converter.

II. Description of the Proposed Method

Fig. 2 shows a power circuit of an interleaved boost PFC converter. L_1 and L_j are boost inductances. $v_{\rm in}, i_{\rm in}, i_{L,1}, i_{L,{\rm j}}, v_{gs,1}, v_{gs,j}$, and $v_{\rm dc}$ are line voltage, line current, first module inductor current, jth module inductor current, first module gate-source voltage, jth module gate-source voltage, and output voltage, respectively. Current sensing resistor R_S is placed in series with each MOSFET switch, Q_1 and Q_j, to obtain boost inductor current information. To understand an operation principle of the proposed method, the basic control law presented in [27] is explained. The unity power factor operation requires that average inductor current follows a current reference proportional to rectified line voltage as

$$i_{L,\rm avg} = i_{\rm ref} = \frac{|v_{\rm in}|}{R_e} \tag{1}$$

where $|v_{\rm in}|$ is the rectified line voltage and R_e is the emulated resistance determined by output voltage controller. For a boost converter operating in CCM, the input to output voltage gain incorporating duty ratio d is given by

$$\frac{v_{\rm dc}}{|v_{\rm in}|} = \frac{1}{1-d}. \tag{2}$$

Combining (1) and (2) with the current sensing resistor R_S yields

$$\frac{(1-d)v_{\rm dc}R_S}{R_e} = i_{L,\rm avg}R_S \tag{3}$$

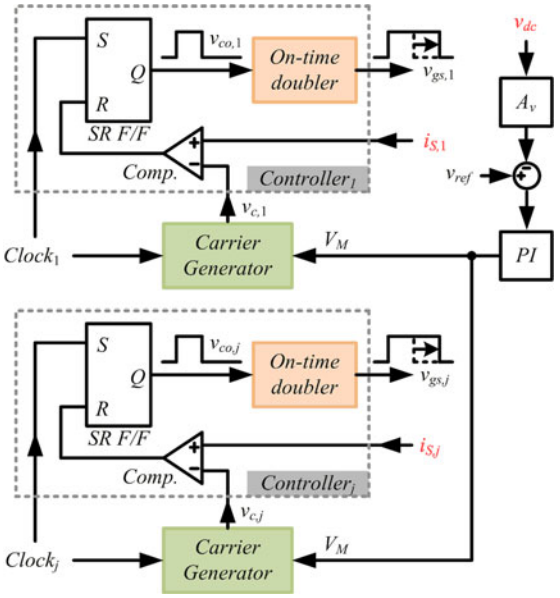

Fig. 3. Control block diagram of the proposed control.

and let

$$V_M = \frac{v_{\rm dc} R_S}{R_e}. \tag{4}$$

Then, the control law for the boost PFC converter is presented as follows:

$$V_M(1-d) = R_S i_{L,\rm avg}. \tag{5}$$

The control equation shows that average inductor current can be controlled to follow the sinusoidal line voltage by controlling d to satisfy (5) in each switching cycle. This equation can be implemented with the modified modulated carrier and on-time doubler.

A. Operation Principle

Figs. 3 and 4 depict the control block diagram and timing diagram of the proposed modulation method to realize (5). The control circuit contains a proportional–integral (PI) controller, clocks, sawtooth carrier signal generators, comparators, set–reset flip-flops (SR F/Fs), and on-time doublers. First, $v_{\rm dc}$ is sensed and compared with reference voltage $v_{\rm ref}$. This error is processed by the PI controller to generate a signal V_M, which varies with load condition. A sawtooth carrier signal whose peak-to-peak value is $2V_M$ is generated. As shown in Fig. 4, the carrier signal, $v_{c,j}$, decreases linearly from the maximum voltage V_M to the minimum voltage $-V_M$ during one switching period as expressed in the following:

$$v_{c,j}(t) = V_M\left(1 - \frac{2t}{T_S}\right) \quad \text{for} \quad \frac{T_s}{j} \le t < \left(1+\frac{1}{j}\right)T_s \tag{6}$$

where j, N, and T_S are the module number, number of modules, and time period of one switching cycle, respectively. The carrier signal $v_{c,j}$ of the jth module is obtained by shifting the carrier signal $v_{c,1}$ by T_S/j.

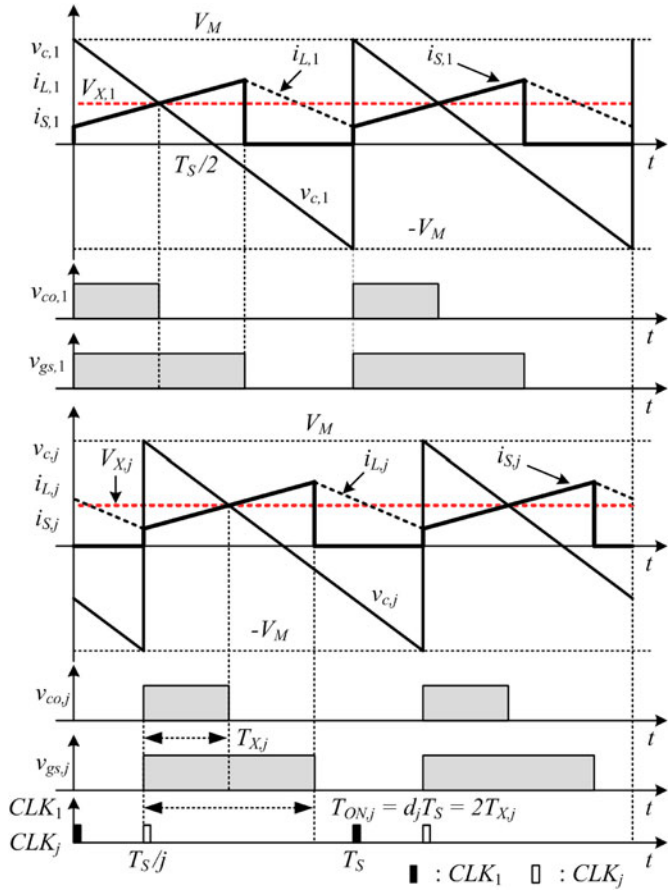

Fig. 4. Timing diagram of the proposed interleaved boost PFC control.

The rising edge of the clock signal (CLK_j) sets the SR F/F, which initiates corresponding switching cycle. Once the switch is turned on, the switch current increases. When the measured switch current intersects the carrier signal, the comparator resets the SR F/F. An on-time doubler measures time duration from the rising edge to the falling edge of the SR F/F output $v_{co,j}$ and then outputs a gate drive signal $v_{gs,j}$ that has twice conduction time of $v_{co,j}$. Thus, the on-time of switch Q_j can be expressed as

$$T_{{\rm ON},j} = d_j T_S = 2T_{X,j} \tag{7}$$

where d_j is the duty cycle of the jth module. In the CCM boost PFC converter, the current of Q_j in the middle of its conduction time is the same as average inductor current as

$$V_{X,j} = i_{L,{\rm avg},j} R_S \tag{8}$$

where $i_{L,{\rm avg},j}$ is the average inductor current within one switching cycle, and $V_{X,j}$ is the voltage across R_S at the intersecting instant.

The duty cycle d_j of a CCM boost PFC converter is

$$d_j = 1 - \frac{|v_{\rm in}|}{v_{\rm dc}}. \tag{9}$$

Therefore, combining (6)–(9) yields

$$i_{L,{\rm avg},j} R_S = V_{X,j} = V_M \frac{|v_{\rm in}|}{v_{\rm dc}}. \tag{10}$$

From (10), it can be inferred that $i_{L,\mathrm{avg},j}$ is proportional to $|v_{in}|$ as long as the boost converter operates in CCM. In conclusion, this allows for a unity power factor with sinusoidal line voltage.

As a result, the proposed modulation technique is able to perform a CCM PFC operation by using only switch current sensing, linear carrier signal, and on-time doubler so that it eliminates the line voltage sensing circuitry, the current loop compensation design, and the precision analog multiplier. It also realizes the interleaving operation with only switch current sensing of each module and output voltage sensing. Moreover, it achieves the current balancing without additional current sensing circuitry on the common path or complicated current balancing algorithm since the ACC is available for each module, as shown in (10).

B. Effect of Parameter Mismatches on Current Sharing

As discussed in Section I, the current imbalance due to the mismatches between components such as boost inductor or current sensing resistor is a primary concern for the multiphase converters [12], [44]. As the proposed method realizes the ACC, it would achieve the current balancing among parallel converters with mismatched boost inductances. However, if the multiphase converters have matched inductances but mismatched sensing resistances among the phases, the inductor currents would be unevenly distributed. To clarify the claim, a detailed analysis considering the mismatched current sensing resistance is conducted.

This analysis assumes that all components among the multiphase converters are matched except switch current sensing resistances. Then, the current sensing resistance mismatch ΔR leads to the worst-case current imbalance through a particular phase; all other phases have the same nominal sensing resistance equal to R, while ith phase has mismatched resistance $R_i = R + \Delta R$. If output power is constant and output voltage is well regulated, total average inductor current during one switching cycle is invariable regardless of the mismatch as follows:

$$\frac{(N-1)V_M'}{R}\frac{|v_{\mathrm{in}}|}{v_{\mathrm{dc}}} + \frac{V_M'}{R_i}\frac{|v_{\mathrm{in}}|}{v_{\mathrm{dc}}} = \frac{NV_M}{R}\frac{|v_{\mathrm{in}}|}{v_{\mathrm{dc}}} \tag{11}$$

where V_M' is the control signal in case of mismatched sensing resistance, and the second term on the left-hand side is the current I_i conducting ith phase while the right-hand side represents the sum of the nominal inductor current I_n of each phase in case of matched sensing resistance.

From (11), when ith switch current sensing resistance is mismatched, the control signal is

$$V_M' = \frac{NR_i}{R + (N-1)R_i}V_M. \tag{12}$$

Then, the relative current mismatch resulting from ith phase can be derived as

$$\frac{\Delta I_i}{I_n} = \frac{I_n - I_i}{I_n} = \frac{(N-1)\Delta R}{NR + (N-1)\Delta R} \tag{13}$$

which can be used to estimate total current mismatch due to the switch current sensing resistance mismatch. Since this sensing resistance mismatch issue prevails in most of the multiphase converters, it would require an additional correction technique such as minimum ripple voltage difference tracking algorithm [48]. However, high-precision sensing resistors, which will minimize the current mismatch, are widely used in practical applications and their tolerance is considered in the converter design process with proper margin. For example, assume that two boost PFC modules have 0.1 Ω sensing resistors with a tolerance of 0.1% ($N = 2$, $\Delta R/R = 0.1\%$). Then, the relative current mismatching is obtained as 0.05% as clarified in (13).

III. Current Distortion Analysis in DCM

The proposed modulation method is derived on the assumption that the boost PFC converter operates in CCM. However, the converter inevitably operates in DCM within a certain region where line voltage is near zero, and the region widens as load decreases. In DCM operation, (9) is no longer valid and the resulting line current would not exactly follow the line voltage. Therefore, following analysis derives CCM operating condition and examines current distortion in DCM to clarify the effect of mode change. In addition, the analysis confirms that the proposed modulation method extends the CCM operating region, which is advantageous to line current shaping with less distortion.

Fig. 5(a) shows main waveforms when the converter operates at the boundary of CCM and DCM. From the geometry of these waveforms, peak inductor current, i_{sp}, in each switching cycle is given by

$$i_{sp} = \frac{v_{\mathrm{dc}} - |v_{\mathrm{in}}|}{L}(1-d)T_S R_S \tag{14}$$

or

$$i_{sp} = \frac{|v_{\mathrm{in}}|}{L}dT_S R_S. \tag{15}$$

From (10), the relationship between d and i_{sp} is

$$V_M(1-d) = \frac{i_{sp}}{2}. \tag{16}$$

Replacing i_{sp} in (14) using (16) yields the following condition for this boundary operation:

$$V_{M,\mathrm{critical}} = \frac{(v_{\mathrm{dc}} - |v_{\mathrm{in}}|)R_S}{2Lf_s} \tag{17}$$

or

$$K_{\mathrm{critical}} = M_g - |\sin\omega t| \tag{18}$$

where

$$K_{\mathrm{critical}} = \frac{2Lf_s V_{M,\mathrm{critical}}}{R_s v_{\mathrm{in,peak}}} \tag{19}$$

is the critical load parameter commonly used in CCM/DCM boundary analysis, and M_g is voltage conversion ratio defined as

$$M_g = \frac{v_{\mathrm{dc}}}{v_{\mathrm{in,peak}}} \tag{20}$$

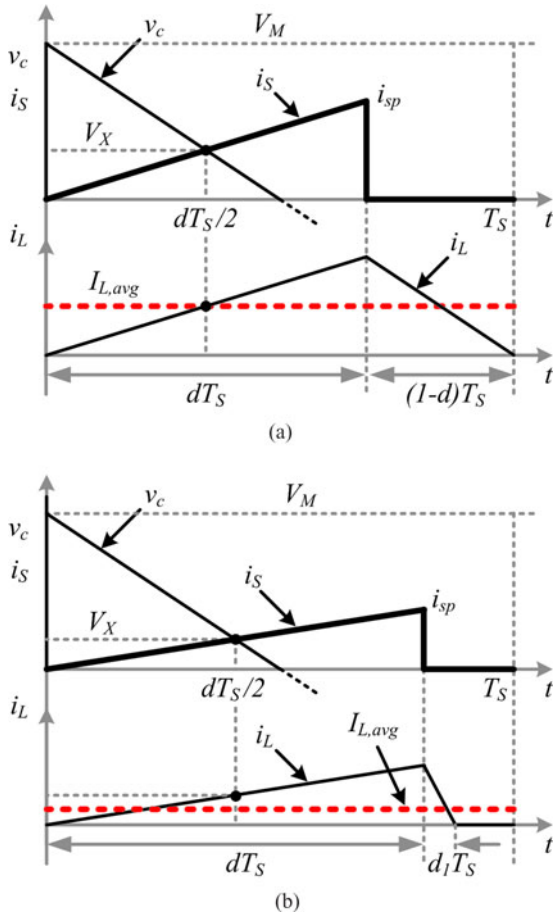

Fig. 5. Control waveforms: (a) at the boundary between CCM and DCM and (b) in DCM.

where $v_{\text{in,peak}}$ is peak value of the line voltage. Therefore, the converter always operates in CCM if

$$K > \max(K_{\text{critical}}) = M_g \tag{21}$$

and always in DCM if

$$K < \min(K_{\text{critical}}) = M_g - 1. \tag{22}$$

For any load between these boundary values, the converter will operate in DCM when v_{in} is near zero, and in CCM when v_{in} approaches $v_{\text{in,peak}}$. From (21) and (22), it can be noted that the proposed method is able to extend the CCM region compared to [40] and [42] without line voltage sensing because the on-time doubler effectively realizes ACC and maximizes the duty ratio around the zero crossings of the line voltage. As a result, the dead angle, which is encountered in the peak current control, is greatly reduced.

To derive an average inductor current in DCM and analyze a current distortion, DCM control waveforms shown in Fig. 5(b) are thoroughly examined. The peak current i_{sp}, as shown in Fig. 5(b), is given by

$$i_{sp} = \frac{v_{\text{dc}} - |v_{\text{in}}|}{L} d_1 T_S R_S. \tag{23}$$

Combining (15) and (16) derives

$$i_{sp} = \frac{2V_M}{1 + (2V_M L f_s / |v_{\text{in}}| R_s)}. \tag{24}$$

Meanwhile, the average inductor current in DCM can be found as a function of the duty ratios in Fig. 5(b) expressed as

$$i_{\text{avg,DCM}} = \frac{i_{sp}}{2R_s}(d + d_1). \tag{25}$$

By inserting (15), (23), and (24) into (25), we can obtain an expression for the average inductor current in DCM as follows:

$$i_{\text{avg,DCM}} = \frac{2v_{\text{dc}}V_M^2}{v_{\text{dc}} - |v_{\text{in}}|} \frac{|v_{\text{in}}|}{Lf_s} \frac{1}{((|v_{\text{in}}|R_s/Lf_s) + 2V_M)^2}. \tag{26}$$

Therefore, the difference between the average inductor currents in (1) and (26) describes the presence of harmonics in the line current. Using (19) and (26), distorted line current waveforms can be obtained for any parameters K and M_g, and also the harmonic contents of the line current due to DCM operation can be analyzed.

Fig. 6(a) and (b) shows normalized line current waveforms during one half of ac-line cycle for various load conditions with K as a running parameter based on (10) and (26) at 110-V_{rms} and 220-V_{rms}, respectively. The line current waveforms depend on the value of K and M_g, as shown in Fig. 6. When the line voltage is relatively low ($M_g = 2.5$), the line current is highly sinusoidal regardless of the load conditions. However, when the line voltage is relatively high ($M_g = 1.25$), the line current is highly sinusoidal only if $K > \max(K_{\text{critical}})$, which, in other words, means the CCM operation. If the load is reduced much below the minimum critical load parameter, significant distortion of the line current is obtained.

Fig. 7 shows estimated third, fifth, seventh, and eleventh harmonics of the line current when the considered load parameters are $K = 0.5\max(K_{\text{critical}})$ and $K = \min(K_{\text{critical}})$. The IEC61000-3-2 limits for each of the harmonics are also shown in Fig. 7. It can be noted that the magnitude of the estimated harmonics are well below the IEC61000-3-2 limits even in the DCM operation. Therefore, although the operation in DCM generates some current harmonics, it is possible to construct a low harmonic rectifier that meets harmonic limits and does not present a problem in practice.

IV. Small-Signal Modeling for Output Voltage Control

A small-signal model of the converter based on the proposed modulation technique is derived to determine the transfer function $\hat{v}_{\text{dc}}/\hat{v}_M$ of the system for output voltage control and also to examine the effect on line regulation for the output voltage. The following modeling and design approach is customized from [45]. A large-signal low-frequency model of the converter is shown in Fig. 8(a). The power consumed by the emulated resistance R_e is transferred to the output through the time-varying power source. For the voltage feedback loop design, the small-signal ac model is derived by averaging an output

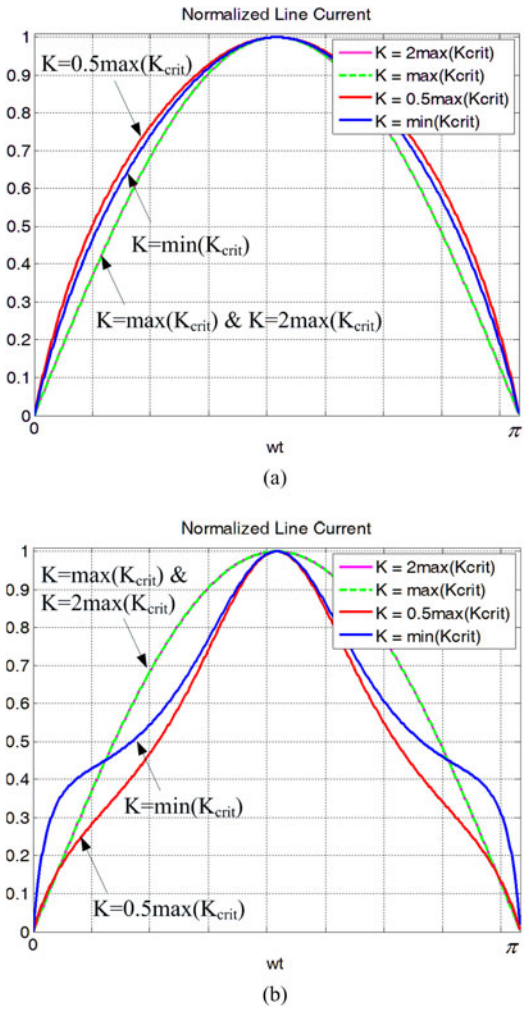

Fig. 6. Normalized line current waveforms with different K with proposed control method: when (a) M_g is 2.5 and (b) M_g is 1.25.

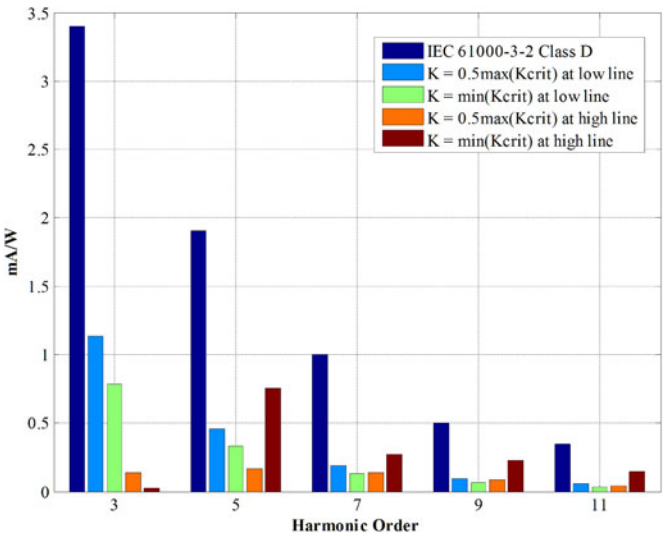

Fig. 7. Compliance to IEC61000-3-2 Class D according to K.

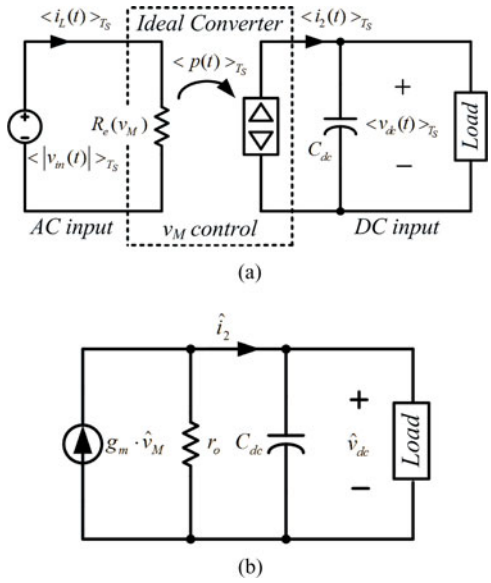

Fig. 8. Large- and small-signal model for output voltage control: (a) large-signal model, averaged over one switching cycle and (b) small-signal model of the proposed modulated carrier control.

current $i_2 = v_{\rm in} i_L / v_{\rm dc}$ over a half-line cycle as follows:

$$I_2 = \frac{V_{\rm in,rms}^2}{R_e(v_M) \cdot v_{\rm dc}} \tag{27}$$

where I_2 is the dc component of the current i_2. By perturbing (27) and subsequently linearizing, the small-signal model can be expressed as

$$\hat{i}_2 = g_m \cdot \hat{v}_M - \frac{\hat{v}_{\rm dc}}{r_o} \tag{28}$$

where

$$g_m = \frac{P_{\rm load}}{V_M \cdot V_{\rm dc}} \tag{29}$$

$$r_o = \frac{V_{\rm dc}^2}{P_{\rm load}}. \tag{30}$$

Fig. 8(b) shows a resultant low-frequency small-signal model of the converter by averaging over a half line cycle [45]. If the boost PFC converter delivers a constant power $P_{\rm load}$ to the load, then the small-signal input impedance at low frequency is given by $-V_{\rm dc}^2/P_{\rm load}$. It should be noted that the small-signal resistance r_o is of opposite sign to the input resistance of the constant power load, and the parallel combination is an open circuit. Therefore, the control-to-output transfer function of the system is given by

$$F(s) = \frac{\hat{v}_{\rm dc}}{\hat{v}_M} = \frac{g_m}{sC_{\rm dc}}. \tag{31}$$

This results in a voltage-loop gain as

$$T_v(s) = F(s) H_v(s) A_v \tag{32}$$

where A_v is scaling factor of the output voltage and H_v is a transfer function of error amplifier. The output voltage controller H_v is implemented with a PI compensator in order to achieve a

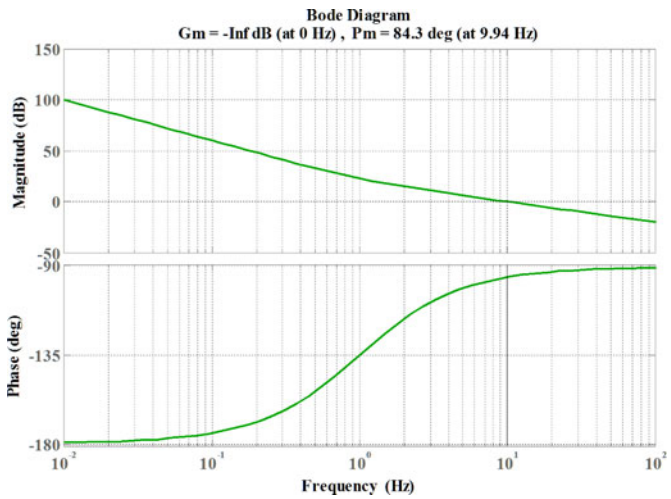

Fig. 9. Bode diagram of output voltage loop gain T_v with PI compensator.

slow voltage loop with a bandwidth lower than 10 Hz as shown in the following:

$$H_v(s) = \frac{w_i}{s}\left(1 + \frac{s}{w_z}\right). \tag{33}$$

Integrator gain w_i and single zero w_z in (33) are determined to let the voltage loop T_v have 10 Hz bandwidth and 90° phase margin to attenuate the half of line period voltage ripple. In the experiment, the compensator zero is placed at $f_z = 1\,\text{Hz}$, and the integrator gain is set to $f_i \approx 8\,\text{Hz}$ to assure no steady-state error in output voltage. Thus, resultant T_v has very low bandwidth and sufficient phase margin, as shown in Fig. 9. In (31), it is notable that outer voltage loop gain of the proposed method is not affected by the line voltage variation. This is an additional benefit for the output voltage regulation since it requires no line voltage feed-forward circuitry.

V. Implementation and Experimental Results of the Modified Carrier Control

A. Implementation

For a single-phase PFC control, analog circuitry has been widely adopted because analog controller ICs available today offer many advantages such as low cost and high performance. On the other hand, with the stringent requirements both on application and performance issues, digital control techniques are also emerging to simplify control circuitry and to implement intelligent control algorithms. However, a pure DSP control is unsuitable for single-phase PFC applications due to cost effectiveness. As a result, a mixed-signal technology or hybrid control combining the benefits of analog and digital controller is preferable [46], [47].

Therefore, the proposed method can be realized by using analog circuitry or hybrid circuitry. Fig. 10(a) shows a feasible implementation of the proposed method using the hybrid control circuitry. To implement the carrier generator block in Fig. 3, analog implementation that contains an integrator with a reset switch and a comparator is advantageous since digital

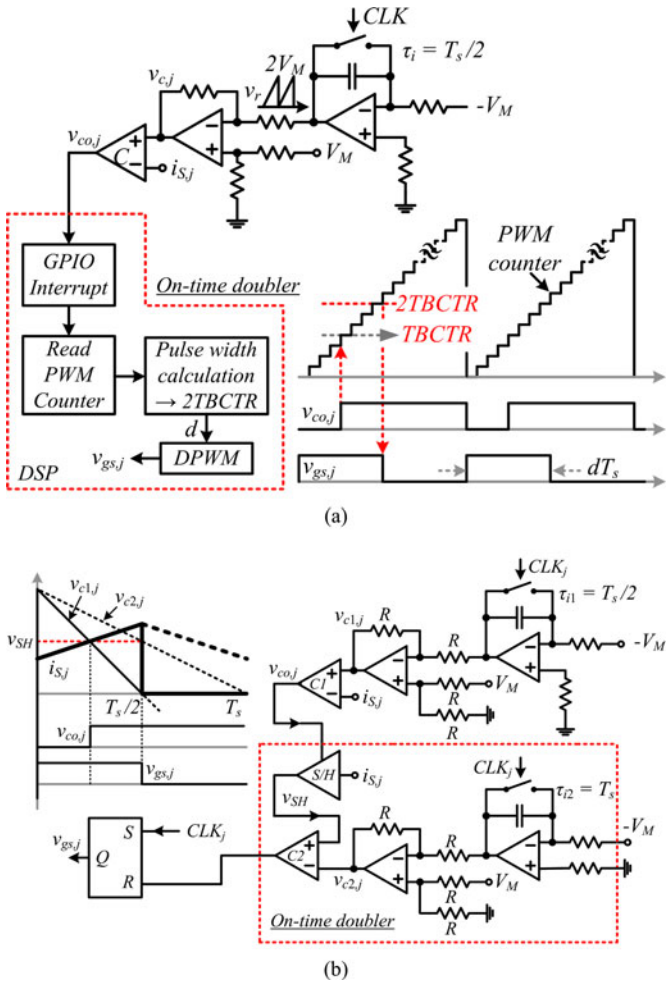

Fig. 10. Feasible implementations of the proposed control technique to boost PFC converter: (a) hybrid method and (b) analog method.

implementation needs very complex high-speed digital-to-analog converter for continuous comparison with sensed switch currents. Also, as the on-time doubler is essential to realize the ACC, digital implementation is able to accomplish (7) precisely. A ramp signal, v_r, is generated by integrating a voltage $-V_M$ with a time constant, τ_i, such that $\tau_i = T_s/2$. The integrator is reset at the beginning of each switching cycle by an external fixed frequency clock signal CLK. The sawtooth carrier signal $v_{c,j}$ as defined in (6) is generated by subtracting v_r from V_M. The output of the comparator, $v_{co,j}$, initiates an external interrupt of DSP when $i_{S,j}$ intersects $v_{c,j}$. As soon as the interrupt occurs, the DSP measures a PWM counter value (TBCTR) at that instant and turns off the switch when the PWM counter value reaches twice the TBCTR to realize (7).

Fig. 10(b) represents another implementation with a pure analog controller which consists of two integrators with reset switches, two comparators, a sample-and-hold, and a SR F/F. This analog version of the controller replaces the digital portion of its hybrid counterpart with the additional components. A sawtooth carrier signal $v_{c1,j}$ as defined in (6) is generated by integrating a voltage $-V_M$ with a time constant τ_{i1} such that $\tau_{i1} = T_s/2$ and by subtracting from V_M. The second sawtooth

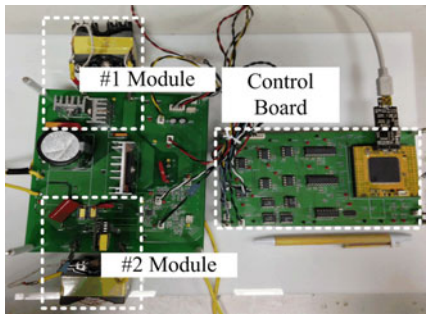

Fig. 11. Hardware of the 600-W two-phase interleaved CCM boost PFC converters.

TABLE I
COMPONENTS AND CIRCUIT PARAMETERS IN THE PROTOTYPE CIRCUIT

Symbol	Parameters	Values
v_{in}	Input voltage	110 V_{rms} / 60 Hz, 220 V_{rms} / 60 Hz
P_o	Output power	600 W
L_1, L_2	Inductor	1.6 *m*H (1.63 *m*H / 1.61 *m*H)
C_{dc}	DC-link capacitor	320 μF for each phase
f_{sw}	Switching frequency	65 kHz

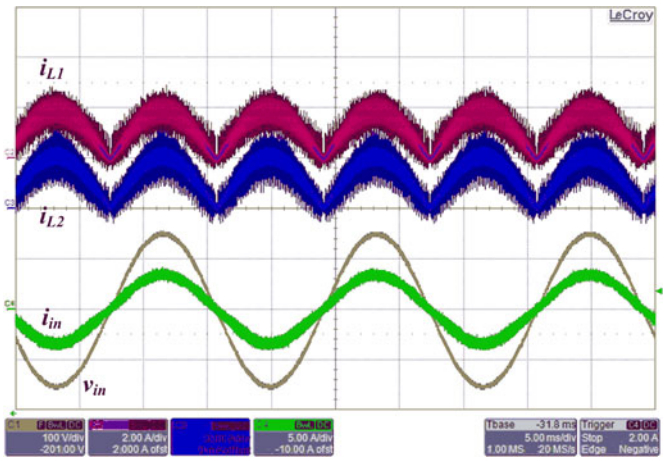

Fig. 12. Measured line voltage, line current, and inductor current waveforms of the proposed control method at $110-V_{\rm rms}$ (i_{L_1}: 2 A/div, i_{L_2}: 2 A/div, $i_{\rm in}$: 5 A/div, $v_{\rm in}$: 100 V/div).

carrier signal $v_{c2,j}$ is generated by integrating a voltage $-V_M$ with a time constant τ_{i2} such that $\tau_{i2} = T_s$ and by subtracting from the v_M as shown in Fig. 10(b). When the sensed switch current $i_{S,j}$ reaches $v_{c1,j}$, the output of the comparator (C_1) samples a sensed switch current and holds the current value v_{SH}. That captured value is compared to $v_{c2,j}$ as illustrated in Fig. 10(b) and determines the turn-off instant of switches by resetting the SR F/F.

B. Experimental Results

The performance of the proposed method has been verified on a 600-W laboratory prototype (300-W per channel). The photograph of the laboratory prototype of interleaved boost PFC converter is shown in Fig. 11. This prototype employs the hybrid control method shown in Fig. 10(a). The key components and

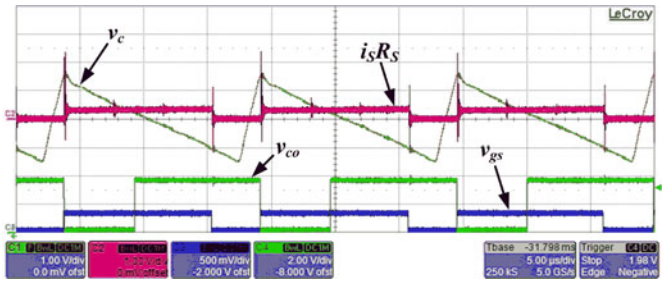

Fig. 13. Operation waveforms.

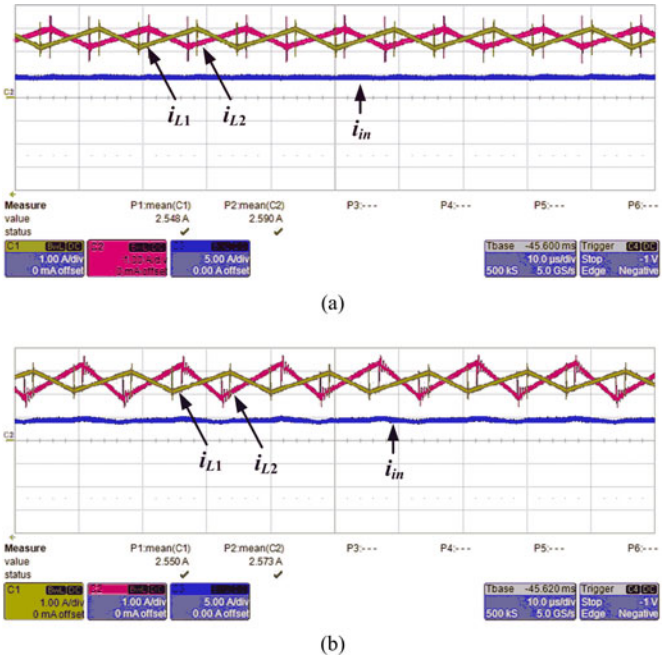

Fig. 14. Detailed inductor ripple current cancellation at $110\text{-}V_{\rm rms}$: (a) without inductance mismatch, $L_1 = 1.63$ mH and $L_2 = 1.61$ mH, (b) with inductance mismatch, $L_1 = 1.61$ mH and $L_2 = 0.98$ mH (i_{L_1}: 1 A/div, i_{L_2}: 1 A/div, $i_{\rm in}$: 5 A/div).

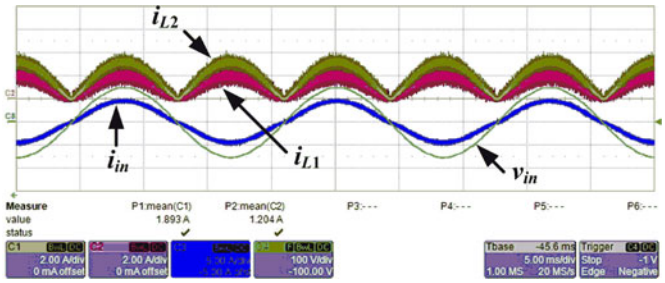

Fig. 15. Measured line voltage, line current, and inductor current waveforms with switch current sensing resistor mismatch (i_{L_1}: 2 A/div, i_{L_2}: 2 A/div, $i_{\rm in}$: 5 A/div, $v_{\rm in}$: 100 V/div).

system specifications of the power circuit are listed in Table I. A TMS320F28335 DSP controller is used to realize the on-time doubler.

Figs. 12 and 13 display experimental waveforms of the prototype converter operation, all of which are in good agreement with the previous discussions. Fig. 12 presents the line voltage $v_{\rm in}$, line current $i_{\rm in}$, and inductor currents i_{L_1} and i_{L_2} for a

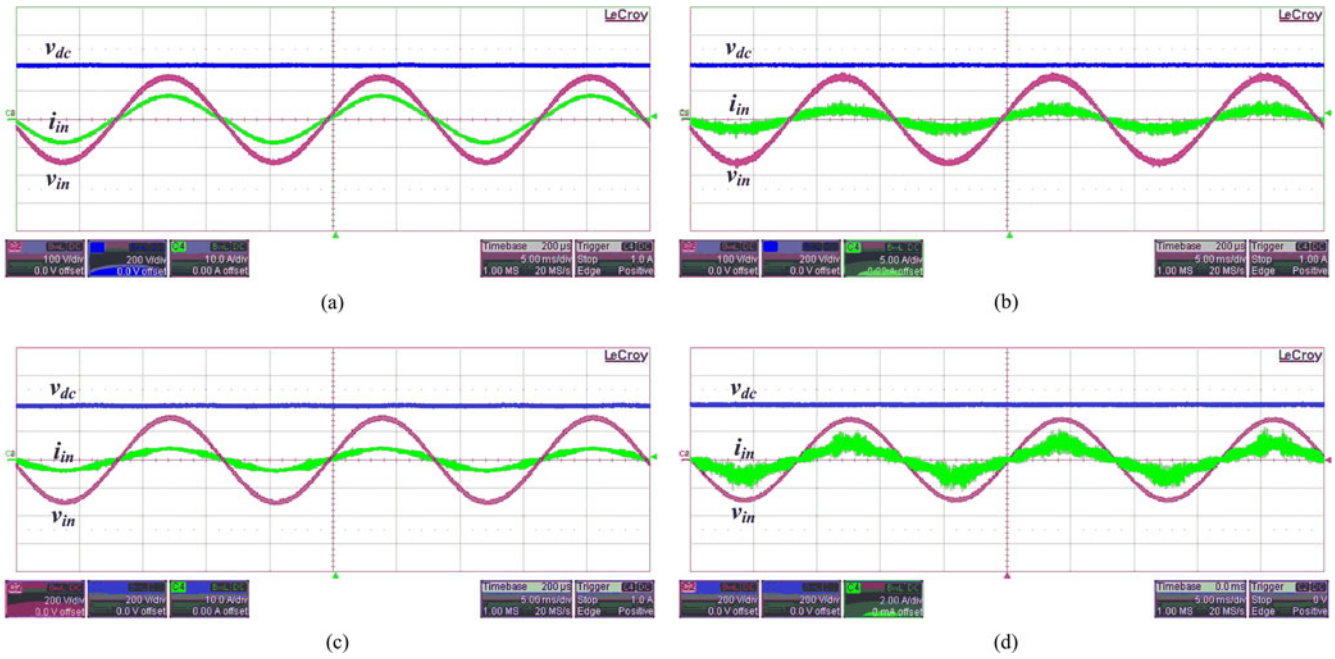

Fig. 16. Steady-state waveforms of the proposed control: (a) 100% load, $V_{\mathrm{in,rms}} = 110\text{-}V_{\mathrm{rms}}$, (b) 20% load, $V_{\mathrm{in,rms}} = 110\text{-}V_{\mathrm{rms}}$, (c) 100% load, $V_{\mathrm{in,rms}} = 220\text{-}V_{\mathrm{rms}}$, (d) 20% load, $V_{\mathrm{in,rms}} = 220\text{-}V_{\mathrm{rms}}$[$v_{\mathrm{dc}}$: 200 V/div, v_{in}: 100 V/div, i_{in}: 10 A/div in (a) and 5 A/div in (b); v_{dc}: 200 V/div, v_{in}: 200 V/div, i_{in}: 10 A/div in (c) and 2 A/div in (d)].

constant 300-W output power. As can be seen, the individual inductor currents follow the sinusoidal line voltage without the inner current loop design as analyzed in Section II. Fig. 13 confirms the operation principle of the proposed control method and validates the analysis presented in Section II.

Concerning the current distribution among interleaved modules, this paper discusses two mismatched conditions: boost inductance mismatch and switch current sensing resistance mismatch. As addressed in Section II, the proposed modulation method lets phase current evenly distributed because it employs common output voltage controller and features ACC. Figs. 14(a) and (b) shows the experimental results of the line and inductor currents of two interleaved PFC converters with matched boost inductance and mismatched boost inductance, respectively. As shown in Fig. 14(a), when the inductances of each module have a tolerance of 2%, $L_1 = 1.63$ mH and $L_2 = 1.61$ mH, the current balancing between two modules was accomplished. Fig. 14(b) shows the line and inductor currents when boost inductances with 40% tolerance are used, i.e., for $L_1 = 1.61$ mH and $L_2 = 0.98$ mH. As can be seen, although the difference in the inductor current ripple amplitude among phases is produced, the average inductor current is evenly distributed as clarified in (10). Therefore, with no additional current balancing circuitry, the proposed method accomplishes multiphase operation. In summary, the proposed modulation method greatly simplifies the implementation for multiphase converter with the inherent current shaping and ACC characteristics as verified in Figs. 12 and 14.

Fig. 15 shows the experimental results of the line and inductor currents of two interleaved PFC converters with mismatched switch current sensing resistances. As can be seen, when the sensing resistances with 1% precision have 33% tolerance, $R_{S1} = 0.1\ \Omega$ and $R_{S2} = 0.066\ \Omega$, the current sharing error between the interleaved PFC converters is 20% as analyzed in (13), whereas, if the tolerance of the sensing resistance is very small, $R_{S1} \approx 0.1\ \Omega$ and $R_{S2} \approx 0.1\ \Omega$, the current sharing error can be neglected, as shown in Fig. 12.

The operation waveforms of the prototype converter at different line and load conditions are arranged in Fig. 16 for further examination. Figs. 16(a) and (b) illustrates the line voltage, the line current, and the dc-link voltage of the prototype converter at $110\text{-}V_{\mathrm{rms}}$ for 100% and 20% load conditions, respectively, whereas Fig. 16(c) and (d) shows them at $220\text{-}V_{\mathrm{rms}}$. The output voltage is regulated at $v_{\mathrm{dc}} = 390$V. At high power and low line, in CCM, the line current and the line voltage are almost in phase, thus maintaining near unity power factor. On the other hand, at medium to light load and high line conditions, a distorted line current is observed around the zero crossings of the line voltage as detailed in Section III.

Fig. 17 shows the measured harmonic contents of the line current along with the IEC61000-3-2 Class D harmonics standard figures. All the data were measured by a Voltech PM6000 power analyzer. It can be seen that the line current harmonics are very small, and it is fully compliant with the IEC 61000-3-2 limits for all specified operation conditions.

Fig. 18 shows the measured power factor and efficiency of the proposed modulated carrier controlled interleaved PFC converter at various load conditions for line voltage of $110\text{-}V_{\mathrm{rms}}$, 60 Hz, and $220\text{-}V_{\mathrm{rms}}$, 60 Hz. For both line voltage conditions, the power factor remains high over the wide load range. The full load efficiency is measured to be 97.87% at the $220\text{-}V_{\mathrm{rms}}$ condition and 95.86% at $110\text{-}V_{\mathrm{rms}}$ condition.

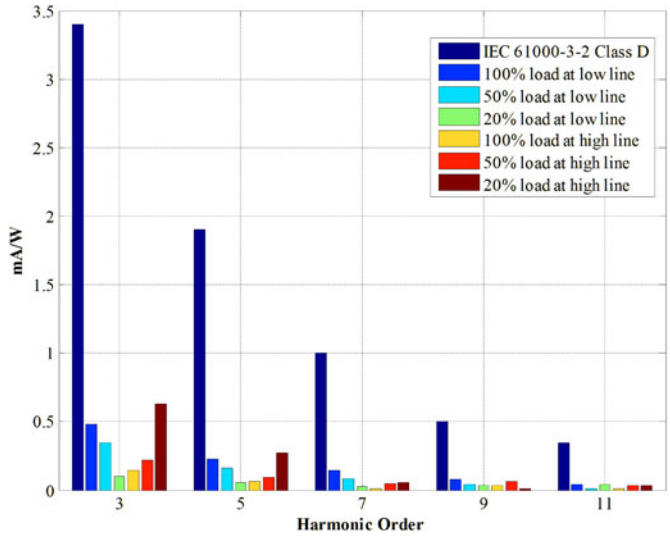

Fig. 17. Measured harmonic contents of line current of the proposed method.

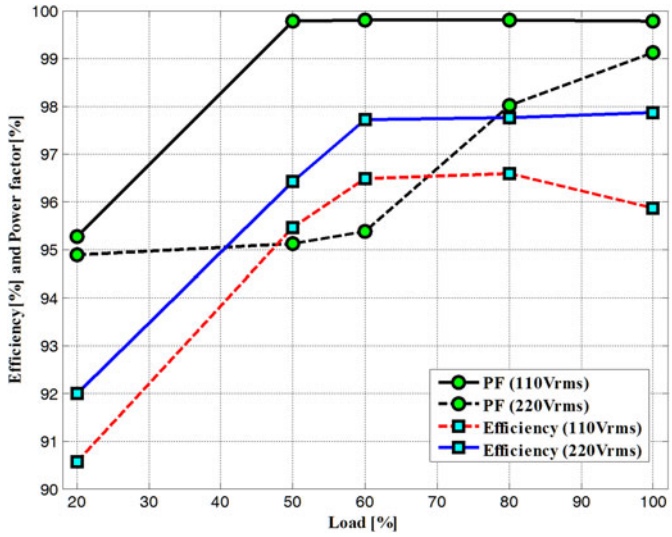

Fig. 18. Power factor and efficiency measurement of the prototype PFC converter.

VI. Conclusion

A new modulated carrier control method for an interleaved CCM PFC boost converter has been proposed. As the proposed modulation scheme realizes the ACC by sampling average current information from the sensed switch current, it is suitable for multiphase PFC converter. Moreover, it does not require the line voltage sensing, the multiplier, and the current loop compensation design owing to its beneficial characteristics in nature, which greatly simplifies control circuitry. The intrinsic features of the proposed method enable a current balancing between the interleaved modules by just letting them use the phase-shifted modulated carrier signals with the same amplitude. The operation principle has been presented and mathematically detailed. In addition, the in-depth analysis of a current distortion resulting from inevitable DCM operation has been derived. Utilizing a practical implementation circuitry, proposed in this paper, a prototype two-module interleaved CCM boost PFC converter is realized to verify the feasibility. The experimental results of the 600-W prototype converter validate the proposed scheme, and they are in good agreement with the aforementioned discussions.

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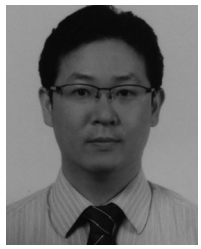

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