A Novel Control Strategy of Suppressing DC Current Injection to the Grid for Single-Phase PV Inverter

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***Abstract*—Photovoltaic (PV) inverters without the isolation transformer become more attractive due to higher efficiency and lower weight. However, it may have dc offset current problem and is critical to the power system. In this paper, a novel control strategy of suppressing dc current injection to the grid for PV inverters is investigated. It is based on the idea of accurately sensing the dc offset voltage of PV inverter output. Since dc component of the inverter output can be eliminated, dc injection to the grid can be effectively suppressed. Finally, the control scheme is verified by the experiment.**

***Index Terms*— DC current injection, dc offset voltage, dc suppression loop, grid, photovoltaic (PV) inverter.**

I. Introduction

DUE to higher efficiency and smaller size, photovoltaic (PV) inverters without isolation transformers become more attractive in grid-connected PV systems [1]–[4], [25]–[36]. However, generally they are unable to automatically suppress dc current injection [5], which may cause the saturation of distribution transformers in the grid and result in poor power quality, higher loss, overheating in the power system [1], [6]–[8], [18]. Consequently, standards and regulations have been formulated to limit PV inverter dc injection to the grid [9]–[11].

To suppress dc injection, some control methods have been proposed [1], [6], [7], [12]–[17], [23]. The methods of dc current injection suppression can be mainly classified into four categories: blocking dc current with the capacitor, novel inverter topology with dc current suppression ability, current-detection control and voltage-detection control. The method of blocking dc current with the capacitor uses a capacitor serially connected between the inverter and the grid [12]. It requires a bulky and expensive capacitor and may cause extra loss. Guo *et al*. [22] developed a method to block dc current by using a virtual capacitor; however, the dynamic response of the closed-loop control system was affected by the virtual capacitor. The method of applying inverter topology with dc current suppression ability uses inherent structure of the inverter topology which can prevent dc current from injecting into the grid, e.g., the half-bridge inverter [13]. However, few practical topologies exist. The method of current-detection control uses current sensors to detect the dc current injection to the grid, but its effectiveness is limited by the accuracy of sensor due to the inherent significant zero-drift characteristic of Hall-effect current sensors. To solve the zero-drift problem, an autocalibrating inverter has been proposed by Armstrong [14]. However, this method requires determining the switch state of the H-bridge in order to measure the inherent zero-drift of the system.

Sharma first introduced a detecting method of dc offset voltage in [21]. A small 1:1 voltage transformer and an *RC* circuit were used to detect the dc offset voltage at the inverter output in the full-bridge grid-connected inverter. And the dc offset in the grid current was eliminated by feeding back the dc offset voltage to the PI controller. Alfock and Bowtell [19] continued studying this method by establishing the mathematical model and verified it. He and Xu [17] used a voltage sensor at the inverter output consisting of a differential amplifier and a low-pass filter. DC offset detected at the output of the low-pass filter is fed back to the controller. A mathematical model is provided in this paper. However, the experimental results under grid mode were not given. The voltage-detection control method uses sensors to detect the dc voltage offset across the ripple filter [15]. This method implies that very low dc voltage across the filter is measured, which is sensitive to noise. A dc offset detection method is proposed by Buticchi [16]. However, this method needs a nonlinear inductor. Hence, a customized inductor should be designed according to specific systems.

In this paper, a novel control strategy to suppress dc current injection of transformerless PV inverters to the grid is investigated. This paper is organized as follows: Section II describes the novel control strategy with dc suppression loop. Section III analyzes the disturbance suppressing effect under the condition without dc suppression loop and with dc suppression loop. Section IV depicts the tuning method of PI controller in the dc offset suppression loop. Section V provides experimental results to verify the theoretical analysis, and the conclusion is given in Section VI.

II. Novel DC Control Strategy

The full-bridge PV inverter without output isolation-transformer is shown in Fig. 1. From Fig. 1, the grid current reference $i_{\rm ref}$ can be expressed as

$$i_{\rm ref} = I_{\rm ref} \cos\theta \tag{1}$$

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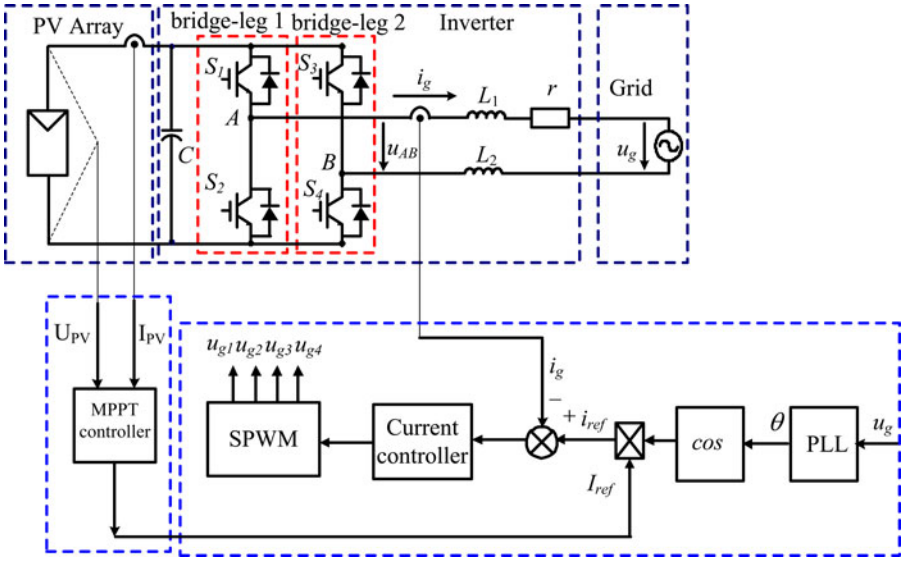

Fig. 1. Original scheme diagram of PV grid-connected inverter.

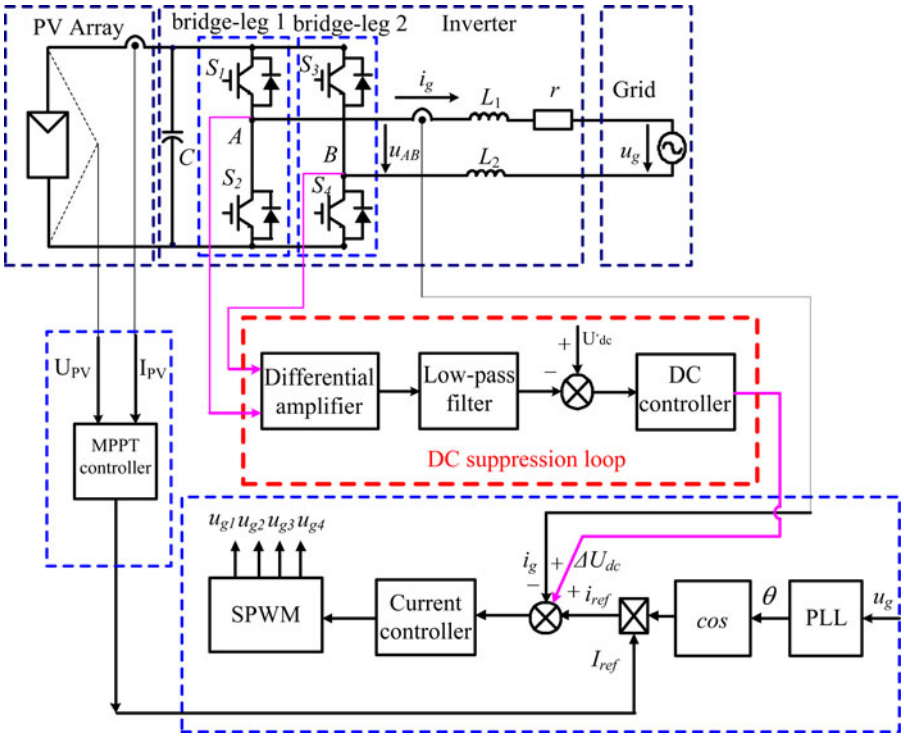

Fig. 2. Novel scheme diagram of PV grid-connected inverter.

where $I_{\rm ref}$ is the amplitude of grid current command, and θ is the phase angle of grid current which is synchronized with grid voltage by phase-locked loop.

PV inverter output generally has dc offset voltage component, which results from disparity of power modules, asymmetry of driving pulses, detection error of current, etc. Traditionally, a transformer is inserted between the PV inverter and the grid. Although the PV inverter output may have dc voltage component, there is no dc current injection to the grid. However, in the case of the PV inverter without isolation transformer, the inverter output dc offset may cause a significant dc current injection to the grid, which may violate the grid connection standards and cannot be neglected [20].

In order to effectively restrain dc current injection to the grid, a control strategy for a single-phase PV inverter without the isolation transformer is shown in Fig. 2 [17], [24].

Compared with Fig. 1, an extra dc offset voltage suppression loop is added to the previous control scheme. The dc suppression loop is composed of a differential amplifier, a low-pass filter, and a dc controller.

The input of dc suppression loop is u_{AB}, which is a high-frequency PWM waveform sampled between the point A of

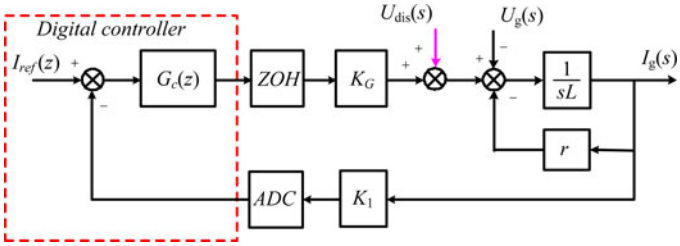

Fig. 3. Control diagram for PV grid-connected inverter.

inverter bridge-leg 1 and the point B of inverter bridge-leg 2. DC offset voltage of u_{AB} is accurately extracted by a differential amplifier and a low-pass filter. Then, it is compared with inverter dc voltage reference $U_{\mathrm{dc\_ref}}$ which is set to zero, and dc offset voltage error is obtained. The error is regulated by the integral controller. Finally, the output of dc controller ΔU_{dc}, which is also the output of dc suppression loop, is added to the grid current reference i_{ref} of the grid current control loop.

The novel control strategy has two significant features. The first is that the differential amplifier is used to sample the dc offset voltage between the two bridge-leg middle points of full-bridge inverter. To accurately detect the dc offset voltage of the inverter switch-side output voltage u_{AB}, a high-precision differential amplifier with low offset and high common-mode rejection ratio is needed. The using of differential amplifier can not only reduce the cost, but also avoid the zero-drift by using Hall-effect sensors. The second one is that dc suppression loop can suppress inverter output disturbances. Therefore, the dc current injected to the grid can be effectively suppressed.

III. Analysis of Disturbance Suppressing Effect

The control block diagram of PV grid-connected inverter is shown in Fig. 3, which is derived from Fig. 1, where $I_{\mathrm{ref}}(z)$ is current reference of the inverter, $G_c(z)$ is digital controller of current loop, and K_G is the gain from the output of current controller $G_c(z)$ to inverter switch-side voltage. $U_{\mathrm{dis}}(s)$ represents the disturbance caused by the turn-on and turn-off difference of the four switches, the saturation voltage difference of the four switches, the gate drive signal delay difference of the four switches, and so on. L is the output filter inductor. r is the equivalent resistance of output filter inductor L. $I_g(s)$ is the grid current of the inverter. K_1 is the feedback gain of current loop. ADC is the analog-to-digital converter which converts the analog sampling value of $I_g(s)$ to digital one. *ZOH* is zero-order holds which is connected in series between the output of digital controller and K_G.

From Fig. 3, the transfer function in s-domain from disturbance source $U_{\mathrm{dis}}(s)$ to grid current $I_g(s)$ with the original control scheme can be derived as follows:

$$\frac{I_g(s)}{U_{\mathrm{dis}}(s)} = \frac{s \cdot e^{-(T_s \cdot s)}}{s(sL+r) + K_1 K_G (K_{pi} s + K_{ii})} \tag{2}$$

where K_{pi} and K_{ii} are the proportional and integral coefficient of current controller, respectively. $e^{-(s \cdot Ts)}$ is the delay effect considering time delay caused by ADC, digital computation and ZOH, where T_s is the duration of sampling period [38], $T_s = 1/f_s$, f_s is switching frequency of PV inverter.

In theory, if both the feedback gain of current loop K_1 and ADC are accurate enough, the dc offset of grid current can be eliminated with PI regulator. However, it is actually limited by ADC resolution and accuracy of the current sensor. The maximum grid dc current detecting error ΔI_g can be calculated as

$$\Delta I_g = \Delta I_{g1} + \Delta I_{g2} \tag{3}$$

where ΔI_{g1} represents error caused by ADC resolution. ΔI_{g2} represents error caused by the error of current sensor and conditioning circuit.

A. Analysis of Detecting Error Caused by ADC

When N-bit ADC is adopted, the DSP sampled digital value I_{gs} of the grid current I_g for the PV grid inverter can be expressed as

$$I_{gs} = I_g \times \frac{2^N}{(1+\beta) \times I_{p\_p}} \tag{4}$$

where I_{p_p} is peak to peak value of the rated grid current, and β represents the overload coefficient of the grid current.

From (4), the detecting error of the grid dc current ΔI_{g1} caused by the ADC resolution is given by

$$\Delta I_{g1} = \frac{(1+\beta) \times I_{p\_p} \times \Delta I_{gs}}{2^N} \tag{5}$$

where ΔI_{gs} is ADC error of the DSP.

B. Analysis of Detecting Error Caused by a Current Sensor and Conditioning Circuit

The grid dc current detecting error ΔI_{g2} caused by the error of the current sensor and conditioning circuit is given by

$$\Delta I_{g2} = \frac{\Delta I_{\mathrm{Lem}}}{K_1'} + \frac{\Delta I_{\mathrm{Con}}}{K_2'} \tag{6}$$

where ΔI_{Lem} and ΔI_{Con} represent the error caused by current sensor and conditioning circuit, respectively. K_1' is current conversion ratio of the current sensor. K_2' is gain of the conditioning circuit. Therefore, by substituting (5) and (6) into (3), the maximum gird dc current detecting error ΔI_g can be calculated as

$$\Delta I_g = \frac{(1+\beta) \times I_{p\_p} \times \Delta I_{gs}}{2^N} + \frac{\Delta I_{\mathrm{Lem}}}{K_1'} + \frac{\Delta I_{\mathrm{Con}}}{K_2'}. \tag{7}$$

Let us take a PV grid inverter as an example with parameters listed as follows. Rated power $P_e = 3$ kW, rated grid voltage $U_g = 220\ \mathrm{V_{rms}}$, peak-to-peak value of the rated grid current $I_{p\_p} = 38.6$ A, overload coefficient of the grid current $\beta = 0.2$, the current sensor accuracy $\Delta I_{\mathrm{Lem}} = \pm 0.1$ mA, and conversion ratio of the current sensor $K_1' = 0.0015$. The conditioning circuit error $\Delta I_{\mathrm{Con}} = \pm 0.2$ mA, the gain of conditioning circuit $K_2' = 0.25$. The ADC error $\Delta I_{gs} = \pm 1.5$ LSB. By substituting the above parameters into (7), the relationship between the ADC bit N and the total grid dc current detecting error ΔI_g is drawn in Fig. 4. The solid line shows the relationship between

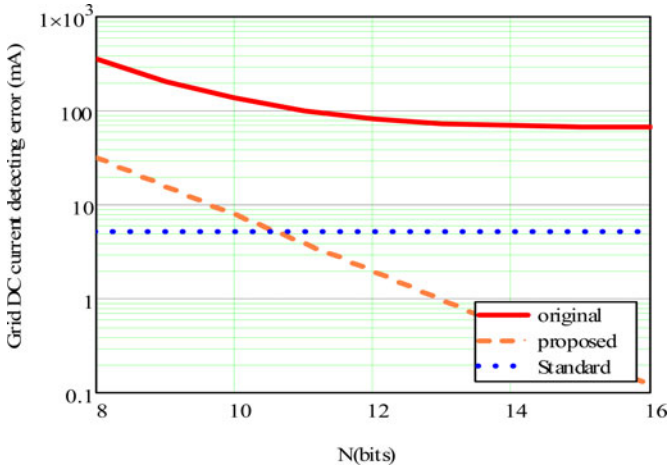

Fig. 4. Relationship between the ADC bits and the grid dc current detecting error, with original control scheme, and with the novel control scheme.

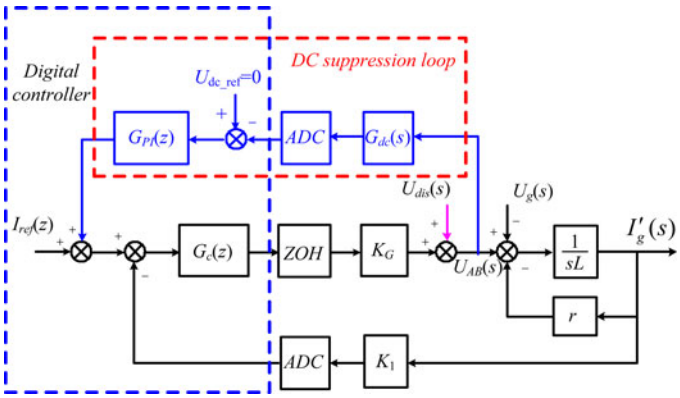

Fig. 5. Control block diagram with novel control scheme.

the ADC bit N and the grid dc current detecting error ΔI_g with the original control scheme. The dotted line is the dc current limit standard [9]–[11]. It can be seen from Fig. 4 that the grid dc current detecting error is larger than the standard value with traditional control.

C. Analysis of Detecting Error With the Novel Control Strategy

In order to realize that the grid dc current detecting error is less than the standard value, the new control scheme is introduced in this paper. As shown in Fig. 5, an extra dc suppressing loop is introduced to the original control scheme of PV grid-connected inverter. $U_{AB}(s)$ is the voltage between the two bridge-leg middle points of full-bridge inverter, and $G_{PI}(z)$ is digital controller of dc suppression loop in z-domain. $G_{\rm dc}(s)$ is the feedback gain of dc suppression loop. $I'_g(s)$ is the grid current of the converter under the new control scheme.

From Fig. 5, the relationship between $U_{AB}(s)$ and the grid current $I'_g(s)$ can be derived as

$$U_{AB}(s) = U_g(s) + (sL + r) \cdot I'_g(s) \tag{8}$$

where L is filter inductor and r is equivalent resistance of the filter inductor. For the dc component of the inverter, (8) can be simplified as

$$I'_{g\_\rm dc} = \frac{U_{AB\_\rm DC}}{r} \tag{9}$$

where U_{AB_DC} is the dc component of $U_{AB}(s)$.

The dc suppression loop in Fig. 5 is designed to detect the dc component of the converter switch-side output voltage $U_{AB}(s)$. The relationship between the dc component of $U_{AB}(s)$ and the DSP sampling value U_{ABs} can be derived as

$$U_{ABs} = U_{AB\_\rm DC} \cdot \frac{2^N}{U_{\rm dc\_max}} \tag{10}$$

where $U_{\rm dc\_max}$ is maximum dc offset voltage. By combining (9) and (10), we obtain

$$I'_{g\_\rm dc} = \frac{U_{\rm dc\_max} U_{ABs}}{2^N r}. \tag{11}$$

Furthermore, the grid dc current detecting error $\Delta I'_{g\_\rm dc}$ with the novel control strategy can be given by

$$\Delta I'_{g\_\rm dc} = \frac{U_{\rm dc\_max} \times \Delta U_{ABs}}{2^N \times r} \tag{12}$$

where ΔU_{ABs} is ADC error of the DSP we used.

Considering the PV grid inverter system: the value of ΔU_{ABs} is $\pm$1.5LSB, maximum dc voltage $U_{\rm dc\_max}$ is 0.5 V, and r is 0.26 Ω. The relationship between the ADC bits and the grid dc current detecting error with the novel control scheme is shown in Fig. 4. The solid line is the relationship between the ADC bits and the grid dc current detecting error with the original control scheme. The dash line is the relationship between the ADC bits and the grid dc current detecting error with the novel control scheme. The dotted line represents the dc current limited standard. It can be seen from Fig. 4 that the grid dc current detecting error is lower than the standard value with the novel control scheme if the ADC number of bits is greater than 9.

D. Comparison of DC Suppressing Effect

From Fig. 5, the transfer function from disturbance source $U_{\rm dis}(s)$ to grid current $I'_g(s)$ in s-domain with the novel control scheme can be derived as

$$\begin{aligned}\frac{I'_g(s)}{U_{\rm dis}(s)} &= s^2 \cdot e^{(-sT_S)} / [s^2 (sL + r) \\ &\quad + K_G \cdot G_{\rm dc}(s) (K_{pi} s + K_{ii}) (K_{pd} s + K_{id}) (sL + r) \\ &\quad + K_1 \cdot K_G \cdot s (K_{pi} s + K_{ii})].\end{aligned} \tag{13}$$

From (2) and (13), the dc current suppression effect is shown in Fig. 6; here, parameters are presented in Table I. It can be seen from Fig. 6, low frequency of dc current suppression effect with the novel control scheme is much better than that with the original control scheme.

IV. Tuning of PI Controller in the DC Offset Suppression Loop

Fig. 7 shows the equivalent control diagram with dc offset suppression loop, which is derived from Fig. 5.

TABLE I
PARAMETERS OF PV INVERTER

Parameter	Symbol	Value
Rated power	P_e	3kW
Grid voltage	U_g	220V
Grid frequency	f	50Hz
DC link capacitor	C	2.75mF
Current loop integral coefficient	K_{ii}	1560
Current loop proportional coefficient	K_{pi}	1.2
Output filter inductance	L_1	5mH
Output filter inductance	L_2	5mH
Switching frequency	f_s	10kHz
DC suppression loop integral coefficient	K_{id}	0.473
DC suppression loop proportional coefficient	K_{pd}	0.015
Feedback gain of current loop	K_1	1/27
Equivalent resistor of output filter inductance	r	0.26Ω
DC feedback gain of DC suppression loop	$G_{dc}(s),s=0$	2
The gain from the output of current controller to inverter switch-side voltage	K_G	360

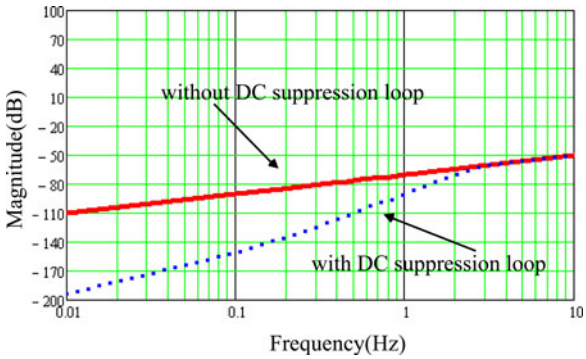

Fig. 6. DC current suppression effect.

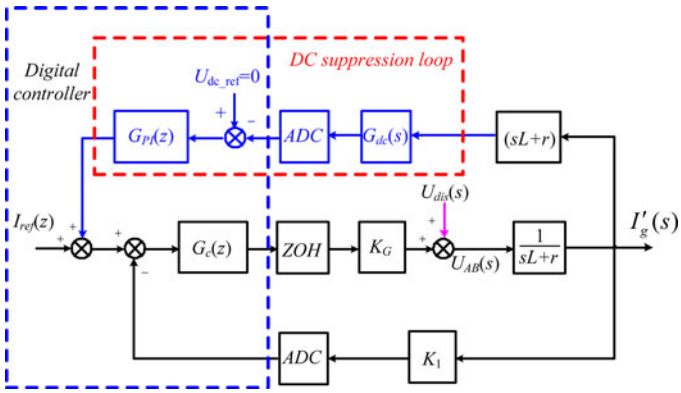

Fig. 7. Equivalent control diagram with DC offset suppression loop.

From Fig. 7, the open-loop uncompensated transfer function of equivalent dc suppression loop can be expressed as

$$G_{\mathrm{dc\_offset}}(s)=\frac{K_G\cdot G_{\mathrm{dc}}(s)\cdot\left(K_{pi}s+K_{ii}\right)\cdot(sL+r)\cdot e^{(-sT_s)}}{Ls^2+\left(r+K_G\cdot K_1K_{pi}\right)s+K_G\cdot K_1K_{ii}} \tag{14}$$

where K_{pi} and K_{ii} are the proportional and integral parameters of current loop, respectively, which are designed as: $K_{pi}=1.2$ and $K_{ii}=1560$. (The bandwidth of current loop is designed as 800 Hz.) $G_{\mathrm{dc}}(s)$ is the feedback gain which includes differential amplifier and low-pass filter, which can be expressed as

$$G_{\mathrm{dc}}(s)=\frac{2}{\left(1+\frac{s}{2\pi f_{LP}}\right)^2} \tag{15}$$

where f_{LP} is the cut-off frequency of the second-order low-pass filter for the dc suppression loop, which has been designed at 3 Hz.

The bandwidth of dc suppressing loop is designed as 1 Hz, which is much smaller than the bandwidth of current loop. The zero-point frequency of PI controllers of dc suppression loop is designed as 5 Hz. Therefore, the proportional coefficient K_{pd} and integral coefficient K_{id} of dc suppression loop can be calculated from the following equations [37]:

$$\begin{cases}\frac{K_{id}}{2\pi K_{pd}}=5\\ \left|G_{\mathrm{dc\_offset}}(s)\cdot\frac{(K_{pd}s+K_{id})}{s}\right|_{s=2\pi\cdot1}=1.\end{cases} \tag{16}$$

From (16), the parameters of the dc suppression loop are finally chosen as $K_{pd}=0.015$ and $K_{id}=0.473$.

V. EXPERIMENTAL RESULTS

The experimental platform is constructed with a 3-kW full-bridge inverter which is used to verify the novel control strategy. The scheme diagram of experimental platform is shown in Fig. 8. The switching frequency of the converter is 10 kHz. The control scheme is implemented with a 32-bit fixed-point DSP TMS320F2808 in the experiments.A shunt resistor 7.5 mΩ is connected in series between the inverter output and the grid in order to measure the dc current injection to the grid. The voltage across the shunt is filtered a low-pass filter (*RC*) with a cut-off

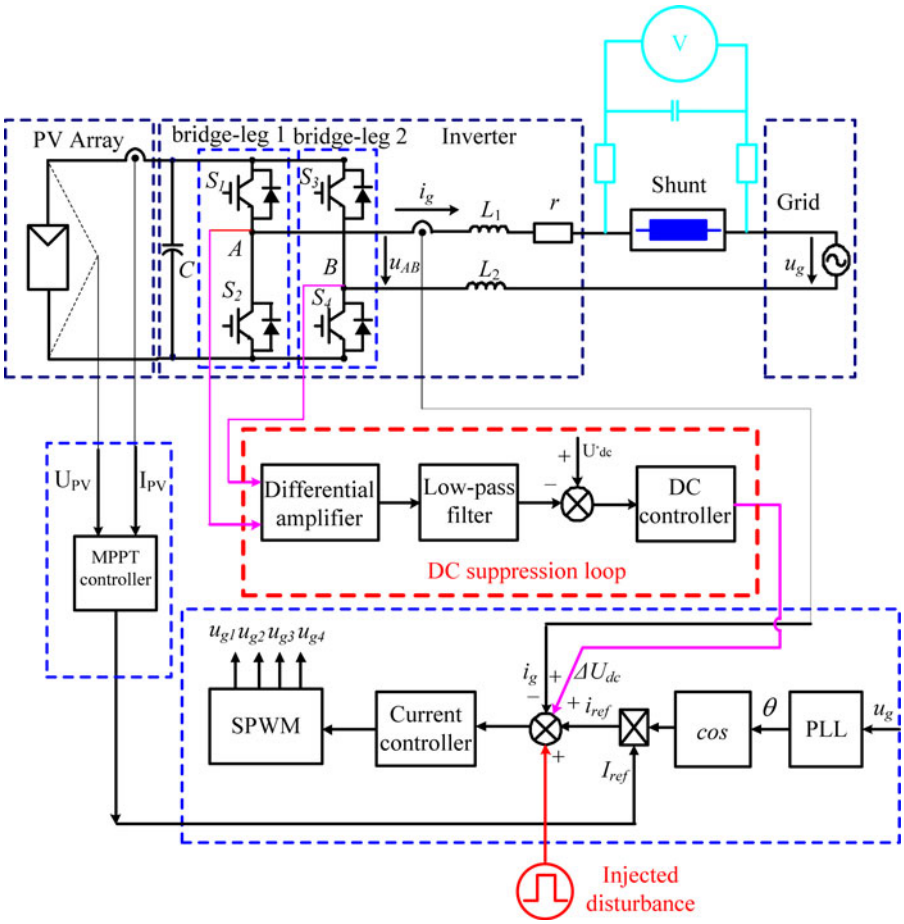

Fig. 8. Scheme diagram of experimental platform.

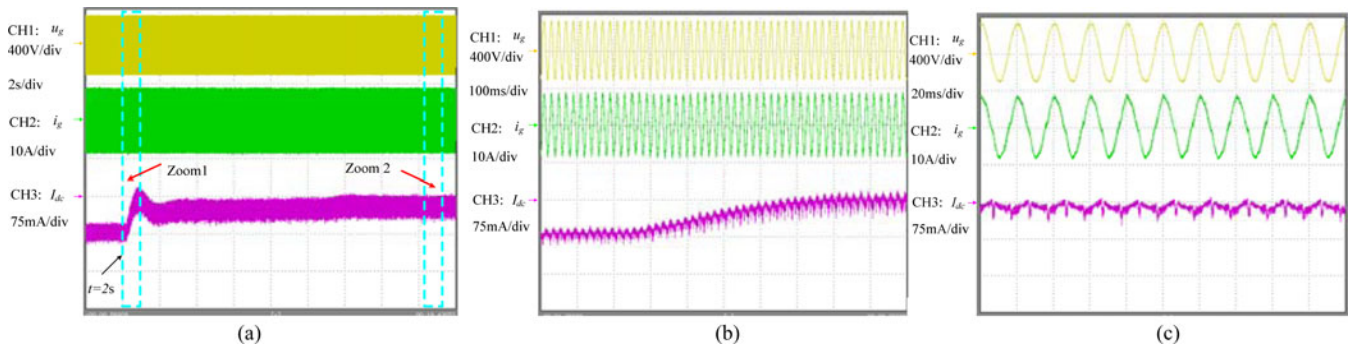

Fig. 9. DC current suppression effect at 37.5% rated power. (a) DC current suppression effect. (b) Zoom 1. (c) Zoom 2.

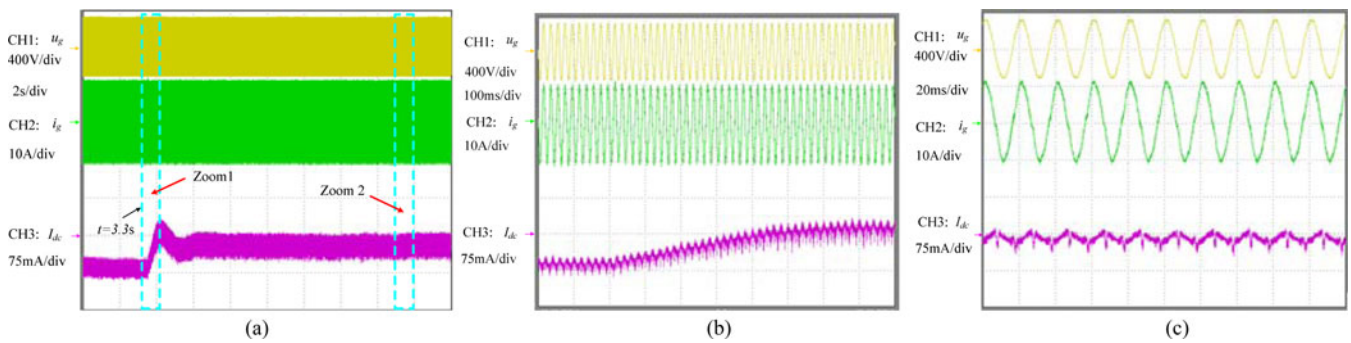

Fig. 10. DC current suppression effect at 50% rated power. (a) DC current suppression effect. (b) Zoom 1. (c) Zoom 2.

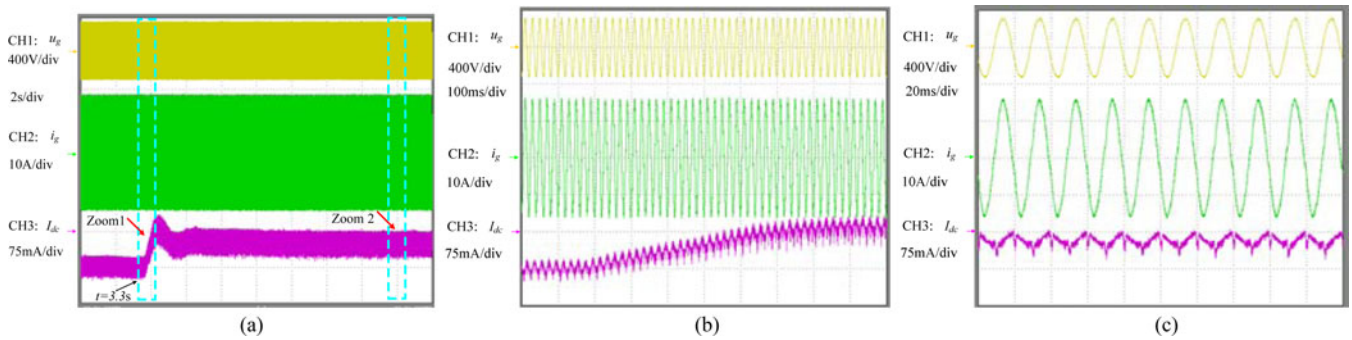

Fig. 11. DC current suppression effect at 75% rated power. (a) DC current suppression effect. (b) Zoom 1. (c) Zoom 2.

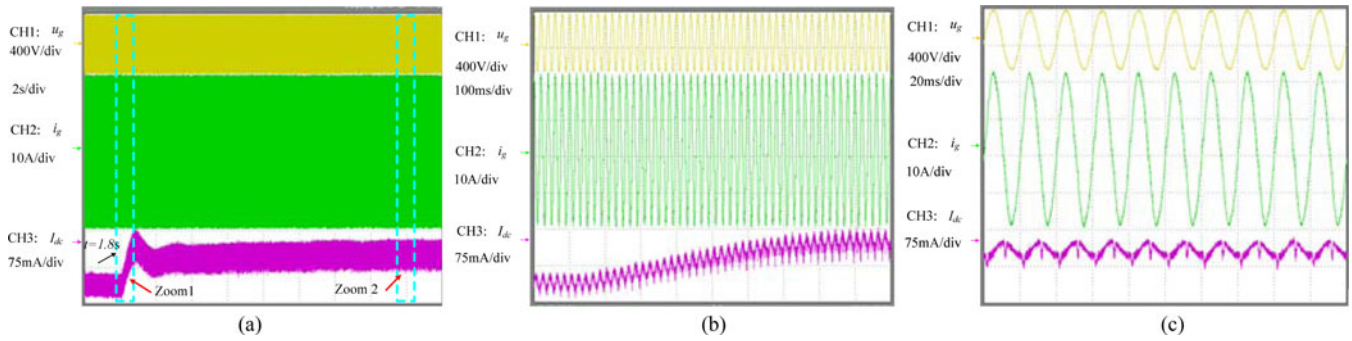

Fig. 12. DC current suppression effect at rated power. (a) DC current suppression effect. (b) Zoom 1. (c) Zoom 2.

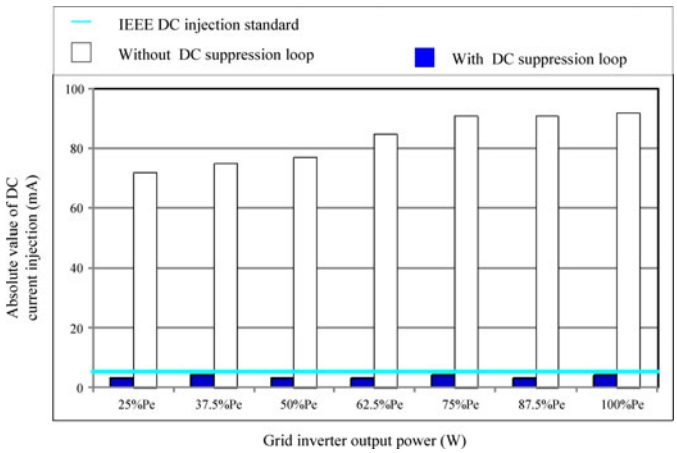

Fig. 13. Comparison of dc suppression effect under different output power.

frequency of 1 Hz in order to suppress 50 Hz component, and a digital multimeter is used to measure the dc offset voltage [23].

The parameters of PV inverter are shown in Table I. Figs. 9, 10, 11, and 12 show the effect of dc suppression loop at 37.5% rated power, 50% rated power, 75% rated power and rated power, respectively. From top to bottom, channel 1 shows the waveform of grid voltage, channel 2 shows the waveform of grid current, and channel 3 shows the waveform of dc injection to the grid. From Fig. 9(a), it can be seen that dc current injection is greatly suppressed by dc suppression loop under 37.5% rated power. Fig. 9(b) shows the waveforms of zoom 1 with dc suppression loop. At first, the dc current injection to the grid by grid inverter is about -75 mA. At the time point $t = 2$ s, the dc suppression loop starts to operate. From Fig. 9(b), it can be seen that the dc current injection decreases under the functioning of dc suppression loop. Meanwhile, waveforms of grid voltage and grid current remain good. Fig. 9(c) shows the steady-state waveforms with the novel control strategy.

From Fig. 10(a), it can be seen that dc current injection is greatly suppressed by dc suppression loop under 50% rated power. Fig. 10(b) shows the waveforms of zoom 1 with dc suppression loop. At first, the dc current injection to the grid by grid inverter is about -77 mA. At the time point $t = 3.3$ s, the dc suppression loop starts to operate. From Fig. 10(b), it can be seen that the dc current injection decreases under the functioning of dc suppression loop. Meanwhile, waveforms of grid voltage and grid current keep good. Fig. 10(c) shows the steady-state waveforms with the novel control strategy.

From Fig. 11(a), it can be seen that dc current injection is greatly suppressed by dc suppression loop under 75% rated power. Fig. 11(b) shows the waveforms of zoom 1 with dc suppression loop. At first, the dc current injection to the grid by grid inverter is about -90 mA. At the time point $t = 3.3$ s, the dc suppression loop starts to operate. From Fig. 11(b), it can be seen that the dc current injection decreases under the operation of dc suppression loop. Meanwhile, waveforms of grid voltage and grid current keep good. Fig. 11(c) shows the steady-state waveforms with the novel control strategy.

From Fig. 12(a), it can be seen that dc current injection is greatly suppressed by dc suppression loop under rated power. Fig. 12(b) shows the waveforms of zoom 1 with dc suppression loop. At first, the dc current injection to the grid by grid inverter

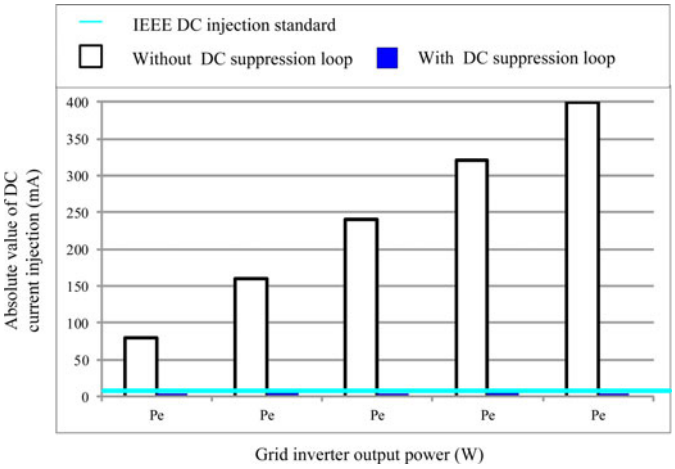

Fig. 14. Comparison of dc suppression effect at rated output power.

is about -92 mA. At the time point $t = 1.8$ s, the dc suppression loop starts to operate. From Fig. 12(b), it can be seen that the dc current injection decreases under the function of dc suppression loop. Meanwhile, waveforms of grid voltage and grid current keep good. Fig. 12(c) shows the steady-state waveforms with the novel control strategy.

Fig. 13 shows the summary of dc suppression effects with dc suppression loop under different inverter output power ratings. The inverter output power changes from 25% rated power to rated power. It can be seen that the absolute value of maximum dc current injection is 92 mA without dc suppression loop, while dc current injection to grid is suppressed below 5 mA with dc current suppression loop over the full power range. Compared with the standards of dc current injection [9]–[11], it can be seen that the novel dc current control strategy can meet the requirement [9]–[11].

To test the ability of dc suppression loop on suppressing disturbance, the dc offset is injected to the reference grid current (see Fig. 8). Fig. 14 shows the dc suppression effect with dc current suppression loop under different disturbances. The inverter output power is fixed at rated power. Inverter is injected with different disturbances to the reference grid current which cause different dc current injections to the grid. The absolute values of dc current injections caused by different disturbances are 80, 160, 240, 320, and 400 mA, which are also the dc current injections without dc suppression loop as shown in Fig. 14. With the dc suppression loop, the dc current injection to grid is able to be suppressed below 5 mA. Compared with the standards of dc current injection [9]–[11], it can be seen that with the novel dc current control strategy the requirement is still fulfilled when different disturbances are injected to the inverter [9]–[11].

VI. Conclusion

This paper investigated a novel control strategy to eliminate dc current injection to the grid for single-phase PV inverter without the isolation transformer. It is based on accurately sensing the dc offset voltage between the two bridge-leg middle points of full-bridge inverter. The novel control strategy is inherently free from offset measurement errors. Both analysis and experimental results show that the novel control strategy can effectively suppress dc injection current of PV system under grid-connected condition.

References

[1] R. Gonzalez, E. Gubia, J. Lopez, and L. Marroyo, "Transformerless single-phase multilevel-based photovoltaic inverter," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2694–2702, Jul. 2008.

[2] T. Kerekes, R. Teodorescu, P. Rodriguez, G. Vazquez, and E. Aldabas, "A new high-efficiency single-phase transformerless PV inverter topology," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 184–191, Jan. 2011.

[3] H. Baeberlin, "Evolution of inverters for grid connected PV-Systems from 1989 to 2000," in *Proc. 17th Eur. Photovoltaic Solar Energy Conf.*, Munich, Germany, Oct. 22–26, 2001, pp. 426–430.

[4] J. M. Carrasco, L. G. Franquelo, J. T. Bialasiewicz, E. Galván, R. C. Portillo Guisado, M. A. M Parts, J. I. León, and N. Moreno-Alfonso, "Power-electronic systems for the grid integration of renewable energy sources: A survey," *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1002–1016, Jun. 2006.

[5] D. G. Infield, P. Onions, A. D. Simmons, and G. A. Smith, "Power quality from multiple grid-connected single-phase inverters," *IEEE Trans. Power Del.*, vol. 19, no. 4, pp. 1983–1989, Oct. 2004.

[6] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep. 2005.

[7] W. M. Blewitt, D. J. Atkinson, J. Kelly, and R. A. Lakin, "Approach to low-cost prevention of DC injection in transformerless grid connected inverters," *IET Power Electron.*, vol. 3, no. 1, pp. 111–119, Jan. 2010.

[8] V. Salas, E. Olías, M. Alonso, F. Chenlo, and A. Barrado, "DC current injection into the network from PV grid inverters," in *Proc. IEEE Photovoltaic Energy Convers. Conf.*, Waikoloa, HI, USA, May 2006, pp. 2371–2374.

[9] AS 4777.2, Grid connection of energy system via inverters. Part 2: Inverter requirements Australia, 2002.

[10] "IEEE recommended practice for utility interface of photovoltaic (PV) systems," IEEE Standard 929-2000, Apr. 3, 2000.

[11] ER G83/1, "Recommendations for the connection of small-scale embedded generators (up to 16 A per phase) in parallel with public low-voltage distribution networks," Eng. Recommendation, U.K., Sep. 2003.

[12] R. González, J. López, P. Sanchis, and L. Marroyo, "Transformerless inverter for single-phase photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 693–697, Mar. 2007.

[13] N. Mohan, T. Undeland, and W. Robbins, *Power Electronics: Converters, Applications and Design*. New York, NY, USA: Wiley, 2002.

[14] M. Armstrong, D. J. Atkinson, C. M. Johnson, and T. D. Abeyasekera, "Auto-calibrating DC link current sensing technique for transformerless, grid connected, H-Bridge inverter systems," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1385–1393, Sep. 2006.

[15] L. Bowtell and A. Ahfock, "Direct current offset controller for transformerless single-phase photovoltaic grid-connected inverters," *IET Renew. Power Gener.*, vol. 4, no. 5, pp. 428–437, Sep. 2010.

[16] G. Buticchi, E. Lorenzani, and G. Franceschini, "A DC offset current compensation strategy in transformerless grid-connected power converters," *IEEE Trans. Power Del.*, vol. 26, no. 4, pp. 2743–2751, Oct. 2011.

[17] G. He and D. Xu, "A novel DC loop current control strategy for paralleled UPS inverter system based on decoupled control scheme," in *Proc. Int. Symp. Ind. Electron.*, Hangzhou, China, May 28–31, 2012, pp. 70–75.

[18] K. Masoud and G. Ledwich, "Grid connection without mains transformers," *J. Electr. Electron. Eng.*, vol. 19, no. 1/2, pp. 31–36, 1999.

[19] T. Ahfock and L. Bowtell, "DC offset elimination in a single-phase grid-connected photovoltaic system," *Australasian Universities Power Engineering Conference*, Melbourne, Australia, Dec. 10–13, 2006.

[20] Wei. Yu, "Key issues research on paralleled UPS systems," Ph.D. dissertation, College Electr. Eng., Zhejiang University, Hangzhou, Zhejiang, China, 2009.

[21] R. Sharma, "Removal of DC offset current from transformerless PV inverters connected to utility," presented at the 40th International Universities Power Engineering Conference, Cork, Ireland, 2005.

[22] X. Guo, W. Wu, W. Herong, and G. San, "DC injection control for grid-connected inverters based on virtual capacitor concept," in *Proc. IEEE Elect. Mach. Syst. Conf.*, Wuhan, China, Oct. 17–20, 2008, pp. 2327–2330.

[23] F. Berba, D. Atkinson, and M. Armstrong, "A review of minimisation of output DC current component methods in single-phase grid-connected inverters PV applications," in *Proc. IEEE Environ.-Friendly Energies Appl. Conf.*, Newcastle upon Tyne, England, Jun. 25–37, 2012, pp. 296–301.
[24] G. He, M. Chen, N. Su, R. Xie, and D. Xu, "A novel control strategy to suppress DC current injection of single-phase PV inverter to the grid," *presented at the IEEE Power Electronics for Distributed Generation Systems Conference*, Rogers, AR, USA, Jul. 8–11, 2013.
[25] B. Yang, W. Li, Y. Gu, W. Cui, and X. He, "Improved transformerless inverter with common-mode leakage current elimination for a photovoltaic grid-connected power system," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 752–762, Feb. 2012.
[26] H. Xiao and S. Xie, "Transformerless split-inductor neutral point clamped three-level PV grid-connected inverter," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1799–1808, Apr. 2012.
[27] Y. Gu, W. Li, Y. Zhao, B. Yang, C. Li, and X. He, "Transformerless inverter with virtual DC bus concept for cost-effective grid-connected PV power systems," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 793–805, Feb. 2013.
[28] D. Dong, F. Luo, D. Boroyevich, and P. Mattavelli, "Leakage current reduction in a single-phase bidirectional AC-DC full-bridge inverter," *IEEE Trans. Power Electron.*, vol. 27, no. 10, pp. 4281–4291, Oct. 2012.
[29] E. Koutroulis and F. Blaabjerg, "Design optimization of transformerless grid-connected PV inverters including reliability," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 325–335, Jan. 2013.
[30] L. Zhang, K. Sun, L. Feng, H. Wu, and Y. Xing, "A family of neutral point clamped full-bridge topologies for transformerless photovoltaic grid-tied inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 730–739, Feb. 2013.
[31] S. Saridakis, E. Koutroulis, and F. Blaabjerg, "Optimal design of modern transformerless PV inverter topologies," *IEEE Trans. Energy Convers.*, vol. 28, no. 2, pp. 394–404, Jun. 2013.
[32] X. Guo, M. C. Cavalcanti, A. M. Farias, and J. M. Guerrero, "Single-carrier modulation for neutral-point-clamped inverters in three-phase transformerless photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2635–2637, Jun. 2013.
[33] Y. Shi, B. Liu, and S. Duan, "Eliminating DC current injection in current-transformer-sensed STATCOMs," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 3760–3767, Aug. 2013.
[34] A. Kulkarni and V. John, "Mitigation of lower order harmonics in a grid-connected single-phase PV inverter," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5024–5037, Nov. 2013.
[35] L. Zhang, K. Sun, Y. Xing, and M. Xing, "H6 transformerless full-bridge PV grid-tied inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1229–1238, Mar. 2014.
[36] J. Lee and K. Lee, "New modulation techniques for a leakage current reduction and a neutral-point voltage balance in transformerless photovoltaic systems using a three-level inverter," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1720–1732, Apr. 2014.
[37] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, 2nd ed. Norwell, MA, USA: Kluwer, 2001.
[38] H. A1-Atrash and I. Batarseh, "Digital controller design for a practicing power electronics engineer," in *Proc. IEEE Appl. Power Electron. Conf.*, Anaheim, CA, USA, Feb. 25–Mar. 1, 2007, pp. 34–41.

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