A High Gain Input-Parallel Output-Series DC/DC Converter With Dual Coupled Inductors

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***Abstract*—High voltage gain dc–dc converters are required in many industrial applications such as photovoltaic and fuel cell energy systems, high-intensity discharge lamp (HID), dc back-up energy systems, and electric vehicles. This paper presents a novel input-parallel output-series boost converter with dual coupled inductors and a voltage multiplier module. On the one hand, the primary windings of two coupled inductors are connected in parallel to share the input current and reduce the current ripple at the input. On the other hand, the proposed converter inherits the merits of interleaved series-connected output capacitors for high voltage gain, low output voltage ripple, and low switch voltage stress. Moreover, the secondary sides of two coupled inductors are connected in series to a regenerative capacitor by a diode for extending the voltage gain and balancing the primary-parallel currents. In addition, the active switches are turned on at zero current and the reverse recovery problem of diodes is alleviated by reasonable leakage inductances of the coupled inductors. Besides, the energy of leakage inductances can be recycled. A prototype circuit rated 500-W output power is implemented in the laboratory, and the experimental results shows satisfactory agreement with the theoretical analysis.**

***Index Terms*—DC–DC converter, dual coupled inductors, high gain, input-parallel output-series.**

I. Introduction

NOWADAYS high voltage gain dc–dc converters are required in many industrial applications [1]–[7], For example, photovoltaic energy conversion systems and fuel–cell systems usually need high step up and large input current dc–dc converters to boost low voltage (18–56 V) to high voltage (200–400 V) for the grid-connected inverters. High-intensity discharge lamp ballasts for automobile headlamps call for high voltage gain dc–dc converters to raise a battery voltage of 12 V up to 100 V at steady operation [8], [9]. Also, the low battery voltage of 48 V needs to be converted to 380 V in the front-end stage in some uninterruptible power supplies and telecommunication systems by high step-up converters [10], [11]. Theoretically, a basic boost converter can provide infinite voltage gain with extremely high duty ratio. In practice, the voltage gain is limited by the parasitic elements of the power devices, inductor and capacitor. Moreover, the extremely high duty cycle operation may induce serious reverse-recovery problem of the rectifier diode and large current ripples, which increase the conduction losses. On the other hand, the input current is usually large in high output voltage and high power conversion, but low-voltage-rated power devices with small on-resistances may not be selected since the voltage stress of the main switch and diode is, respectively, equivalent to the output voltage in the conventional boost converter.

Many single switch topologies based on the conventional boost converter had been presented for high step-up voltage gain [11]–[15]. The cascaded boost converter is also capable of providing high voltage gain without the penalty of extreme duty cycle [16]. However, the voltage stress of the main switch is equal to the output voltage. In [17] and [18], several switching-capacitor/switching-inductor structures are proposed, and transformerless hybrid dc–dc converters with high voltage gain are derived by the use of structures integrated with classical single switch nonisolated PWM converters. They present the following advantage: the energy in the magnetic elements is low, which leads to weight, size, and cost saving for the inductor, and less conduction losses. Another method for achieving high step-up gain is the use of the voltage-lift technique [19], showing the advantage that the voltage stress across the switch is low. However, several diode–capacitor stages are required when the conversion ratio is very large, which makes the circuit complex. In addition, the single switch may suffer high current for high power applications, which risks reducing its efficiency.

Another alternative single switch converters including forward, fly-back and tapped-inductor boost can achieve high conversion ratio by adjusting the turns ratio of the transformer [20]–[22], but these converters require large transformer turns ratio to achieve high voltage gain. In [23], an integrated boost-flyback converter is proposed to achieve high voltage gain, and the energy of a leakage inductor is recycled into the output during the switch-off period. Unfortunately, the input current is pulsed from the experimental results. In addition, it should be noticed that the low-level input voltages usually cause large input currents and current ripples to flow through the single switch for high step up and high power dc–dc conversion, which also leads to increasing conduction losses. Therefore, the

Manuscript received December 8, 2013; revised February 19, 2014; accepted March 20, 2014. Date of publication April 7, 2014; date of current version October 15, 2014. This work was supported in parts by Anhui Provincial Natural Science Foundation under Grant 1408085ME80, Natural Science Foundation of Anhui Education Committee under Grant KJ2012A048, and a Project Funded by the Priority Academic Program Development of Jiangsu Higher Education Institutions. Recommended for publication by Associate Editor F. Costa.

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Digital Object Identifier 10.1109/TPEL.2014.2315613

single-switch topologies are not perfect candidates for high step up dc–dc conversion.

In order to handle high input currents and reduce current ripples, the three-state switching cell based on interleaved control is introduced in boost converters [24]. However, the voltage gain of the conventional three-state switching boost converter is only determined by the duty ratio [18]–[25]. Moreover, the voltage stresses of the power devices are still equivalent to output voltage. Thus, the large duty ratios, high switch voltage stresses, and serious output diode reverse recovery problem are still major challenges for high step up and high power conversion with satisfactory efficiency. To solve aforementioned drawbacks, some three-state switching converters with high static gain employing diode–capacitor cells were presented [25]. However, several diode–capacitor cells are required to meet a very high step-up gain. Thus, other topologies using three-state switching cell and coupled inductors are investigated in [26]–[31]. The authors in [27] proposed an interleaved boost converter with coupled inductors and a voltage doubler rectifier in order to satisfy the high step-up applications and low input current ripple, in which the secondary sides of two coupled inductors are connected in series. The winding-cross-coupled inductors and output diode reverse-recovery alleviation techniques are also introduced in an interleaved three-state switching—dc–dc converters [32], [33], which can get a considerably high voltage conversion ratio and improve the performance of the converter. In [34], an interleaved fly-back converter based on three-state switching cell for high step up and high power conversion is proposed. Although the converter can eliminate the main limitations of the standard fly back, this circuit is a little complex and the input current ripples are large from the experimental results.

This paper proposes an input-parallel output-series boost converter with dual coupled inductors for high step up and high power applications. This configuration inherits the merits of high voltage gain, low output voltage ripple, and low voltage stress across the power switches. Moreover, the presented converter is able to turn ON the active switches at zero current and alleviate the reverse recovery problem of diodes by reasonable leakage inductances of the coupled inductors.

II. Topology and Operation Principle of the Presented Converter

The derivation procedure for the proposed topology is shown in Fig. 1. This circuit can be divided as two parts. These two segments are named a modified interleaved boost converter and a voltage doubler module using capacitor–diode and coupled inductor technologies. The basic boost converter topology shown in Fig. 1(a) and (b) is another boost version with the same function in which the output diode is placed on the negative dc-link rail. Fig. 1(c) is called a modified interleaved boost converter, which is an input-parallel and output-series configuration derived from two basic boost types. Therefore, this part based on interleaved control has several main functions: 1) it can obtain double voltage gain of the conventional interleaved boost; 2) low output voltage ripple due to the interleaved series-connected capacitors; and 3) low switch voltage stresses. Then, the double independent inductors in the modified interleaved boost converter are separately replaced by the primary windings of coupled inductors that are employed as energy storage and filtering as shown in Fig. 1(d). The secondary windings of two coupled inductors are connected in series for a voltage multiplier module, which is stacked on the output of the modified converter to get higher voltage gain. Fortunately, this connection is also helpful to balance the currents of two primary sides. The coupling references of the inductors are denoted by the marks "$*$" and "$\cdot$". The equivalent circuit of the presented converter is demonstrated in Fig. 2, where:

1) $L_{\mathrm{m}1}, L_{\mathrm{m}2}$: magnetizing inductances;
2) $L_{\mathrm{k}1}, L_{\mathrm{k}2}$: leakage inductances;
3) C_1, C_2, C_3: output and clamp capacitors;
4) S_1, S_2: main switches;
5) D_1, D_2: clamp diodes;
6) D_r, C_r: regenerative diode and capacitor;
7) D_3: output diode;
8) N: turns ratio of N_s/N_p;
9) V_{N1}, V_{N2}: the voltage on the primary sides of coupled inductors.

Fig. 3 shows the theoretical waveforms when the converter is operated in continuous conduction mode (CCM). The duty cycles of the power switches are interleaved with 180° phase shift, and the duty cycles are greater than 0.5. That is to say, the two switches can only be in one of three states (S_1: ON, S_2: ON; S_1: ON, S_2: OFF; S_1: OFF, S_2: ON), which ensures the normal transmission of energy from the coupled inductor's primary side to the secondary one. The operating stages can be found in Figs. 4–11.

1) *First stage [t_0–t_1]:* At $t = t_0$, the power switch S_1 is turned on with zero-current switching (ZCS) due to the leakage inductance $L_{\mathrm{k}1}$, while S_2 remains turned ON, as shown in Fig. 4. Diodes D_1, D_2, and D_r are turned OFF, and only output diode D_3 is conducting. The current falling rate through the output diode D_3 is controlled by the leakage inductances $L_{\mathrm{k}1}$ and $L_{\mathrm{k}2}$, which alleviates the diodes' reverse recovery problem. This stage ends when the current through the diode D_3 decreases to zero.

2) *Second stage [t_1–t_2]:* During this interval, both the power switches S_1 and S_2 are maintained turned ON, as shown in Fig. 5 All of the diodes are reversed-biased. The magnetizing inductances $L_{\mathrm{m}1}$ and $L_{\mathrm{m}2}$ as well as leakage inductances $L_{\mathrm{k}1}$ and $L_{\mathrm{k}2}$ are linearly charged by the input voltage source V_{in}.

This period ends at the instant t_2, when the switch S_2 is turned OFF.

3) *Third stage [t_2–t_3]:* At $t = t_2$, the switch S_2 is turned OFF, which makes the diodes D_2 and D_r turned ON. The current flow path is shown in Fig. 6. The energy that magnetizing inductance $L_{\mathrm{m}2}$ has stored is transferred to the secondary side charging the capacitor C_r by the diode D_r, and the current through the diode D_r and the capacitor C_r is determined by the leakage inductances $L_{\mathrm{k}1}$ and $L_{\mathrm{k}2}$. The input voltage source, magnetizing inductance $L_{\mathrm{m}2}$ and leakage inductance $L_{\mathrm{k}2}$ release energy to the capacitor C_2 via diode D_2.

4) *Fourth stage [t_3–t_4]:* At $t = t_3$, diode D_2 automatically switches OFF because the total energy of leakage inductance

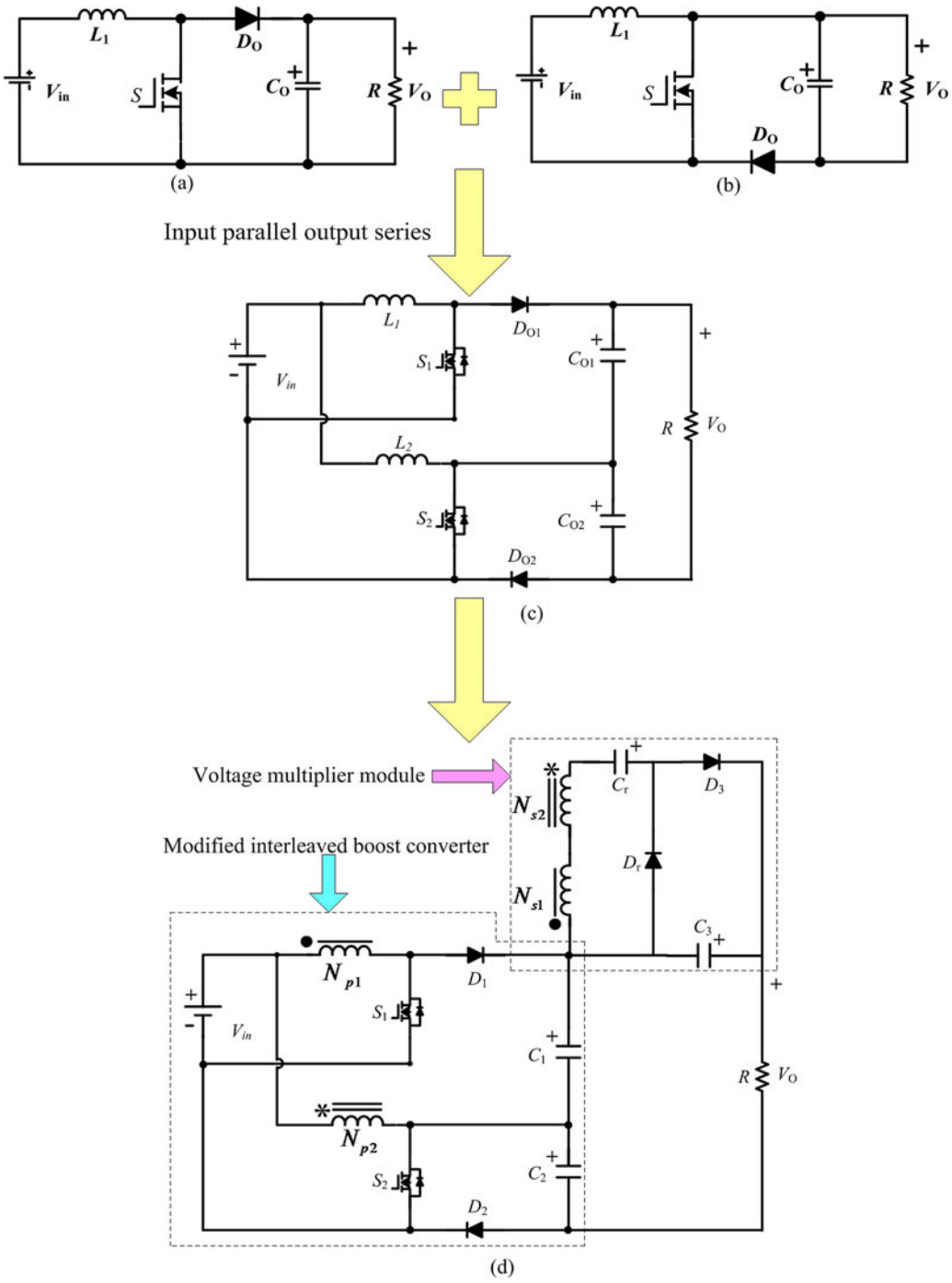

Fig. 1. Procedure to obtain the proposed converter with high voltage gain. (a) Conventional boost converter. (b) Other structure of boost converter. (c) Modified interleaved boost. (d) High gain input-parallel output-series dc/dc converter with dual coupled inductors.

L_{k2} has been completely released to the capacitor C_2. There is no reverse recovery problem for the diode D_2. The current-flow path of this stage is shown in Fig. 7. Magnetizing inductance L_{m2} still transfers energy to the secondary side charging the capacitor C_r via diode D_r. The current of the switch S_1 is equal to the summation of the currents of the magnetizing inductances L_{m1} and L_{m2}.

5) *Fifth stage [t_4–t_5]:* At $t = t_4$, the switch S_2 is turned ON with ZCS soft-switching condition. Due to the leakage inductance L_{k2} and the switch S_1 remains in ON state. The current-flow path of this stage is shown in Fig. 8. The current falling rate through the diode D_r is controlled by the leakage inductances L_{k1} and L_{k2}, which alleviates the diode reverse recovery problem. This stage ends when the current through the diode D_r decreases to zero at $t = t_5$.

6) *Sixth stage [t_5–t_6]:* The operating states of stages 6 and 2 are similar. During this interval, all diodes are turned OFF. The magnetizing inductances L_{m1} and L_{m2}, and the leakage inductances L_{k1} and L_{k2} are charged linearly by the input voltage. The voltage stress of D_1 is the voltage on C_1, and the voltage

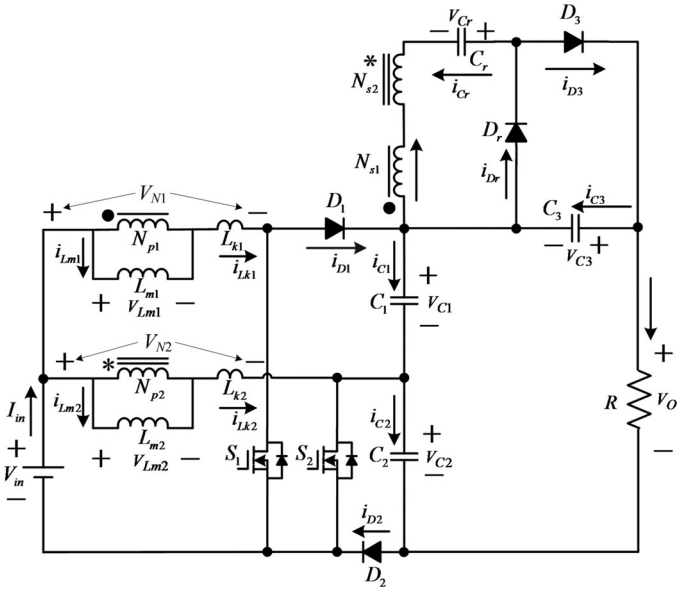

Fig. 2. Equivalent circuit of the presented converter.

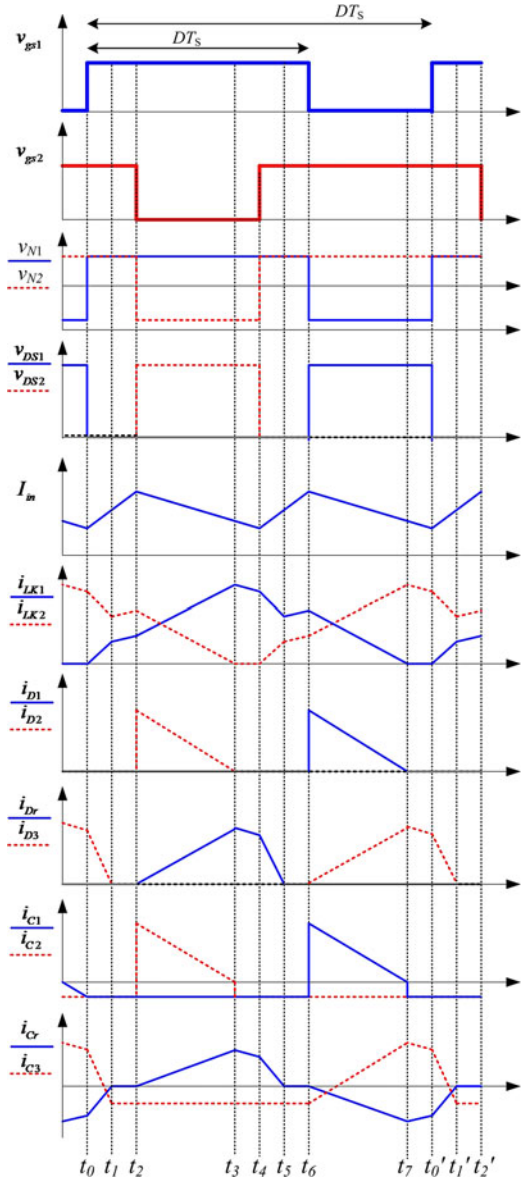

Fig. 3. Key theoretical waveforms.

stress of D_2 is the voltage on C_2. The voltage stress of D_r is equivalent to the voltage on C_r, and the voltage stress of D_3 is the output voltage minus the voltages on C_1 and C_2 and C_r.

7) *Seventh stage [t_6–t_7]:* The power switch S_1 is turned OFF at $t = t_6$, which turns ON D_1 and D_3, and the switch S_2 remains in conducting state. The current-flow path of this stage is shown in Fig. 10. The input voltage source $V_{\rm in}$, magnetizing inductance $L_{\rm m1}$ and leakage inductance $L_{\rm k1}$ release their energy to the capacitor C_1 via the switch S_2. Simultaneously, the energy stored in magnetizing inductor $L_{\rm m1}$ is transferred to the secondary side. The current through the secondary sides in series flows to the capacitor C_3 and load through the diode D_3.

8) Eighth stage [t_7–t_0']: At $t = t_7$, since the total energy of leakage inductance $L_{\rm k1}$ has been completely released to the capacitor C_1, diode D_1 automatically switches OFF. The current of the magnetizing inductance $L_{\rm m1}$ is directly transferred to the output through the secondary side of coupled inductor and D_4 until t_0'.

It should be pointed out that the time periods of stages I, IV, V, and VIII are much shorter than those shown in Fig. 3, which were enlarged in order to clearly show the waveform variations.

III. Steady-State Performance Analysis of the Proposed Converter

To simplify the circuit performance analysis of the proposed converter in CCM, the following conditions are assumed.

1) All of the power devices are ideal. That is to say, the on-state resistance $R_{\rm DS(ON)}$ and all parasitic capacitors of the main switches are neglected, and the forward voltage drop of the diodes is ignored.

2) The coupling-coefficient k of each coupled inductor is defined as $L_{\rm m}/(L_{\rm m} + L_{\rm k})$. The turn ratio N of each coupled inductor is equal to N_S/N_P.

3) The parameters of two coupled inductors are considered to be the same, namely $L_{\rm m1} = L_{\rm m2} = L_{\rm m}, L_{\rm k1} = L_{\rm k2} = L_{\rm k}$, $N_{S1}/N_{P1} = N_{S2}/N_{P2} = N$, and $k_1 = L_{\rm m1}/(L_{\rm m1} + L_{\rm k1}) = k_2 = L_{\rm m2}/(L_{\rm m2} + L_{\rm k2}) = k$.

4) Capacitors C_1, C_2, C_3, and C_r are large enough. Thus, the voltages across these capacitors are considered as constant in one switching period.

A. Voltage Gain Expression

If the transient characteristics of circuit are disregarded, each magnetizing inductance has two main states in one switching period. In one state, the magnetizing inductance is charged by the input source. In the other state, the magnetizing inductance is discharged by the output capacitor voltage V_{C1} or V_{C2} minus the input voltage. Since the time durations of stages I, IV, V, and VIII are significantly short, only stages II, III, VI, and VII are considered for the steady-state analysis. At stages II and VI, the

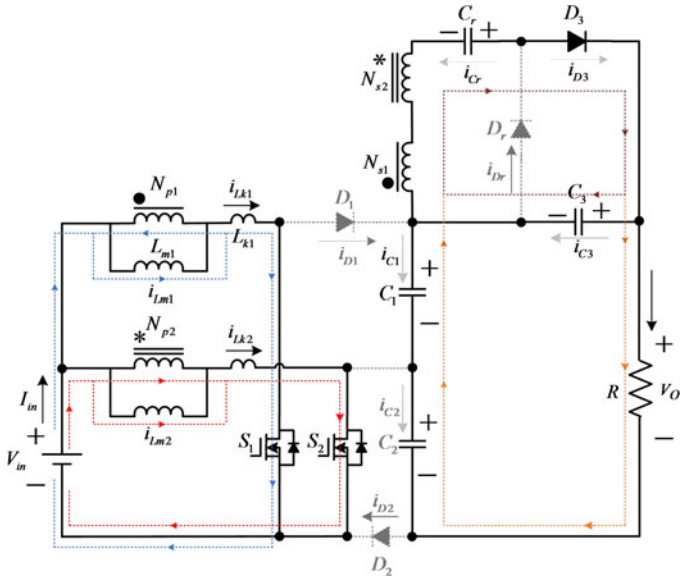

Fig. 4. First stage.

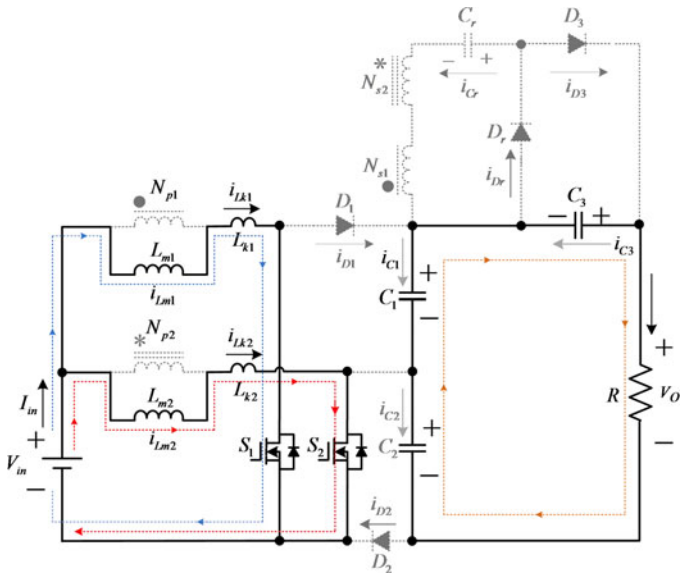

Fig. 5. Second stage.

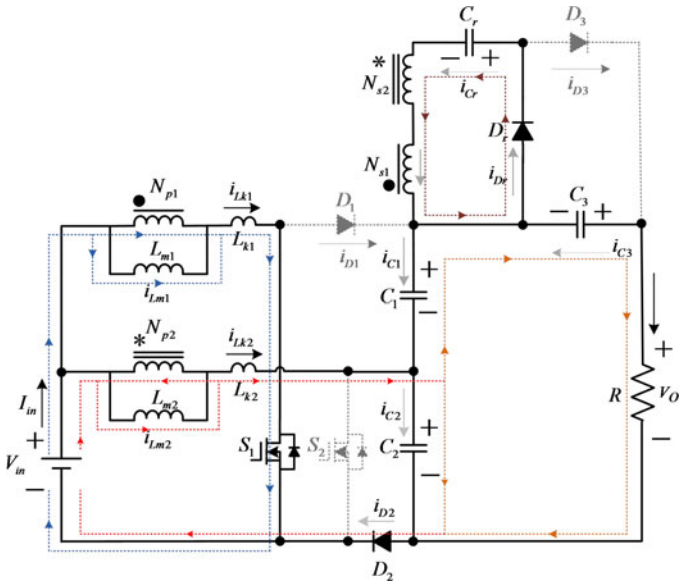

Fig. 6. Third stage.

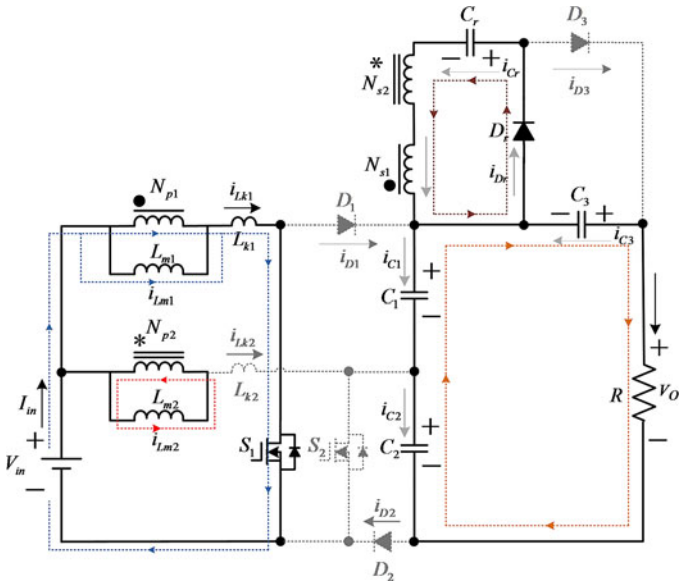

Fig. 7. Fourth stage.

following equations can be written from Figs. 5 and 9:

$$V_{\mathrm{Lm1}}^{\mathrm{II}} = V_{\mathrm{Lm1}}^{\mathrm{VI}} = kV_{\mathrm{in}} \tag{1}$$

$$V_{\mathrm{Lm2}}^{\mathrm{II}} = V_{\mathrm{Lm2}}^{\mathrm{VI}} = kV_{\mathrm{in}} \tag{2}$$

$$V_O = V_{C1} + V_{C2} + V_{C3}. \tag{3}$$

At stage III, the following equations are derived from Fig. 6:

$$V_{\mathrm{Lm1}}^{\mathrm{III}} = kV_{\mathrm{in}} \tag{4}$$

$$V_{\mathrm{Lm2}}^{\mathrm{III}} = k(V_{\mathrm{in}} - V_{C2}) \tag{5}$$

$$V_{Cr} = V_{S1} - V_{S2} = kNV_{C2}. \tag{6}$$

During the time duration of stage VII, the following voltage equations can be expressed based on Fig. 10:

$$V_{\mathrm{Lm1}}^{\mathrm{VII}} = k(V_{\mathrm{in}} - V_{C1}) \tag{7}$$

$$V_{\mathrm{Lm2}}^{\mathrm{VII}} = kV_{\mathrm{in}} \tag{8}$$

$$V_{C3} = V_{Cr} + V_{S2} - V_{S1} = kN(V_{C1} + V_{C2}). \tag{9}$$

Using the volt-second balance principle on L_{m1} and L_{m2}, respectively, the following equation is derived:

$$\int_0^{\frac{(2D-1)T}{2}} V_{\mathrm{Lm1}}^{\mathrm{II}}\,dt + \int_0^{(1-D)T} V_{\mathrm{Lm1}}^{\mathrm{III}}\,dt + \int_0^{\frac{(2D-1)T}{2}} V_{\mathrm{Lm1}}^{\mathrm{VI}}\,dt + \int_0^{(1-D)T} V_{\mathrm{Lm1}}^{\mathrm{VII}}\,dt = 0 \tag{10}$$

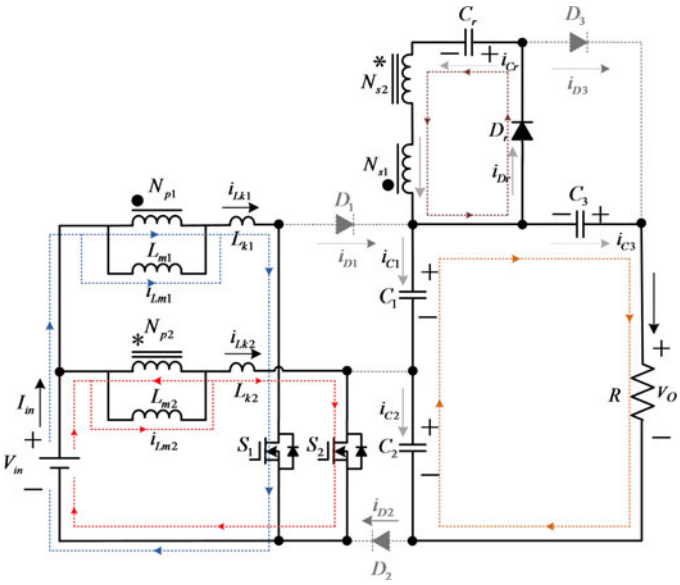

Fig. 8. Fifth stage.

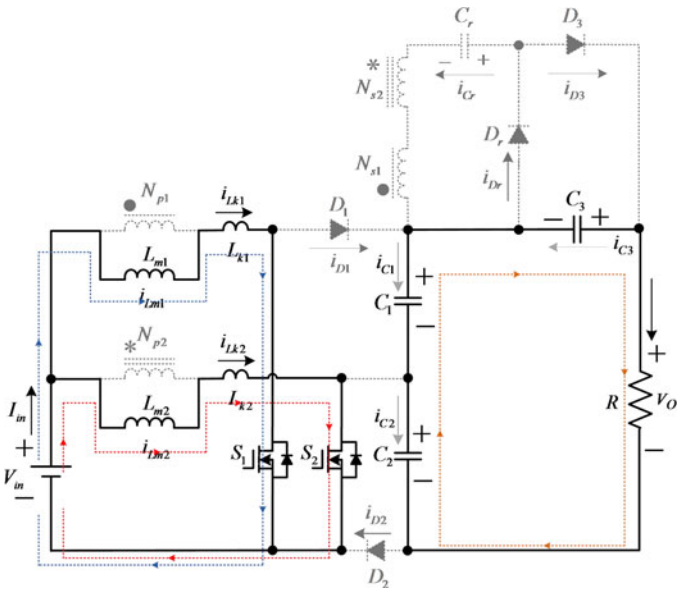

Fig. 9. Sixth stage.

$$\int_0^{\frac{(2D-1)T}{2}} V_{Lm2}^{\mathrm{II}}dt + \int_0^{(1-D)T} V_{Lm2}^{\mathrm{III}}dt + \int_0^{\frac{(2D-1)T}{2}} V_{Lm2}^{\mathrm{VI}}dt + \int_0^{(1-D)T} V_{Lm2}^{\mathrm{VII}}dt = 0 \quad (11)$$

where T is the switching period of the active switches.

Substituting (1), (4), (5), (7), and (8) into (10) and (11), the voltage across capacitors C_1 and C_2 are obtained as

$$V_{C1} = V_{C2} = \frac{V_{\mathrm{in}}}{1-D}. \quad (12)$$

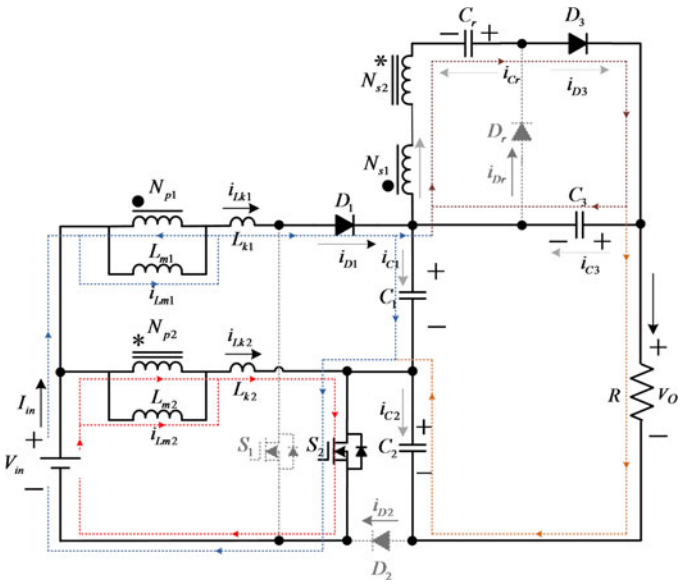

Fig. 10. Seventh stage.

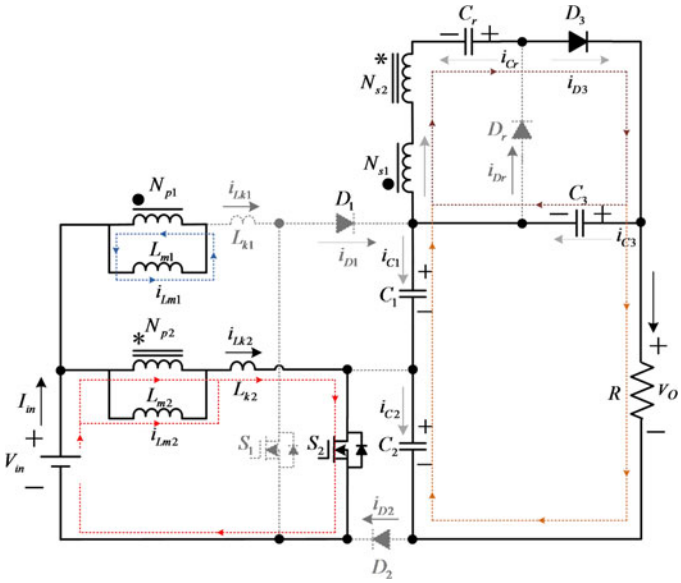

Fig. 11. Eighth stage.

And substituting (12) into (6) and (9), the voltage of capacitors C_r and C_3 are expressed as

$$V_{Cr} = \frac{kN}{1-D}V_{\mathrm{in}} \quad (13)$$

$$V_{C3} = \frac{2kN}{1-D}V_{\mathrm{in}}. \quad (14)$$

Substituting (12) and (14) into (3), the voltage gain is obtained as

$$M_{\mathrm{CCM}} = \frac{V_O}{V_{\mathrm{in}}} = \frac{2(kN+1)}{(1-D)}. \quad (15)$$

Thus, the plot of the voltage gain M_{CCM} versus the duty cycle under various coupling coefficients and turns ratio of the

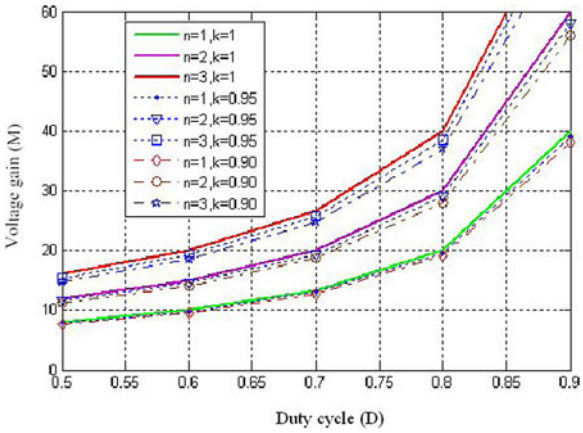

Fig. 12. Static voltage gain curves under different coupling coefficients.

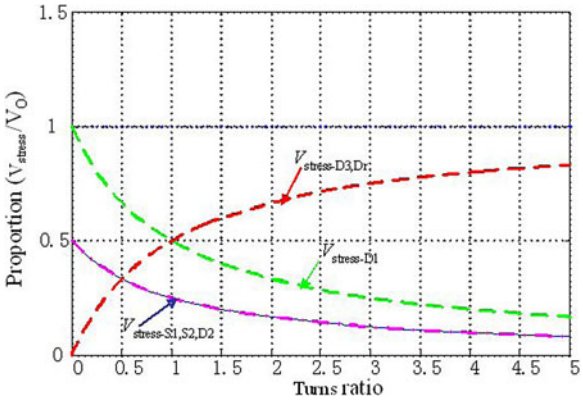

Fig. 13. Voltage stress curve of power devices.

coupled inductor is shown in Fig. 12. It can be seen the coupling coefficient k has only minor influence on the voltage gain. If the impact of the leakage inductances of the coupled inductor is neglected, then coupling coefficient k is equal to one. The ideal voltage gain is rewritten as

$$M_{\mathrm{CCM}} = \frac{V_O}{V_{\mathrm{in}}} = \frac{2(N+1)}{(1-D)}. \tag{16}$$

B. Voltage and Current Stress Analysis

To simplify the voltage stress analyses of the components, the leakage inductance of coupled inductor and the voltage ripples on the capacitors are ignored. The voltage stresses on power switches S_1 and S_2 are derived from

$$V_{S1-\mathrm{stress}} = V_{S2-\mathrm{stress}} = \frac{V_{\mathrm{in}}}{1-D} = \frac{V_O}{2(1+N)}. \tag{17}$$

Equation (17) confirms that low-voltage-rated metal–oxide–semiconductor field-effect transistors with low $R_{\mathrm{DS\text{-}ON}}$ can be adopted for the proposed converter to reduce conduction losses and costs. The relationship between the normalized switch voltage stress and the turns ratio of the coupled inductors is plotted in Fig. 13.

From aforementioned analysis, the voltage stresses on the diodes D_1, D_2, D_3, and D_r related to the turns ratio and the output voltage can be derived as

$$V_{D1-\mathrm{stress}} = \frac{2V_{\mathrm{in}}}{1-D} = \frac{Vo}{(1+N)} \tag{18}$$

$$V_{D2-\mathrm{stress}} = \frac{V_{\mathrm{in}}}{1-D} = \frac{Vo}{2(1+N)} \tag{19}$$

$$V_{D3-\mathrm{stress}} = V_{Dr-\mathrm{stress}} = \frac{2NV_{\mathrm{in}}}{1-D} = \frac{NVo}{(1+N)}. \tag{20}$$

From the steady operation in previous section, the average currents that pass through output capacitors C_1, C_2, C_3, and C_r are equal to the output current at stages II and VI, which are given by

$$I_{C1} = I_{C2} = I_{C3} = -\frac{Vo}{R} \tag{21}$$

$$I_{Cr} = 0. \tag{22}$$

At stage III, the currents flowing through each capacitor are written by

$$I_{C1} = I_{C3} = -\frac{Vo}{R} \tag{23}$$

$$I_{C2} = I_{D2} - \frac{V_O}{R} \tag{24}$$

$$I_{Cr} = I_{Dr}. \tag{25}$$

At stage VII, the average currents that pass through output capacitors are

$$I_{C1} = I_{D1} + I_{C3} + I_{Cr} \tag{26}$$

$$I_{C2} = -\frac{V_O}{R} \tag{27}$$

$$I_{C3} = I_{D3} - \frac{V_O}{R} \tag{28}$$

$$I_{Cr} = -I_{D3}. \tag{29}$$

Using the amp-second principle on capacitors, the following equations can be written:

$$\int_0^{\frac{(2D-1)T}{2}} I_{C1}^{II}dt + \int_0^{(1-D)T} I_{C1}^{III}dt + \int_0^{\frac{(2D-1)T}{2}} I_{C1}^{VI}dt + \int_0^{(1-D)T} I_{C1}^{VII}dt = 0 \tag{30}$$

$$\int_0^{\frac{(2D-1)T}{2}} I_{C2}^{II}dt + \int_0^{(1-D)T} I_{C2}^{III}dt + \int_0^{\frac{(2D-1)T}{2}} I_{C2}^{VI}dt + \int_0^{(1-D)T} I_{C2}^{VII}dt = 0 \tag{31}$$

$$\int_0^{\frac{(2D-1)T}{2}} I_{C3}^{II}dt + \int_0^{(1-D)T} I_{C3}^{III}dt + \int_0^{\frac{(2D-1)T}{2}} I_{C3}^{VI}dt + \int_0^{(1-D)T} I_{C3}^{VII}dt = 0 \tag{32}$$

$$\int_0^{\frac{(2D-1)T}{2}} I_{Cr}^{II}dt + \int_0^{(1-D)T} I_{Cr}^{III}dt + \int_0^{\frac{(2D-1)T}{2}} I_{Cr}^{VI}dt + \int_0^{(1-D)T} I_{Cr}^{VII}dt = 0. \quad (33)$$

Thus, the average currents of the diodes D_1, D_2, D_3, and D_r can be derived

$$I_{D1} = I_{D2} = I_{D3} = I_{Dr} = \frac{Vo}{(1-D)R}. \quad (34)$$

Similarly, according to the steady operating principle, the average currents of the power switches are given by

$$I_{S1} = \frac{D}{1-D} I_{D1} = \frac{DV_O}{(1-D)^2 R} \quad (35)$$

$$I_{S2} = \frac{D}{1-D} I_{D2} + (1-D) I_{D1} = \frac{(D^2 - D + 1)V_O}{(1-D)^2 R}. \quad (36)$$

C. Current Sharing Performance

In order to simplify the current sharing performance analysis, only stages II, III, VI, and VII are considered. When the switch S_1 is turned ON, the average current of diode D_1 is equal to zero. However, the average current that passes through D_1 is equal to the average current of $L_{\rm K1}$ as the power switch S_1 is turned OFF. The following equations can be written:

$$I_{D1}(t) = 0 \quad 0 \le t < DT \quad (37)$$

$$I_{D1}(t) = I_{LK1}(t) \quad DT \le t < T \quad (38)$$

$$I_{D1} = \frac{1}{T}\int_0^T I_{D1}(t)dt. \quad (39)$$

Substituting (37) and (38) into (39), the relationship equation of I_{D1} and $I_{\rm LK1}$ can be given as

$$I_{D1} = \frac{1}{T}\int_0^T I_{D1}(t)dt = \frac{1}{T}\left(\int_0^{DT} 0dt + \int_{DT}^T I_{LK1}dt\right). \quad (40)$$

So the average current flowing through $L_{\rm K1}$ is derived as

$$I_{LK1} = \frac{1}{1-D} I_{D1} = \frac{V_O}{(1-D)^2 R} = \frac{2(N+1)\cdot V_{\rm in}}{(1-D)^3 \cdot R}. \quad (41)$$

Similarly, the average current of diode D_2 is equal to zero during the power switch S_2 is in turn-on state. When the power switch S_2 is in turn-off state, the average current that passes through D_2 is equal to the average current of $L_{\rm K2}$. Thus, the average current flowing through $L_{\rm K2}$ is obtained

$$I_{LK2} = \frac{1}{1-D} I_{D2} = \frac{V_O}{(1-D)^2 R} = \frac{2(N+1)\cdot V_{\rm in}}{(1-D)^3 \cdot R}. \quad (42)$$

TABLE I
PERFORMANCE COMPARISON OF SIMILAR PROTOTYPES

Similar prototypes with high voltage gain	Converter [27]	Converter [29]	Converter [33]	The proposed converter
Quantities of switches	2	2	2	2
Quantities of diodes	4	4	6	4
Quantities of cores	2	3	2	2
Quantities of secondary side windings	1	1	2	1
Voltage gain	$(2N+1)/(1-D)$	$ND+[2/(1-D)]$	$2(N+1)/(1-D)$	$2(N+1)/(1-D)$
Voltage stress on active switch	$V_O/(2N+1)$	$V_O/[2+ND(1-D)]$	$V_O/2(N+1)$	$V_O/2(N+1)$
The maximum voltage stress on diodes	$2NV_O/(2N+1)$	$2V_O/[2+ND(1-D)]$	$(2N+1)V_O/2(N+1)$	$NV_O/(N+1)$

From (41) and (42), the average currents of $L_{\rm K1}$ and $L_{\rm K2}$ are equal, which depend on the turns ratio of coupled inductors, the duty cycles of the power switches, the input source $V_{\rm in}$ and load R. Therefore, if the turns ratio of two coupled inductors are the same as much as possible, the proposed converter has good current sharing performance under symmetrical interleaving control.

D. Key Performance Comparison

For demonstrating the performance of the proposed converter, Table I shows the voltage gain, the number of key components, and normalized voltages stress of semiconductor devices of the proposed converter and other similar converters. These converters can be as a candidate for high step up and high power conversion applications.

One can see that the presented converter has the highest voltage gain and the lowest voltage stress on the active switches as the converter introduced in [33]. And the quantities of diodes and the secondary side windings used in the proposed converter are less than the converter in [33]. Moreover, the maximum voltage stress on diodes of the proposed converter is the lowest among the compared converters when the turns ratio is designed as less than 2.

IV. DESIGN CONSIDERATIONS

A. Coupled-Inductor Design

Usually, the duty cycle should be less than 0.8 to reduce conduction loss of the switches. If the voltage gain and switch duty cycle are selected, the turns ratio of the coupled inductor

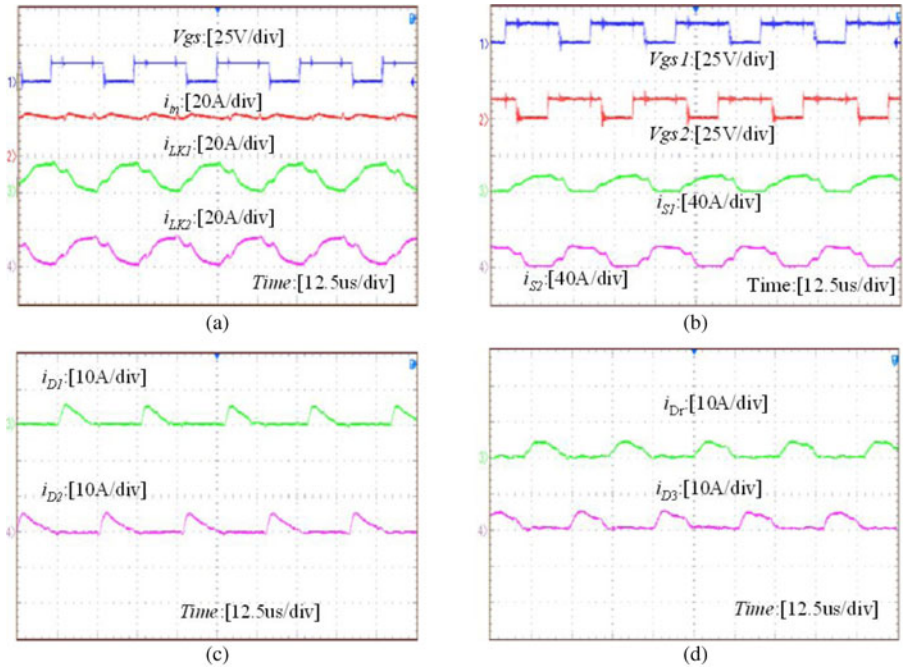

Fig. 14. Key experimental current waveforms.

can be calculated by (43)

$$N = \frac{M_{\mathrm{CCM}}(1-D)}{2} - 1. \tag{43}$$

According to aforementioned analysis, the leakage inductance of the coupled inductors has some effects on the voltage gain. Fortunately, the leakage inductance can be used to limit the diode current falling rate and alleviate the diode reverse recovery problem. Therefore, a compromise should be made to optimize the performance of the converter. Moreover, considering the input current ripples and current sharing performance, the leakage inductance of the coupled inductors should be designed as symmetrical as possible. The relationship of the leakage inductance, the diode current falling rate, and the turns ratio is expressed by the following equation:

$$L_{\mathrm{k1}} = L_{\mathrm{k2}} = \frac{kV_O}{2N(N+1)}\frac{diD_r}{dt} = \frac{kV_O}{2N(N+1)}\frac{diD_3}{dt}. \tag{44}$$

B. Active Switches and Diodes Selection

The voltage rating of the power components have been derived from (17)–(20). In practice, voltage spike may be produced during switch transition process because of the effect of the leakage inductance and parasitic capacitor. Therefore, regarding the margin of safety, the voltage rating of the selected power devices will usually be more than 150% of the calculated value.

C. Considerations of the Capacitor Design

How to suppress the voltage ripple on every capacitor an acceptable value is main consideration. According to $\Delta Q = C \cdot \Delta V_C = I_C \Delta T$, The capacitance of the capacitors C_1, C_2, C_3 or C_r can be estimated by the (45)–(48), in which V_O is the output voltage, $\Delta V_{C1} \sim \Delta V_{C3}$ and ΔV_{Cr} are the maximum tolerant voltage ripple on the capacitors C_1, C_2, C_3 or C_r, f_S is the switching frequency, and R is the load

$$C_1 \geq \frac{D \cdot V_O}{\Delta V_{C1} \cdot R \cdot f_S} \tag{45}$$

$$C_2 \geq \frac{D \cdot V_O}{\Delta V_{C2} \cdot R \cdot f_S} \tag{46}$$

$$C_3 \geq \frac{D \cdot V_O}{\Delta V_{C3} \cdot R \cdot f_S} \tag{47}$$

$$C_r \geq \frac{V_O}{\Delta V_{Cr} \cdot R \cdot f_S}. \tag{48}$$

Generally, the equivalent series resistor (ESR) of an aluminum electrolytic capacitor will be smaller as the capacitance increases. So the capacitor is usually selected to be larger than the calculated value for reducing the power losses caused by the ESR. Moreover, it is a favorable solution that parallel several capacitors are adopted to make the equivalent ESR minimum.

V. Experimental Verifications

In order to verify the operation and evaluate the performance of the proposed three-state switching boost converter with high voltage gain, a prototype was assembled and tested with the specifications defined in the Table II.

Fig. 14 shows some experimental current waveforms. Fig. 14(a) displays the gate signals of S_1, the input current

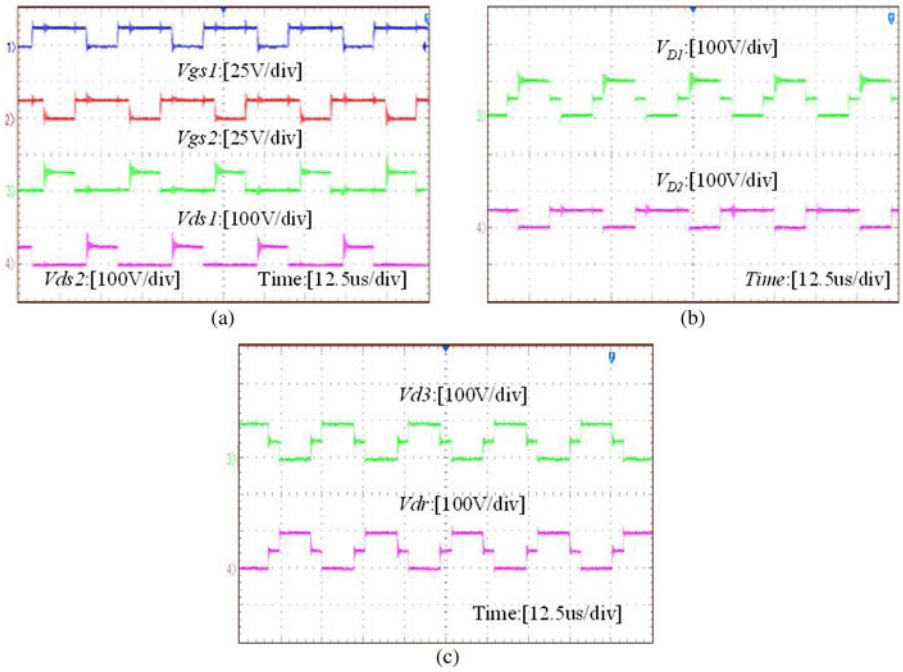

Fig. 15. Voltage stress waveforms of power components.

TABLE II
UTILIZED COMPONENTS AND PARAMETERS OF PROTOTYPE

Components	Parameters
Input voltage V_{in}	18-36V
Output voltage V_O	200V
Maximum output power P	500W
Switching frequency f_s	40kHz
Turns ratio N_s/N_p	19/18
Magnetizing inductor L_m	120uH
Leakage inductor L_{k1},L_{k2}	2.1 uH
Power switches S_1,S_2	FIRFP150N
Diodes D_1 ,D_3 and D_r	DSSK20-015A
Diode D_2	DSSK28-01AS
Capacitors C_1 and C_2	220uF/100 V
Capacitor C_r	47uF/100 V
Capacitor C_3	470uF/ 200V

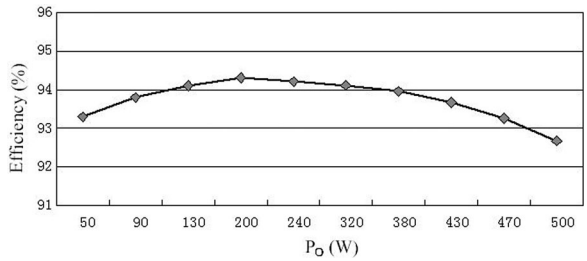

Fig. 16. Measured efficiency of the proposed converter.

$i_{\rm in}$, the primary side leakage inductor currents i_{LK1} and i_{LK2} of the dual coupled inductors. It is seen that the currents i_{LK1} and i_{LK2} are nearly same, which confirms the current sharing performance of the proposed converter. In addition, the input current ripples are very low due to the interleaved operation. Fig. 14(b) shows the gate signals of S_1 and S_2 and current waveforms passing through them. One can see that the active switches are turned ON from ZCS, which reduces the switching losses and the electromagnetic interference noise. Fig. 14(c) and (d) illustrates the experimental waveforms of i_{D1}, i_{D2}, i_{D3}, and i_{Dr}, which agree with the operating principle and the steady-state analysis.

Fig. 15 shows the voltage stress waveforms of main switches and diodes when turns ratio N is 1. From Fig. 15(a), it is seen that the voltage stresses $V_{\rm ds1}$ and $V_{\rm ds2}$ on the main switches are only a quarter of the output voltage during the steady-state period, which is about 50 V. Thus, low voltage ratings and low on-state resistance levels active switches can be selected for high efficiency. Fig. 15(b) and (c) shows that the voltage stresses on the diodes D_1, D_2, D_3, and D_r. One can see that the voltage stresses of the diodes D_1, D_3, and D_r are approximately 100 V, which are equal to half of the output voltage in the steady-state period. The voltage stress of the diode D_2 is only a quarter of the output voltage, approximately 50 V. Therefore, low-voltage-rated Schottky diodes with high performance can be adopted for the presented converter.

Fig. 16 shows the measured conversion efficiency of the proposed converter considering the loss of control circuit. The corresponding efficiency is around 94.37% at Po = 200 W. The full-load efficiency is appropriately 92.76%. In order to

improve the efficiency further, the soft switching and integration magnetic techniques can be used to this converter, which is also the future work.

VI. Conclusion

For low input-voltage and high step up power conversion, this paper has successfully developed a high-voltage gain dc–dc converter by input-parallel output-series and inductor techniques. The key theoretical waveforms, steady-state operational principle, and the main circuit performance are discussed to explore the advantages of the proposed converter.

Some important characteristics of the proposed converter are as follows: 1) it can achieve a much higher voltage gain and avoid operating at extreme duty cycle and numerous turn ratios; 2) the voltage stresses of the main switches are very low, which are one fourth of the output voltage under $N = 1$; 3) the input current can be automatically shared by each phase and low ripple currents are obtained at input; 4) the main switches can be turned ON at ZCS so that the main switching losses are reduced; and 5) the current falling rates of the diodes are controlled by the leakage inductance so that the diode reverse-recovery problem is alleviated. At the same time, there is a main disadvantage that the duty cycle of each switch shall be not less than 50% under the interleaved control with 180° phase shift.

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