Letters

Modular Snubberless Bidirectional Soft-Switching Current-Fed Dual 6-Pack (CFD6P) DC/DC Converter

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***Abstract*—This letter presents a modular naturally clamped snubberless bidirectional soft-switching current-fed dual 6-pack (CFD6P) dc/dc converter to interface two dc buses of large voltage difference such as 24 V and 380 V. It is therefore suitable for energy storage, uninterruptible power system, renewable energy system, vehicle, and micro-grid applications. The proposed novel secondary modulation technique forces the currents through the primary-side (low-voltage side) devices to reverse its direction resulting in zero-current switching (ZCS) or natural commutation of current-fed low-voltage side devices. Secondary-side (high-voltage side) devices are turned-on with zero-voltage switching (ZVS). In addition, the resonance between the device parasitic capacitance and transformer leakage inductance achieves ZVS turn-on of the primary-side devices. Thus, the converter maintains a zero-voltage zero-current switching of the current-fed devices and ZVS of high-voltage devices. High-current applications needs short-circuit protection and that is built-in the converter inherently. It limits the peak current and circulating current through the devices resulting in low kVA rating devices. Steady-state operation, analysis, and design of the proposed converter have been studied and explained. Experimental results for 1-kW laboratory prototype have been demonstrated as a proof of concept to validate the claims.**

***Index Terms*—Current-fed dual 6-pack converter (CFD6P), natural clamping, natural commutation, soft-switching, snubberless.**

I. Introduction

THE traditional power grid is based on centralized generation with high transmission losses. In south Asian countries transmission losses are up to 30% or above. Therefore, a need of local generation close to users with storage and dedicated power electronics resulted in development of distributed generation and microgrid. Low-voltage high-current bidirectional dc/dc converters with high-voltage conversion ratio are required for uninterruptible power system (UPS), electric vehicles, heavy electric vehicles (HEVs), bidirectional chargers, solar photovoltaic power system, battery or ultracapacitor storage, etc. [1].

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Nonisolated converters are simpler in structure and can achieve better efficiency. However, transformer is mandatory while dealing with high-voltage amplification [2] while maintaining low components' count, high reliability, and efficiency. High-frequency (HF) approach has been used to realize a compact, low cost, and light weight system. However, to raise the switching frequency, soft switching is necessary to limit the switching transition losses. Most of the research in the literature focuses on the voltage-fed dual active bridge (VFDAB) topologies and resonant topologies [3]–[5]. On the other hand, current-fed converters have been justified meritorious over voltage-fed converters for such applications mentioned above owing to lower input current ripple, lower transformer turns ratio, no duty cycle loss, reduced peak current stress, low circulating current, and easier current control ability [6], [7]. Usually current-fed converters employ RCD snubber, active clamp or regenerative snubber to absorb device turn-off voltage spike which is a major limitation of current-fed circuits. However, RCD snubber leads to low efficiency owing to energy dissipation by snubber resistor and active-clamp requiring floating active devices and large HF capacitors. We propose a new modulation technique to naturally clamp the device voltage while achieving zero-current commutation of the devices making the circuit snubberless.

In addition, circuit parasitics are utilized to obtain soft-switching avoiding any additional resonant tank or auxiliary transition circuit. The proposed secondary modulation ensures natural commutation with ZCS of the primary switches and ZVS on the secondary switches, thus avoiding the use of active-clamp circuits. Natural voltage clamping of devices is obtained employing the proposed modulation that adds as novel contribution. It solves the traditional problem associated with current-fed topologies. As the current level increases, three-phase serves better substitute in terms of lower rms and peak currents through the devices compared to single-phase full-bridge bidirectional converter with eight devices and also reduction in size of reactive components due to increased 3x ripple frequency. Interleaved converter (each cell sharing equal current/power) has twice the number of components, i.e., 16 devices, and then the switch rms current rating is lower than three-phase converter but at the cost of very high number of devices and components. Therefore, three-phase is a promising solution.

The objectives of this letter are to explain steady-state operation and analysis of the proposed current-fed dual 6-pack (CFD6P) converter (see Section II), and employ the design

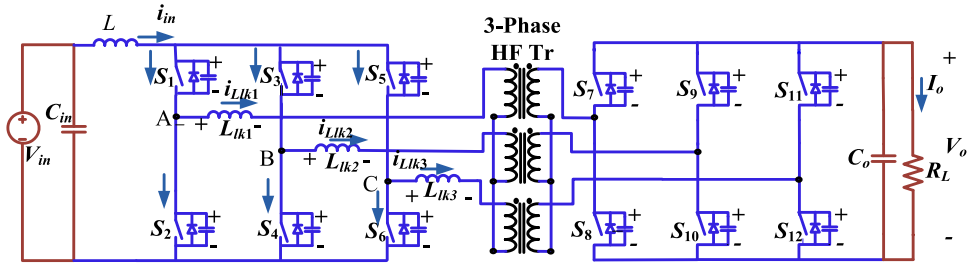

Fig. 1. Proposed snubberless bidirectional current-fed dual 6-pack (CFD6P) converter.

of the converter (see Section III) along with experimental demonstration of results (see Section IV) to validate the operation and claims.

II. Operation and Analysis of the Converter

Fig. 1 shows the circuit diagram of the proposed CFD6P converter. The steady-state operating waveforms are shown in Fig. 2. The steady-state operation of the converter is explained during different intervals for one-third HF cycle using equivalent circuits as shown in Fig. 3. For the rest of the cycle, the intervals are repeated in the same sequence with other symmetrical devices in operation. The gating pulses to the active switches of one leg are 180° phase shifted with some overlap and is met by keeping the duty ratio above 50% as shown in Fig. 2. The duty cycle of the primary switches is the sum of the conduction period of the switches and their body diode. However, the gating pulses to the switches can be removed at any instant during the conducting period of the body diode. A phase difference of 120° is maintained between the switches of three legs of the converter. The secondary-side switches are phase-shifted from the primary switches by 120° for the power to flow from the low-voltage side to high-voltage side. The secondary modulation forces the device current to flow through its body diode reducing device current to zero before it can be naturally turned-off.

The resonance between the leakage inductance and the device parasitic capacitance makes the voltage across primary switches zero before the current rises through the switch resulting in ZVS turn-on. Similarly, secondary devices undergo ZVS turn-on. The proposed modulation is innovative and novel achieving soft-switching of all devices without external resonant tank or auxiliary transition circuit.

Interval 1 (Fig. 3(a); $t_o < t < t_1$): Primary switches S_1 and S_6 and secondary side S_{10} are conducting. The antiparallel body diodes of switches S_7 and S_{12} are conducting and switch S_4 is getting naturally commutated through its antiparallel body diode. In this interval, I_{S6} is higher than I_{in}, the balance flows through the body diode of S_4 that links with L_{lk2}. Hence, $I_{LK3} = I_{S6} = 2I_{in}$, $I_{D4} = I_{lk2} = I_{S6} - I_{in}$.

Interval 2 (Fig. 3(b); $t_1 < t < t_2$): The switch S_3 is turned-on at $t = t_2$ by discharging the parasitic capacitor C_{S3}. However, the gating pulses to S_3 is applied at $t = t_1$. The resonance between the device parasitic capacitance (C_{S3}), parasitic capacitances of two forward blocked switches (C_{S2} and C_{S5}), and

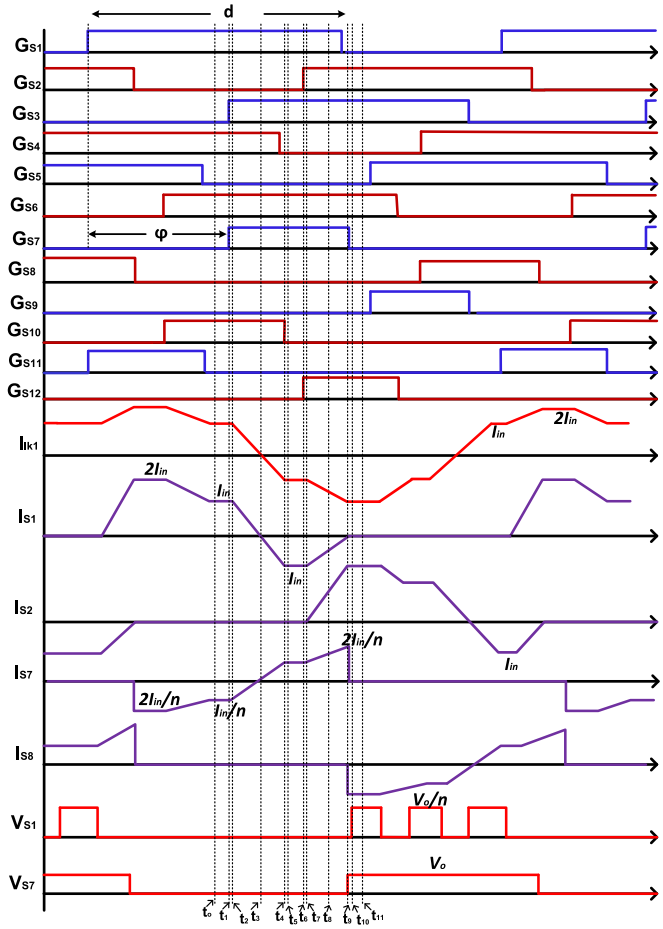

Fig. 2. Steady-state analytical waveforms of the proposed current-fed dual 6-pack (CFD6P) dc/dc converter.

three leakage inductances results in soft-start and ZVS turn-on of primary switch.

Interval 3 (Fig. 3(c); $t_2 < t < t_3$): The switches S_3 and S_7 start conducting with ZVS. The body diode conduction before the switch S_7 takes over help to achieve ZVS of the secondary switches.

Interval 4 (Fig. 3(d); $t_3 < t < t_4$): The current through S_7 reverses the polarity of the voltage across the transformer. This, results in reversing of the current through L_{lk1} which makes the antiparallel body diode D_{S1} of switch S_1 to conduct. The current through D_{S1} of switch S_1 starts rising up with the same

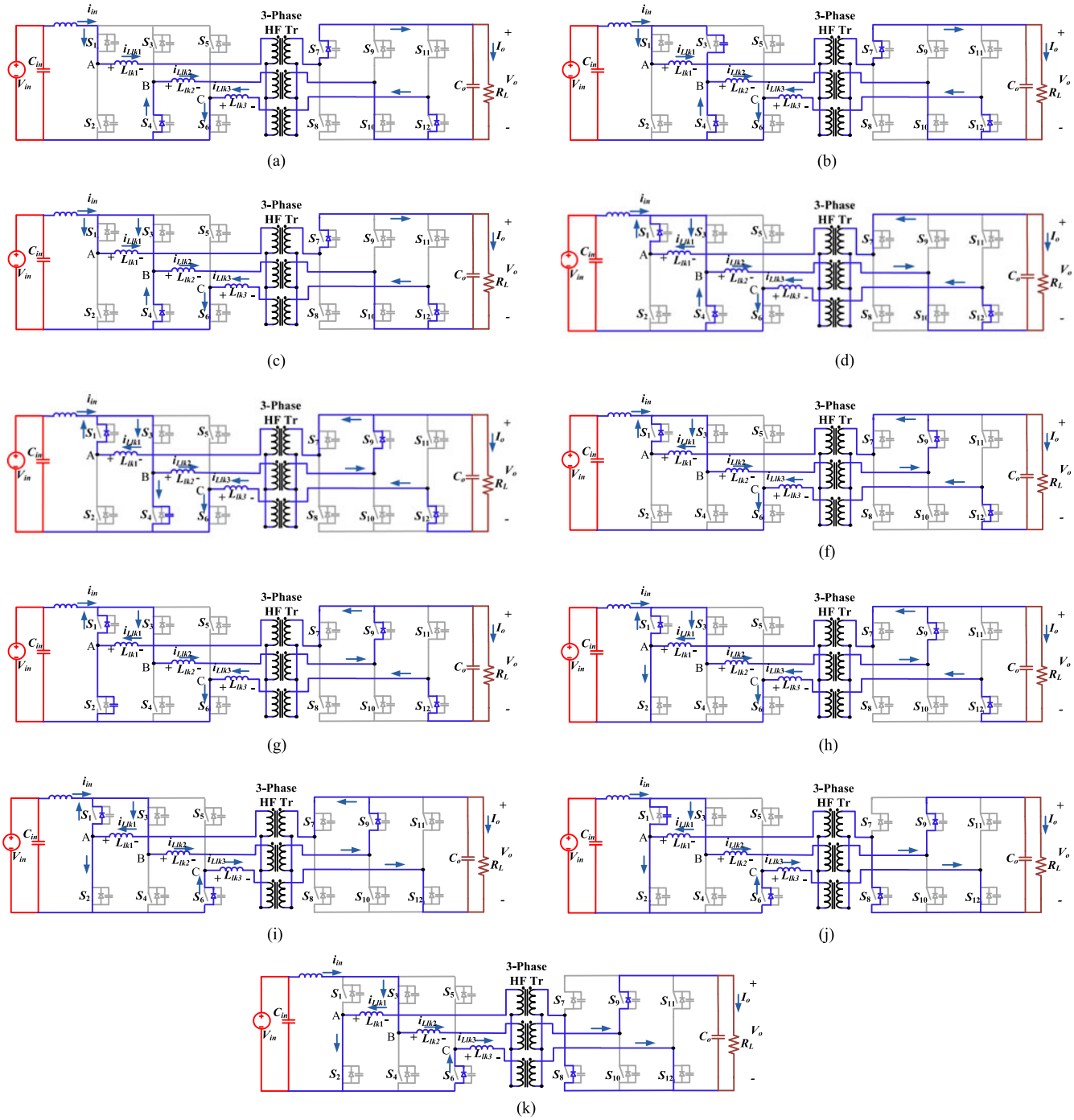

Fig. 3. Different modes of operation of the proposed converter.

slope as L_{lk1} resulting in natural commutation of S_1 with ZCS turn-off.

Interval 5 (Fig. 3(e); $t_4 < t < t_5$): The parasitic capacitance of switch S_4 charges to V_0/n. This mode ends when switch S_4 enters into forward blocking mode and thus, the device voltage is clamped naturally.

Interval 6 (Fig. 3(f); $t_5 < t < t_6$): The value of the current through the leakage inductances and the switches remain same. The input current flows through the active switch S_3 and switch S_6. The antiparallel body diode D_{S1} conducts for zero-current commutation of switch S_1.

Interval 7 (Fig. 3(g); $t_6 < t < t_7$): The device parasitic capacitance of switch S_2 (C_{S2}) and parasitic capacitances of two forward blocked switches (C_{S4} and C_{S5}) resonates with three leakage inductances. The switch voltage drops down to zero before the switch S_2 is turned-on with ZVS. This mode persists for a short duration of time and the current through all the components remain the same.

Interval 8 (Fig. 3(h); $t_7 < t < t_8$): Switches S_2, S_3 and S_7 are conducting. This mode ends when the current through switch S_6 drops down to zero and S_{12} conducts with ZVS.

Interval 9 (Fig. 3(i); $t_8 < t < t_9$): During this mode of operation, devices S_2, S_3 and S_{12} are conducting and antiparallel body diode of D_{S6} of switch S_6 takes over. Therefore, switch S_6 gets naturally commutated. The current through body diode D_{S1} of switch S_1 is zero resulting in its ZCS turn-off.

Interval 10 (Fig. 3(j); $t_9 < t < t_{10}$): At the end of this mode, device S_1 parasitic capacitance is naturally clamped to V_0/n. The voltage and current through other components remain the same.

Interval 11 (Fig. 3(k); $t_{10} < t < t_{11}$): The current through all three primary windings and devices (primary and secondary) remain constant. Switch S_6 is getting naturally commutated with $-I_{\rm in}(I_{\rm DS,peak})$ through its body diode.

In one third HF cycle, current has been transferred from one phase of primary to the other one. The only condition to fulfil to achieve soft-switching is proper design of leakage or series inductance value. It decides the slope of current falling in switch in one-leg as a result of secondary modulation and gets transferred to the other phase resulting in its natural ZCS turn-off. It should be done within time interval of $(d-0.5)T_s$. It is determined by analysis within intervals 2 to 5 of this duration with voltage $V_o/3$ appearing across the primary leakage inductance.

III. Design of the CFD6P Converter

The steady-state analysis of the CFD6P converter resulted in the following equations to determine the components' value. The voltage conversion ratio is obtained by applying volt-second balance across the boost inductor and is obtained by

$$V_o = \frac{nV_{\rm in}}{2(2-3d)}. \tag{1}$$

The leakage inductance of the transformer is given by the slope of the current through the same as

$$L_{lk} = \frac{V_o(2d-1)}{6nI_{\rm in}f_s}. \tag{2}$$

The value of the main inductor is given by

$$L = \frac{V_{\rm in}(2d-1)}{2\Delta I_{\rm in}f_s}. \tag{3}$$

For the specifications of input voltage $V_{\rm in} = 24$ V, output voltage $V_o = 380$ V, switching frequency $f_s = 100$ kHz, output power $P_o = 1$ kW, duty cycle $d = 0.611$, the calculated values of $n = 5.4$, $L_{lk} = 0.65$ μH, $L = 12$ μH for $\Delta I_{\rm in} = 5\%$.

IV. Experimental Results

A laboratory prototype rated at 1 kW is designed and developed in research lab to validate the proof of concept. Experimental results demonstrate the proposed operation, similar performance, and verify the claims and proposal. The gating pulses are generated through Xilinx FPGA board. The details of the components are shown in Table I. In order to achieve voltage boost, the gating signals of devices in one leg have overlap to implement energy storage interval, and the duty cycle is always

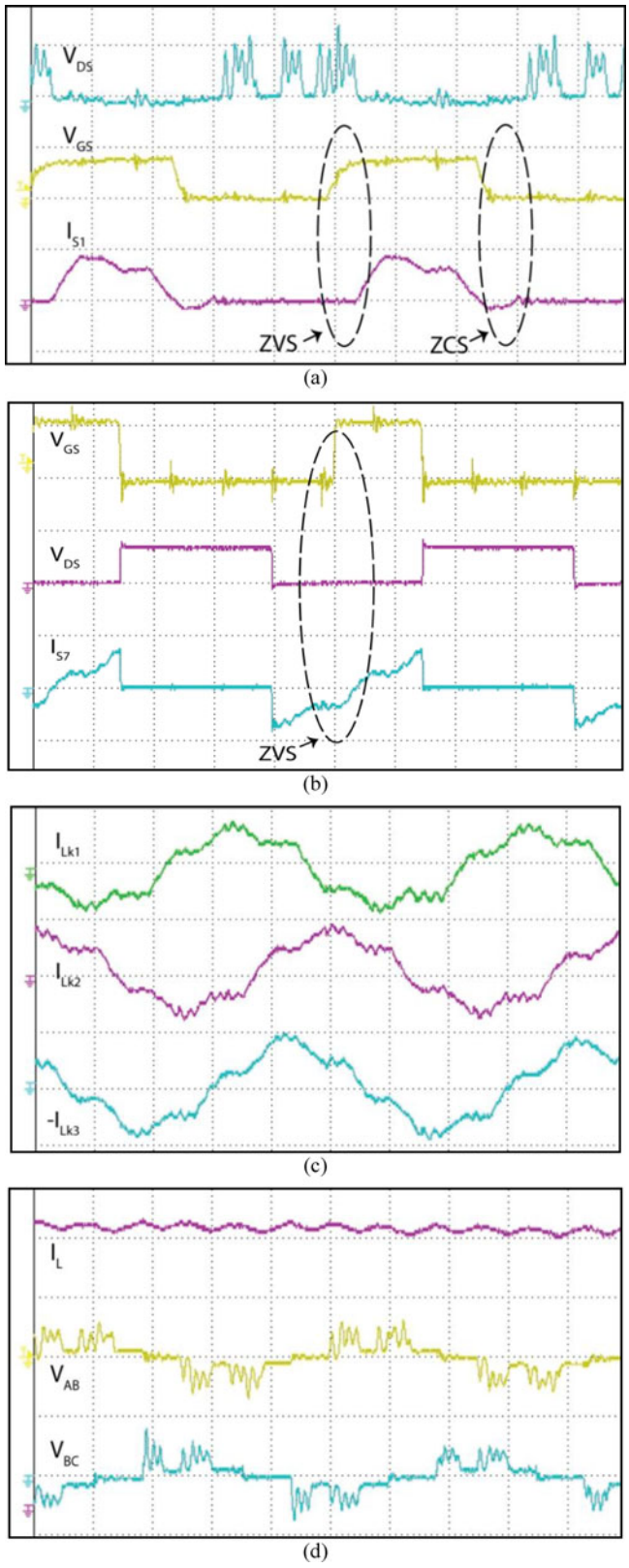

Fig. 4. Experimental waveforms: (a) the voltage(*y*-axis: 100 V/div), gate signal(*y*-axis: 20 V/div), and current(*y*-axis: 100 A/div) through switch S_1; (b) the voltage(*y*-axis: 300 V/div), gate signal(*y*-axis: 20 V/div), and current (*y*-axis: 20 A/div) through switch S_7; (c) the currents through the leakage inductors of the transformers(*y*-axis: 100 A/div); (d) the input inductor current (*y*-axis: 10 A/div), and the line voltages $V_{\rm AB}$ (*y*-axis: 100 V/div) and $V_{\rm BC}$ (*y*-axis: 100 V/div) on the primary side of transformer.

TABLE I
DETAILS OF EXPERIMENTAL PROTOTYPE

Primary devices $S_1 \sim S_6$	IRF4110, 100 V, 180 A, on-state resistance $R_{ds}(on) = 3.7$ mΩ
Secondary devices $S_7 \sim S_{12}$	IPB60R125CP, 650 V, 25 A, on-state resistance $R_{ds}(on) = 125$ mΩ
Input inductor *L*	MP-250205–2 toroidal core, 3 turns using 42 strands of SWG42
Three-phase HF transformers	3C95ETD49 ferrite core with primary turns $N_1 = 4$ turns, 42 strands of AWG 42 and secondary turns $N_2 = 20$ turns, 5 strands of AWG 42.
Output filter capacitor	450 V, 0.68 μF
Driver (both sides)	SEMIKRON SKHI 61R 6-channel

above 50%. The corresponding secondary switch is turned-on with a time difference of $T_s/3$ and turned-off simultaneously with corresponding primary switch. It means, duty cycle of secondary devices is *d*–(1/3).

Fig. 4(a) demonstrates zero-voltage zero-current switching (ZVZCS) of the primary switch S_1. Parasitic resonance should be observed resulting in ZVS of primary switches. After the gating signal V_{gs} is applied, the device S_1 starts conducting only after the device voltage V_{ds} is completely discharged to zero, resulting in ZVS turn-on.

On another note, before the gating signal V_{gs} is removed for turn-off, the current through S_1 naturally reduces to zero and the body diode takes over resulting in ZCS. The turn-on of corresponding secondary device S_7 causes the current through the switch S_1 to reduce naturally to zero and then reverse the direction (body-diode conduction). Later, the device voltage rises to forward blocking voltage naturally.

Fig. 4(b) illustrates the ZVS turn-on of the secondary switch S_7. As a result of primary modulation, the secondary-side body diode D_7 is conducting to rectify the HF ac signal, causing zero voltage to appear across switch S_7. The gating pulse V_{gs} to S_7 is applied for natural commutation of primary switch S_1, the currents through S_1 and D_7 falls simultaneously. Then, while natural commutation or ZCS turn-off happens on primary side for S_1, on secondary side S_7 takes over with ZVS.

Fig. 4(c) shows the three transformer primary currents marinating balance conditions with 120° phase-shift. Polarity change happens as a result of secondary modulation and slope depends upon the value of leakage inductance of the transformer.

Fig. 4(d) shows that ripple frequency of the input inductor current is $6f_s$. The higher ripple frequency results in selection of input inductor of smaller size. Similarly output frequency is $6\text{x}f_s$ resulting in output filer capacitor requirement of low value, low cost, and volume.

V. CONCLUSION

This letter proposes naturally clamped soft-switching snubberless modular CFD6P dc/dc converter for low-voltage high-current applications requiring high voltage gain such as UPS, energy storage, vehicles, and micro-grid applications. It is suitable for interfacing two dc voltages buses having large voltage difference. Steady-state operation, analysis, and design are presented. Experimental results are demonstrated to validate the claims. The converter attains ZVZCS of the current-fed low-voltage switches and ZVS of the high-voltage devices. Proposed modulation results in natural commutation resulting in natural clamping of the current-fed devices without additional snubber or active-clamp circuit making it snubberless. The converter design allows reduction in the size of input inductor and output capacitor with increased 6x ripple frequency.

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