Modeling and Elimination of Zero-Sequence Circulating Currents in Parallel Three-Level T-Type Grid-Connected Inverters

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***Abstract*—Unique pitfalls in parallel three-level T-type inverters (3LT^{2}Is) are potential zero-sequence circulating currents (ZSCCs) which are more complex than parallel two-level inverters and can cause current discrepancy, current waveform distortion, power losses, etc. In this paper, the ZSCC paths in the parallel 3LT^{2}Is are first presented, and an equivalent model of the ZSCCs is developed. It is seen from this model that the ZSCCs consist of conduction, switching, and hybrid components. Based on the aforementioned analysis, an original sharing neutral bus structure is proposed to eliminate the conduction ZSCCs. With regard to the switching ZSCCs composed of high-frequency and low-frequency harmonics, modified LCL filters are proposed to eliminate the former, and zero-sequence control loops are put forward to suppress the latter. Furthermore, the proposed schemes are also proven to be effective to elimination of the hybrid ZSCCs. Experimental results validate the developed models and the proposed ZSCC elimination schemes.**

***Index Terms*—Model, parallel operation, three-level T-type inverter (3LT^{2}I), zero-sequence circulating current (ZSCC).**

I. Introduction

In recent years, three-level T-type inverter (3LT^{2}I), as shown in Fig. 1, has been discussed for implementing a centralized inverter [1], [2]. Compared to the three-level neutral-point-clamped (NPC) topology [3]–[5], the T-type employs an active bidirectional switch to the dc-bus neutral point and gets along with two diodes less per phase leg. It is an alternative to more complex three-level topologies such as active neutral-point-clamped (ANPC) inverters or split-inductor inverters [6], [7]. The 3LT^{2}I basically combines the positive aspects of the two-level inverter such as low conduction losses, small part count and a simple operation principle with the advantages of the three-level inverter such as low switching losses and superior output voltage quality. However, due to the fundamental limitations of active switches, a centralized 3LT^{2}I will have a limited power rating [8]. One way to achieve a high power level is to use parallel operation. Compared with the centralized inverter, inverters in parallel can offer higher power rating, higher reliability, and lower grid-side current harmonics [9]–[11].

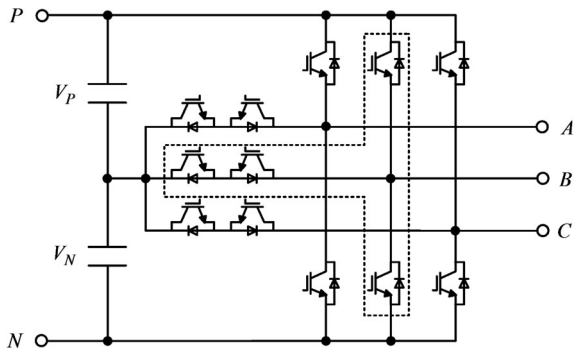

Fig. 1. Schematic of the 3LT^{2}I. A single-phase leg of the 3LT^{2}I resembles the shape of the character "T", accordingly the topology is named as T-type topology.

It should be pointed out that unique pitfalls in parallel inverters are potential zero-sequence circulating currents (ZSCCs). When individual inverters connect both ac and dc buses directly, the ZSCCs may find their paths to flow through different inverters [12]. The ZSCCs can cause current discrepancy, current waveform distortion, power losses, etc [13]–[15]. In addition, the high-frequency harmonics of the ZSCCs can introduce problems with electromagnetic interference (EMI) [16].

Current researches of the ZSCCs focus mainly on the paths, equivalent models, and elimination schemes in parallel two-level inverters. In [17] and [18], the paths and equivalent models of the ZSCCs in parallel two-level inverters are proposed, and the generating mechanism and the affecting factors of the ZSCCs are introduced; however, the path analysis and modeling approach are not applicable to parallel 3LT^{2}Is. To eliminate the ZSCCs in parallel inverters, a solution with dc or ac buses isolated is proposed to cut off the ZSCC paths [19], [20]. Nevertheless, inverters need to be isolated and the resulting system becomes bulky and costly. Interphase reactors are used to provide high impedance at high frequencies to prevent the high-frequency ZSCCs [21], [22]. However, additional reactors also increase the size and cost, and have no effect on the low-frequency ZSCCs. A modified LCL filter is proposed to connect the midpoint of the filter capacitances to the dc-bus neutral point to prevent high-frequency common mode voltage [23], [24]. However, applied to a centralized inverter, the impact of this filter on the

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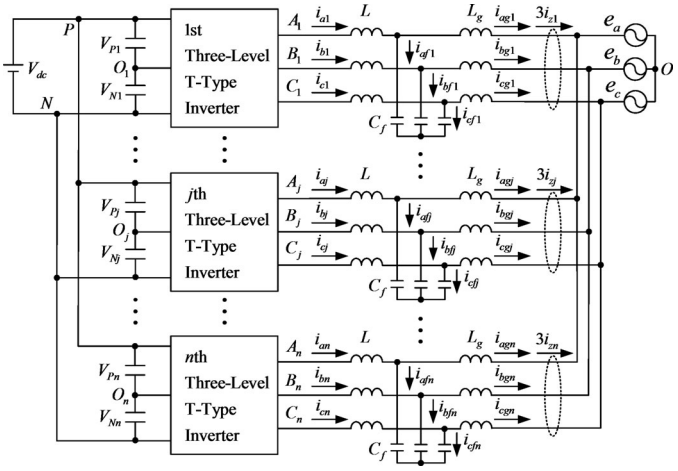

Fig. 2. Structure of the proposed parallel system.

high-frequency ZSCCs is not analyzed. Zero-sequence control loops are developed to suppress the low-frequency ZSCCs in parallel two-level inverters [25]; however, so far, application of this approach in parallel 3LT^{2}Is has not been presented in publications.

This paper proposes a parallel system where individual 3LT^{2}Is connect both ac and dc buses directly without additional passive components. The ZSCC paths in the parallel 3LT^{2}Is are first identified, and the characteristics of each path are analyzed in detail. An equivalent model of the ZSCCs is then developed. It is seen from this model that the ZSCCs in the parallel 3LT^{2}Is consist of conduction, switching, and hybrid components, which are more complex than parallel two-level inverters. Based on the aforementioned analysis, an original sharing neutral bus structure is proposed to eliminate the conduction ZSCCs. With regard to the switching ZSCCs composed of high-frequency and low-frequency harmonics, modified LCL filters are proposed to eliminate the former, and zero-sequence control loops are put forward to suppress the latter. Furthermore, the proposed schemes are also proven to be effective to elimination of the hybrid ZSCCs.

The remainder of this paper is organized as follows. In Section II, the ZSCC paths in the parallel 3LT^{2}Is are first presented. Then, an equivalent model of the ZSCCs is developed in Section III. Based on the aforementioned analysis, several schemes for eliminating the ZSCCs are proposed in Section IV. Section V shows some experimental results to validate the developed models and the proposed elimination schemes. Section VI summarizes the conclusions and contributions of this paper.

II. Analysis of the ZSCC Paths

The proposed parallel system is illustrated in Fig. 2. Each inverter is a 3LT^{2}I and n inverters with the same structures connect both ac and dc buses directly without additional passive components. Low pass LCL filters called "conventional LCL filters" in this paper are used to connect the inverter outputs with the grid. In order to simplify explanation, the parameters of the LCL filters are assumed to be identical and their equivalent series resistors (ESRs) are ignored. Damping resistors in series with the capacitances of the LCL filters, which are not identified as separate circuit elements in Fig. 2, are used to suppress resonance effects.

The ZSCCs will be generated automatically when individual inverters connect both ac and dc buses directly. The ZSCC of the jth inverter, namely, i_{zj}, can be defined as

$$i_{zj} = \frac{1}{3}\sum_{k=a,b,c} i_{kgj} = \sum_{i=1;i\neq j} i_{zji} \tag{1}$$

where i_{kgj} is the phase-k grid-side current of the jth inverter; i_{zji} is the ZSCC between the jth inverter and the ith inverter; $k \in \{a, b, c\}$; $i, j \in \{1, 2, \ldots, n\}$.

To facilitate the explanation of how the ZSCCs flow, consider a single-phase system, where single-phase legs of the jth inverter and the ith inverter are paralleled. S_{kj} ($S_{kj} \in \{1, 0, -1\}$) indicates the phase-k switching state of the jth inverter. Since a single-phase leg of the 3LT^{2}I has three switching states, according to the multiplication principle, there are $3^2 = 9$ ZSCC paths between parallel phase legs, as shown in Fig. 3.

Taking the case $S_{kj} = 1$ as an example, S_{ki} ($i \neq j$) varies among 1, 0, and -1 to form the following three ZSCC paths:

Path 1: $P-K_j-L-L_g-L_g-L-K_i-P$

Path 2: $P-K_j-L-L_g-L_g-L-K_i-O_i-P$

Path 3: $P-K_j-L-L_g-L_g-L-K_i-N-P$

where P and N are the positive and negative dc buses, respectively; K_j and O_j are the ac output and dc-bus neutral point of the jth inverter, respectively; L is the inverter-side inductance; L_g is the grid-side inductance.

For Path 1 ($S_{kj} = 1$, $S_{ki} = 1$), as shown in Fig. 3(a), the switching states of the parallel phase legs are identical and no exciting source exists. For Path 2 ($S_{kj} = 1$, $S_{ki} = 0$), as shown in Fig. 3(b), the switching state of the jth inverter differs from that of the ith inverter and the exciting source is V_{Pi} (the positive dc bus voltage of the ith inverter), thus, the ZSCC occurs. Path 3 ($S_{kj} = 1$, $S_{ki} = -1$), as shown in Fig. 3(c), is the same as Path 2, except that the exciting source of Path 3 is $V_{\rm dc}$ (the total dc-bus voltage). It is seen that the difference in switching states is a major reason for generating the ZSCCs in the parallel 3LT^{2}Is, similar to the parallel two-level inverters.

Similarly, when $S_{kj} = 0$ and $S_{kj} = -1$, the ZSCC paths are shown in Figs. 3(d)–(j), and the corresponding exciting sources are listed in Table I.

In Table I, V_{Pj} and V_{Nj} are the positive and negative dc bus voltages of the jth inverter, respectively; ΔV_j is the neutral point potential of the jth inverter, which is equal to $V_{Pj} - V_{Nj}$.

According to Fig. 3 and Table I, one can see that like Path 1, Path 9 where no exciting source exists also makes no contribution to the ZSCC. Meanwhile, for Paths 4 and 6 – 8 which are the same as Paths 2 and 3, the ZSCC is generated by the difference in switching states of the parallel inverters.

It is interesting to observe that Path 5 is a unique ZSCC path in the parallel 3LT^{2}Is, for it has two branch circuits, namely, Path $5P$ and Path $5N$, as shown in Figs. 3(e) and (f), respectively. Besides, Path 5 is formed with the exciting source (ΔV_j –

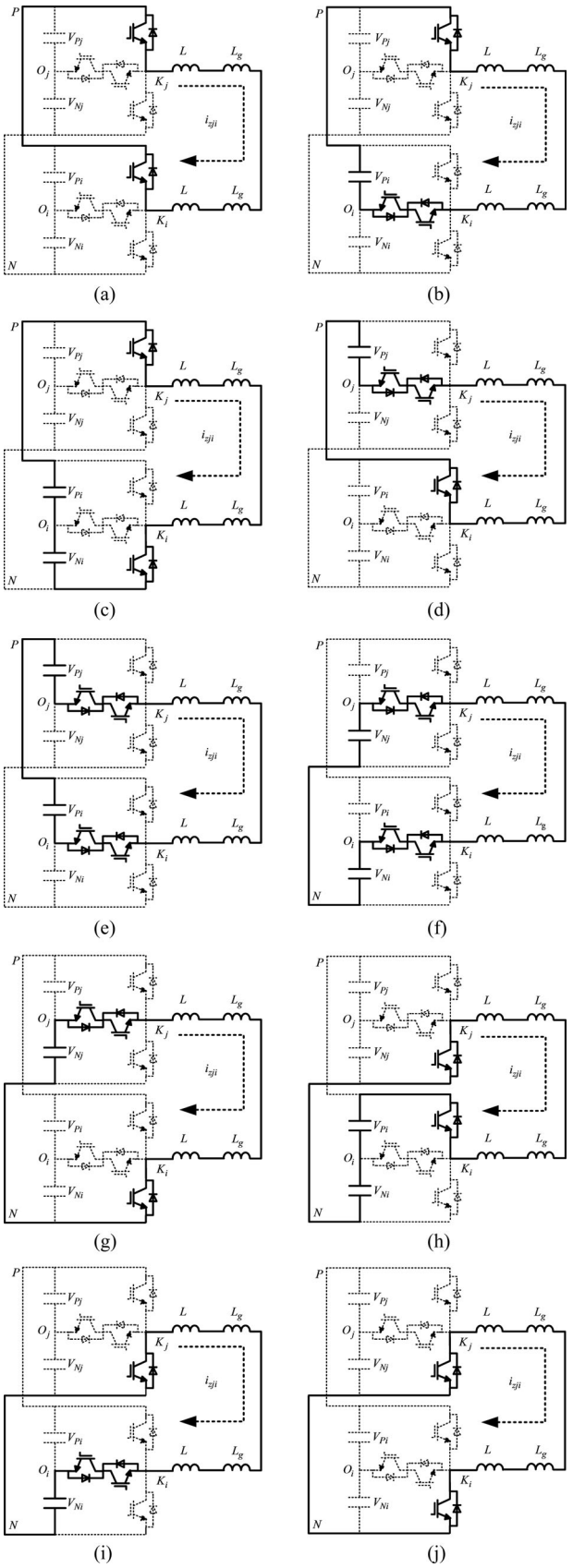

Fig. 3. ZSCC paths. (a) Path 1. (b) Path 2. (c) Path 3. (d) Path 4. (e) Path $5P$. (f) Path $5N$. (g) Path 6. (h) Path 7. (i) Path 8. (j) Path 9.

TABLE I
PATHS AND EXCITING SOURCES OF THE ZSCCS

Paths	S_{kj}	S_{ki}	Exciting Sources
1	1	1	0
2	1	0	V_{Pi}
3	1	–1	V_{dc}
4	0	1	V_{Pj}
$5P$	0	0	$(\Delta V_j - \Delta V_i)/2$
$5N$	0	0	$(\Delta V_j - \Delta V_i)/2$
6	0	–1	V_{Nj}
7	–1	1	V_{dc}
8	–1	0	V_{Ni}
9	–1	–1	0

$\Delta V_i)/2$ when S_{kj} and S_{ki} are equal to 0 at the same time, it means that the ZSCC in Path 5 is not relevant to the difference in switching states of the parallel 3LT^{2}Is.

In addition, it is seen from Fig. 3 that both the inverter-side inductance L and the grid-side inductance L_g are contained in the ZSCC paths, which influence the magnitude of the ZSCCs. Although the capacitance C_f is also a part of the LCL filter, unlike L or L_g, the ZSCCs do not flow through it.

III. MODELING OF THE ZSCCS

A. Derivation of the ZSCC Model

In the proposed system illustrated in Fig. 2, all the active switches are assumed to be ideal. Then, from Kirchhoff's voltage law (KVL), we can obtain the following equations corresponding to three-phases of the jth inverter:

$$\begin{cases} V_{Nj} + u_{aj} - L\dfrac{di_{aj}}{dt} - L_g\dfrac{di_{agj}}{dt} = e_a + u_{\mathrm{ON}} \\ V_{Nj} + u_{bj} - L\dfrac{di_{bj}}{dt} - L_g\dfrac{di_{bgj}}{dt} = e_b + u_{\mathrm{ON}} \\ V_{Nj} + u_{cj} - L\dfrac{di_{cj}}{dt} - L_g\dfrac{di_{cgj}}{dt} = e_c + u_{\mathrm{ON}} \end{cases} \tag{2}$$

where u_{kj} is the phase-k output voltage of the jth inverter between the phase-k ac output K_j and dc-bus neutral point O_j; i_{kj} and i_{kgj} are the phase-k inverter-side and grid-side currents of the jth inverter, respectively; $k \in \{a, b, c\}$; u_{ON} is the voltage between the neutral point of the grid O and the negative dc bus N.

Since no ZSCC flows through the capacitances of the filter, that is, $i_{afj} + i_{bfj} + i_{cfj} = 0$, the ZSCC of the jth inverter i_{zj} can be expressed as

$$i_{zj} = \frac{1}{3}\sum_{k=a,b,c} i_{kgj} = \frac{1}{3}\sum_{k=a,b,c} i_{kj}\ . \tag{3}$$

For a balance three-phase system, $e_a + e_b + e_c = 0$. Summing up the equations in (2), and using (3), we can obtain the

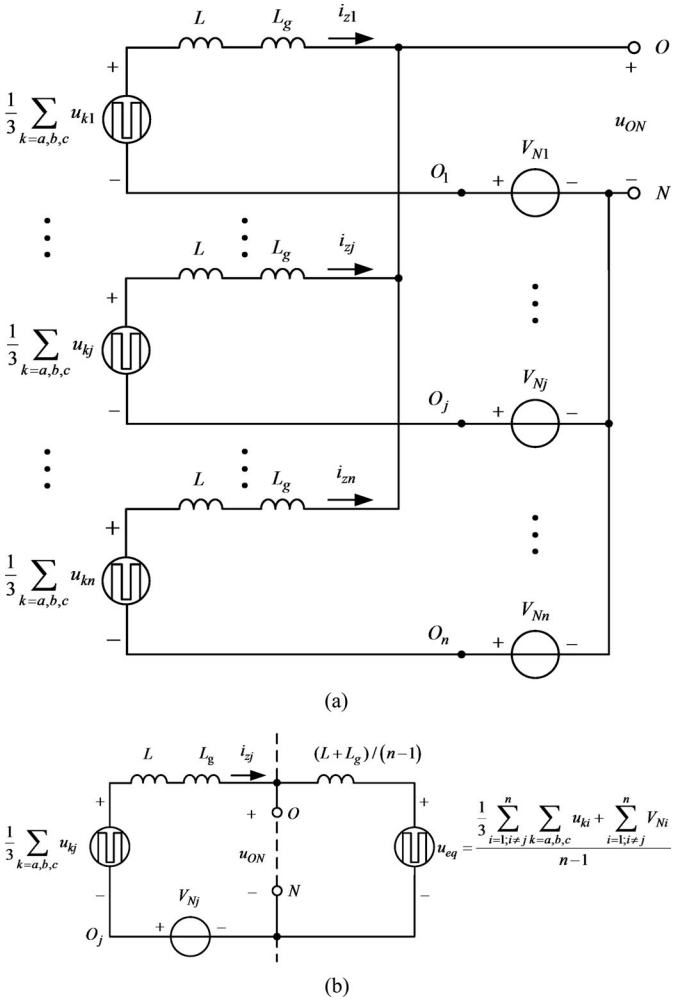

Fig. 4. Equivalent model of the ZSCCs. (a) Equivalent model. (b) Simplified model after application of Thévenin's theorem.

following equation:

$$V_{Nj}+\frac{1}{3}\sum_{k=a,b,c} u_{kj}-(L+L_g)\frac{di_{zj}}{dt}=u_{\mathrm{ON}}. \tag{4}$$

Equation (4) describes the dynamics of the ZSCC of the jth inverter with the conventional LCL filter. As $j\in\{1,2,\ldots,n\}$, according to (4), an equivalent model of the ZSCCs is developed, and depicted in Fig. 4(a). According to Thévenin's theorem, all two-terminal networks can be treated as a voltage source in series with output impedance. Therefore, the equivalent model of Fig. 4(a) can be simplified by an application of Thévenin's theorem. The network except the jth inverter is replaced in Fig. 4(b) by a voltage source u_{eq} in series with an inductance $(L+L_g)/(n-1)$.

Therefore, from Fig. 4(b), the ZSCC of the jth inverter can be expressed in complex frequency domain as follows:

$$\begin{aligned} i_{zj}(s) &= \frac{V_{Nj}(s)+\frac{1}{3}\sum_{k=a,b,c} u_{kj}(s)-u_{\mathrm{eq}}(s)}{(L+L_g)s+(L+L_g)s/(n-1)} \\ &= H(s)\cdot u_{zj}(s) \end{aligned} \tag{5}$$

where u_{zj} is the exciting source of i_{zj}; $H(s)$ is the transfer function from u_{zj} to i_{zj}. $u_{zj}(s)$ and $H(s)$ are expressed as

$$\begin{cases} u_{zj}(s)=\sum_{i=1;i\neq j}^{n}\left(V_{Nj}(s)-V_{Ni}(s)\right) \\ \qquad +\frac{1}{3}\sum_{i=1;i\neq j}^{n}\sum_{k=a,b,c}\left(u_{kj}(s)-u_{ki}(s)\right) \\ H(s)=\frac{1}{n(L+L_g)s} \end{cases}. \tag{6}$$

From the resulting ZSCC model of (5) and (6), one can see that the transfer function $H(s)$ is of the first order, and both L and L_g influence the magnitude of the ZSCC. Nevertheless, as a part of the LCL filter, C_f is not contained in $H(s)$ of (6), indicating that C_f has no effect on the ZSCC. This conclusion is consistent with the aforementioned analysis in Section II.

B. Classification of the ZSCCs

Based on the path analysis in Section II, one can get that the ZSCCs in the parallel 3LT^{2}Is are more complex than parallel two-level inverters. In order to obtain the components of the ZSCCs in the parallel 3LT^{2}Is, three-phase output voltages of the jth inverter, u_{aj}, u_{bj}, and u_{cj}, are given as functions of their switching states as follows:

$$\begin{cases} u_{aj}=\frac{V_{\mathrm{dc}}}{2}\cdot S_{aj}+\frac{\Delta V_j}{2}\cdot S_{aj}^2 \\ u_{bj}=\frac{V_{\mathrm{dc}}}{2}\cdot S_{bj}+\frac{\Delta V_j}{2}\cdot S_{bj}^2 \\ u_{cj}=\frac{V_{\mathrm{dc}}}{2}\cdot S_{cj}+\frac{\Delta V_j}{2}\cdot S_{cj}^2 \end{cases}. \tag{7}$$

Summing up the equations of (7), one can obtain the following equation:

$$\sum_{k=a,b,c} u_{kj}=\frac{V_{\mathrm{dc}}}{2}\sum_{k=a,b,c} S_{kj}+\frac{\Delta V_j}{2}\sum_{k=a,b,c} S_{Kj}^2. \tag{8}$$

Meanwhile, for the jth 3LT^{2}I, we have $V_{Pj}+V_{Nj}=V_{\mathrm{dc}}$ and $V_{Pj}-V_{Nj}=\Delta V_j$. Thus, V_{Nj} can be expressed as

$$V_{Nj}=\frac{1}{2}\left(V_{\mathrm{dc}}-\Delta V_j\right). \tag{9}$$

As $j\in\{1,2,\ldots,n\}$, according to (6), (8), and (9), we can get the expression of the exciting source u_{zj} as follows:

$$\begin{aligned} u_{zj}=&-\frac{1}{2}\sum_{i=1;i\neq j}^{n}\left(\Delta V_j-\Delta V_i\right) \\ &+\frac{V_{dc}}{6}\sum_{i=1;i\neq j}^{n}\sum_{k=a,b,c}\left(S_{kj}-S_{ki}\right) \\ &+\frac{1}{6}\sum_{i=1;i\neq j}^{n}\sum_{k=a,b,c}\left(\Delta V_j S_{kj}^2-\Delta V_i S_{ki}^2\right). \end{aligned} \tag{10}$$

Equation (10) shows that the exciting source u_{zj} contains three components, as follows:

1) The conduction source, namely, u_{zcj}, is expressed as (11). It is observed that u_{zcj} is not relevant to the switching states but dependent on the difference of the neutral point potentials.

The neutral point potential is dependent on the modulation index and power factor. If parallel inverters in the grid-connected mode have the same modulation indexes and power factors, their neutral point potentials are almost identical. It means that u_{zcj} is close to zero, and the corresponding conduction ZSCC, namely, i_{zcj}, can be hardly generated. However, if a portion of inverters are switched to the grid-connected mode from the standby mode, their modulation indexes and power factors will change drastically, which will cause the conduction ZSCC at the switching instant

$$u_{zcj} = -\frac{1}{2}\sum_{i=1;i\neq j}^{n}(\Delta V_j - \Delta V_i). \tag{11}$$

2) The switching source, namely, u_{zsj}, is expressed as (12). It is observed that u_{zsj} is generated by the difference in switching states of the parallel inverters. The corresponding switching ZSCC is represented by i_{zsj}. The switching ZSCC can be separated into high-frequency and low-frequency harmonics

$$u_{zsj} = \frac{V_{\rm dc}}{6}\sum_{i=1;i\neq j}^{n}\sum_{k=a,b,c}(S_{kj} - S_{ki}). \tag{12}$$

3) The hybrid source, namely, u_{zhj}, is expressed as (13). It is observed that u_{zhj} is influenced by both the switching states and neutral point potentials of the parallel inverters. If the neutral points are all clamped at half of the total dc bus voltage, that is, $\Delta V_1 = \Delta V_2 = \cdots = \Delta V_n = 0$, no hybrid ZSCC will be generated. Actually when switching strategies are applied, the neutral point potentials deviate from the center potential of the dc bus voltage. Thus, the hybrid ZSCC, i_{zhj}, comes into existence. The hybrid ZSCC can also be separated into high-frequency and low-frequency harmonics

$$u_{zhj} = \frac{1}{6}\sum_{i=1;i\neq j}^{n}\sum_{k=a,b,c}\left(\Delta V_j S_{kj}^2 - \Delta V_i S_{ki}^2\right). \tag{13}$$

From (11)–(13), we can see that consisting of conduction, switching, and hybrid components, the ZSCCs in the parallel $3LT^2$Is are more complex than parallel two-level inverters.

IV. Elimination of the ZSCCs

A. Elimination of the Conduction ZSCCs

The conduction ZSCCs are particular circulating currents in the parallel $3LT^2$Is, which have two remarkable characteristics. On one hand, the conduction ZSCCs have no correlation with the switching states of the parallel inverters. On the other hand, the conduction sources relate to the difference of the neutral point potentials. From Fig. 3 and Table I, one can see that only Paths $5P$ in Fig. 3(e) and $5N$ in Fig. 3(f) meet the aforementioned characteristics. Thus, the conduction ZSCCs only flow through paths $5P$ and $5N$.

If a portion of inverters are switched to the grid-connected mode from the standby mode, the conduction ZSCCs will occur, which will result in the grid-side current spikes, and may damage the active switches and reduce the reliability of the system.

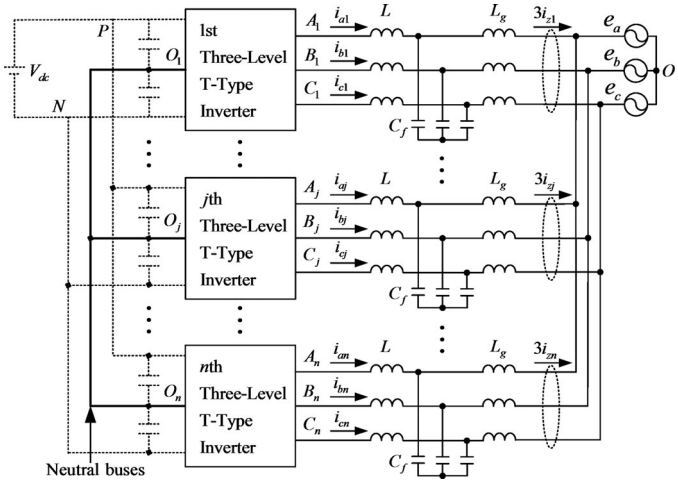

Fig. 5. Proposed sharing neutral bus structure. The dc-bus neutral points of all inverters, from O_1 to O_n, are connected directly.

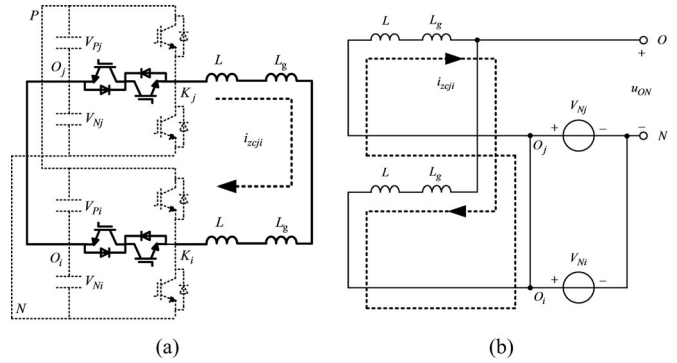

Fig. 6. Benefits of the proposed parallel structure. (a) Path 5 with the proposed structure. (b) The conduction source with the proposed structure.

In order to eliminate the conduction ZSCCs, an original sharing neutral bus structure as shown in Fig. 5, is proposed, wherein, the dc-bus neutral points of all inverters, from O_1 to O_n, are connected directly. The main benefits of the proposed structure are as follows:

1) Path 5 is changed. The conduction ZSCC between the jth inverter and the ith inverter, namely, i_{zcji}, flows not through the positive or negative dc buses, but through the neutral buses in the new Path 5 in Fig. 6(a).
2) As all the dc-bus neutral points are connected directly, V_{Nj} is clamped to V_{Ni}, as shown in Fig. 6(b). Then, ΔV_j is identical to ΔV_i and no conduction source exists in the path of i_{zcji}.

Therefore, i_{zcji} is removed by sharing the neutral buses. As the conduction ZSCC i_{zcj} is the sum of $i_{zcj1}, \ldots, i_{zcji}$ $(i \neq j), \ldots,$ and i_{zcjn}, based on the analysis aforementioned, i_{zcj} becomes zero. As a result, the elimination of the conduction ZSCCs can be achieved by applying the proposed parallel structure.

B. Elimination of the High-Frequency Switching ZSCCs

As is known, through interleaving the switching cycles of parallel inverters by an appropriate angle (it is usually π for

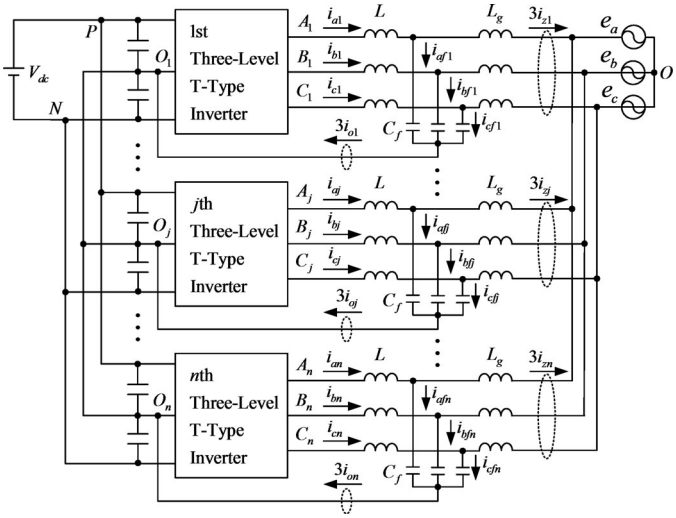

Fig. 7. Proposed system with modified LCL filters. The midpoints of the filter capacitances are connected to the dc-bus neutral points directly.

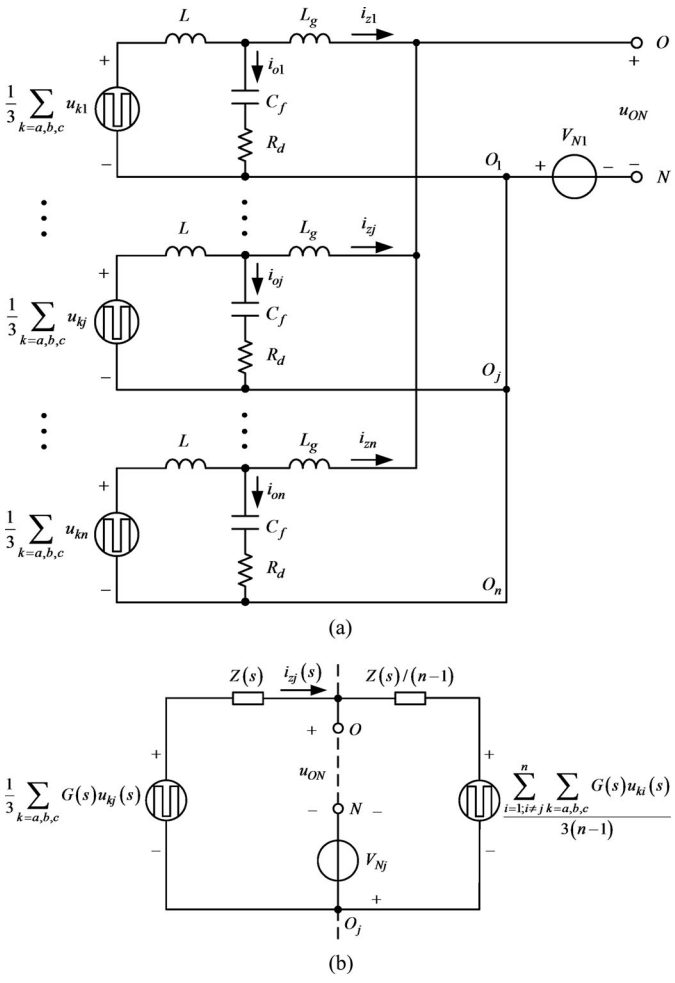

Fig. 8. Equivalent model of the ZSCCs with the modified LCL filters. (a) Equivalent model. (b) Simplified model after application of Thévenin's theorem.

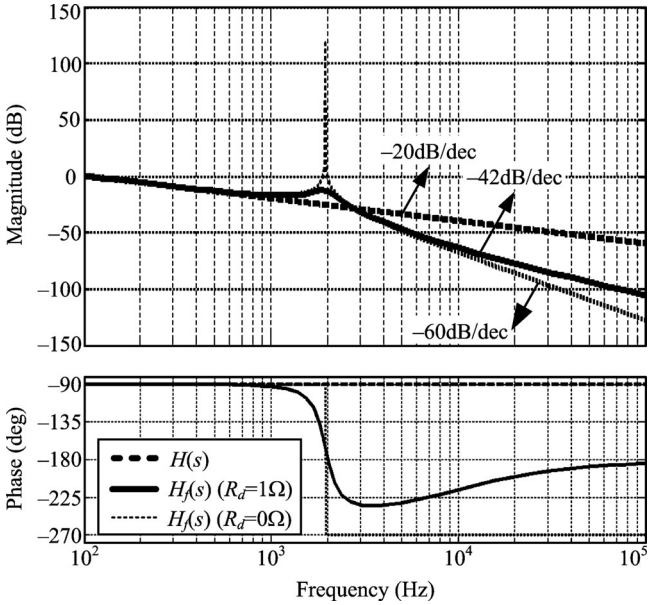

Fig. 9. Bode diagram of both $H_f(s)$ and $H(s)$.

TABLE II
PARAMETERS OF THE SIMULATION MODEL

Parameters	Values	Parameters	Values
L	1mH	L_g	0.5mH
C_f	30μF	R_d	1Ω
f_s	10kHz	ω	100π
V_{dc}	600V	n	1
Grid Voltage		e_a=311cosωt V	
		e_b=311cos(ωt-2π/3) V	
		e_c=311cos(ωt+2π/3) V	

two parallel inverters), some harmonics of the inverter outputs can be reduced significantly [26]. However, interleaving generally worsens the circulating current problem by introducing additional high-frequency switching ZSCCs. Because of the finite bandwidth as well as the limited switching speed of active switches, the high-frequency switching ZSCCs cannot be eliminated by existing control schemes [25]. Interphase reactors are used to provide high impedance at high frequencies to prevent high-frequency ZSCCs [21], [22]. But additional reactors increase the size and cost of the system.

In order to eliminate the high-frequency switching ZSCCs, modified LCL filters without additional reactors are proposed in this paper, as shown in Fig. 7, where the midpoints of the filter capacitances are connected to the dc-bus neutral points. Thus, for the jth inverter, a common mode current, namely, i_{oj}, is generated and flows through the following path.

Path for i_{oj}: $O_j - K_j - L - C_f - R_d - O_j$.

Note that i_{oj} flows through the same inverter and cannot be considered as the ZSCC. Then, from KVL, the equations corresponding to the three-phase common mode circuits of the

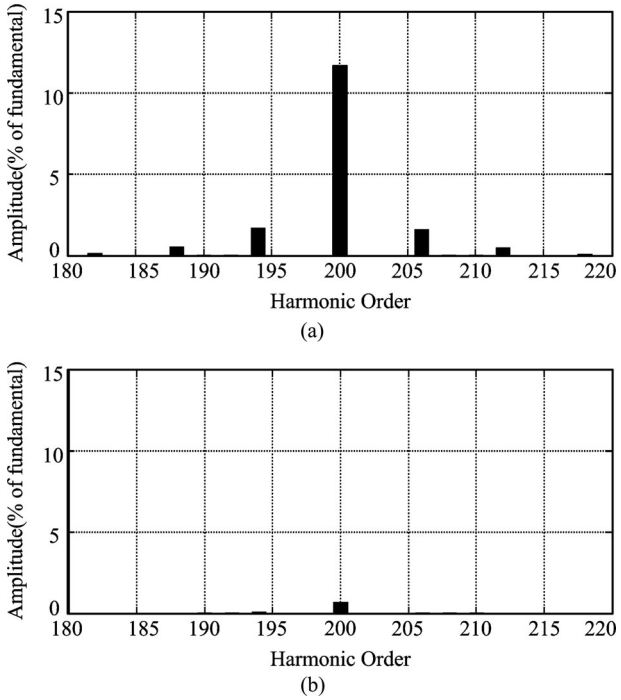

Fig. 10. Simulated results of the grid-side current spectra around the switching frequency. (a) The spectra with the conventional LCL filter. (b) The spectra with the modified LCL filter.

jth inverter are derived as (14)

$$\begin{cases} u_{aj} - L\dfrac{di_{aj}}{dt} - \dfrac{\int i_{afj}dt}{C_f} - R_d i_{afj} = 0 \\ u_{bj} - L\dfrac{di_{bj}}{dt} - \dfrac{\int i_{bfj}dt}{C_f} - R_d i_{bfj} = 0 \\ u_{cj} - L\dfrac{di_{cj}}{dt} - \dfrac{\int i_{cfj}dt}{C_f} - R_d i_{cfj} = 0 \end{cases}. \tag{14}$$

Because of the modified LCL filter, $i_{afj} + i_{bfj} + i_{cfj} = 3i_{oj}$, the ZSCC of the jth inverter is redefined as

$$i_{zj} = \frac{1}{3}\sum_{k=a,b,c} i_{kgj} = \frac{1}{3}\sum_{k=a,b,c} i_{kj} - i_{oj}. \tag{15}$$

Summing up the equations in (14), and using (15), we can obtain the following equation

$$\frac{1}{3}\sum_{k=a,b,c} u_{kj} - L\frac{d\left(i_{oj}+i_{zj}\right)}{dt} - \frac{\int i_{oj}dt}{C_f} - R_d i_{oj} = 0. \tag{16}$$

Meanwhile, because i_{zj} is redefined, (3) is not applicable to the jth inverter with the modified LCL filter. Summing up the equations in (2), and using the redefined expression of (15), we can obtain the following equation

$$V_{Nj} + \frac{1}{3}\sum_{k=a,b,c} u_{kj} - L\frac{d\left(i_{zj}+i_{oj}\right)}{dt} - L_g\frac{di_{zj}}{dt} = u_{\mathrm{ON}}. \tag{17}$$

Equations (16) and (17) describe the dynamics of the ZSCC of the jth inverter with the modified LCL filter. As $j \in \{1, 2, \ldots, n\}$, an equivalent model of the ZSCCs with the modified

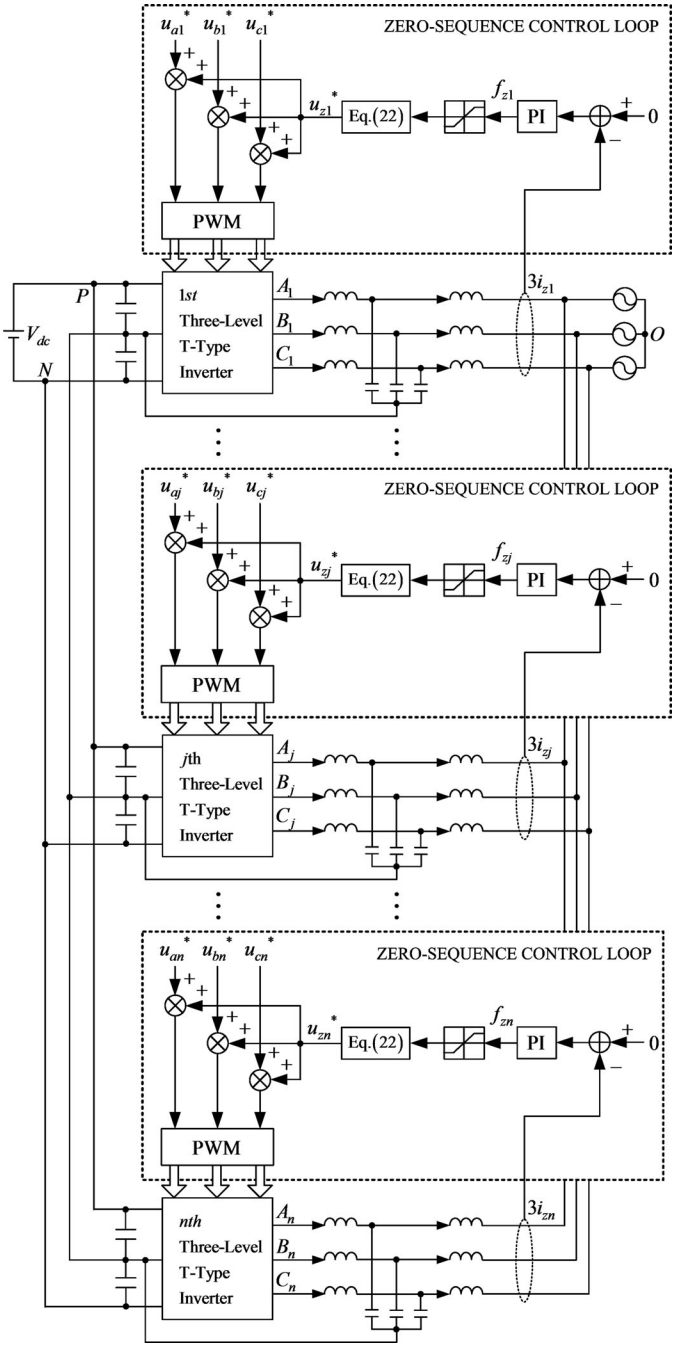

Fig. 11. Zero-sequence control loops for low-frequency switching ZSCCs.

LCL filters is developed, and depicted in Fig. 8(a). According to Thévenin's theorem, the equivalent model of Fig. 8(a) can be represented by the simplified model in Fig. 8(b), where $G(s)$ is the coefficient of the equivalent voltage source and Z is the equivalent impedance, as shown in (18)

$$\begin{cases} G(s) = \dfrac{R_d C_f s + 1}{LC_f s^2 + R_d C_f s + 1} \\ Z(s) = \dfrac{LL_g C_f s^3 + (L + L_g) R_d C_f s^2 + (L + L_g) s}{LC_f s^2 + R_d C_f s + 1} \end{cases}. \tag{18}$$

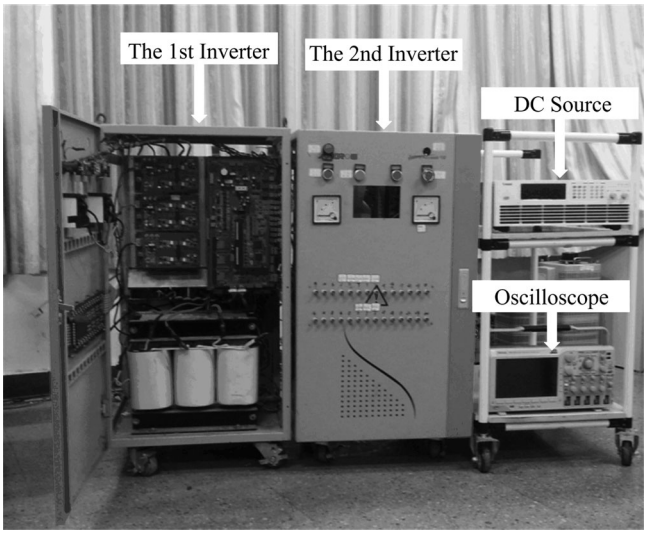

Fig. 12. Photograph of the experimental prototype.

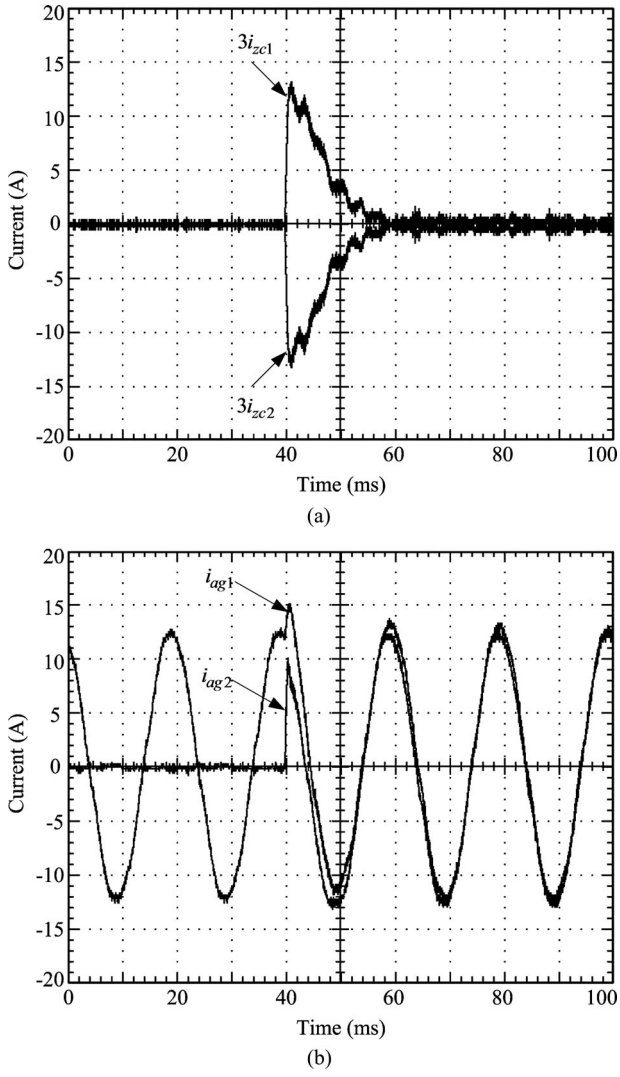

Fig. 13. Experimental waveforms without sharing neutral buses (the second inverter is switched to the grid-connected mode at the fortieth millisecond). (a) The conduction ZSCCs. (b) The grid-side currents.

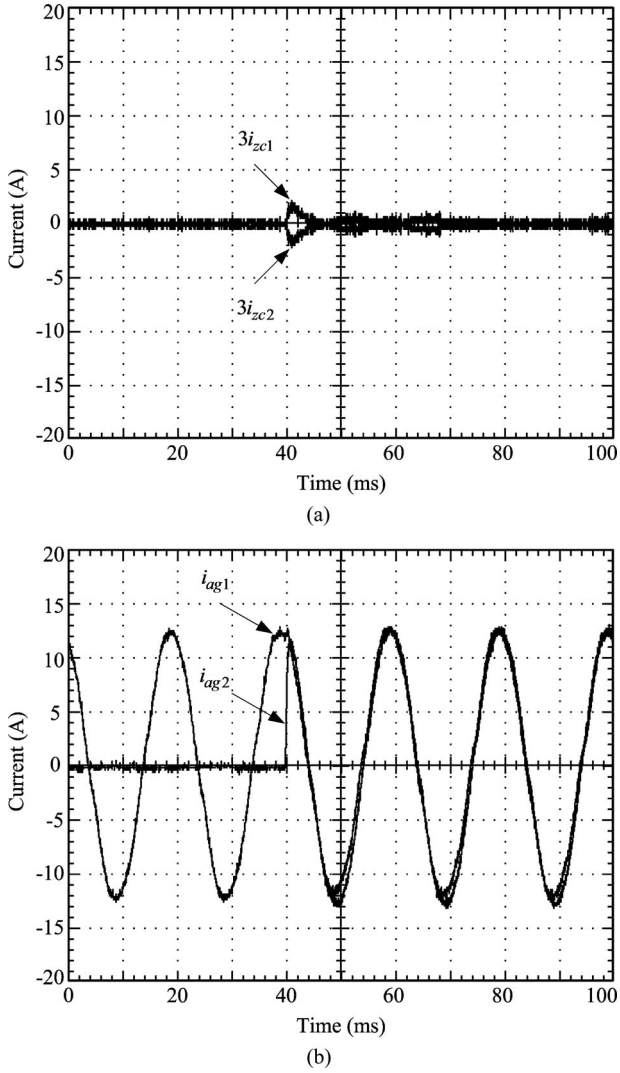

Fig. 14. Experimental waveforms with sharing neutral buses (the second inverter is switched to the grid-connected mode at the fortieth millisecond). (a) The conduction ZSCCs. (b) The grid-side currents.

Therefore, from Fig. 8(b), we can get the ZSCC expression of the jth inverter with the modified LCL filter in complex frequency domain as follows:

$$\begin{aligned} i_{zj}(s) &= \frac{G(s)\left(\sum_{k=a,b,c} u_{kj}(s) - \frac{\sum_{i=1;i\neq j}^{n}\sum_{k=a,b,c} u_{ki}(s)}{n-1}\right)}{3\left(Z(s)+Z(s)/(n-1)\right)} \\ &= H_f(s)\cdot u_{zj}(s) \end{aligned} \tag{19}$$

where $H_f(s)$ is the transfer function from u_{zj} to i_{zj} with the modified LCL filter, as shown in (20)

$$H_f(s) = \frac{R_d C_f s + 1}{n\left(LL_g C_f s^3 + (L+L_g) R_d C_f s^2 + (L+L_g) s\right)}. \tag{20}$$

Comparing (20) with (6), we can see that $H_f(s)$ differs from $H(s)$ in that the former is of the third order, whereas the latter is

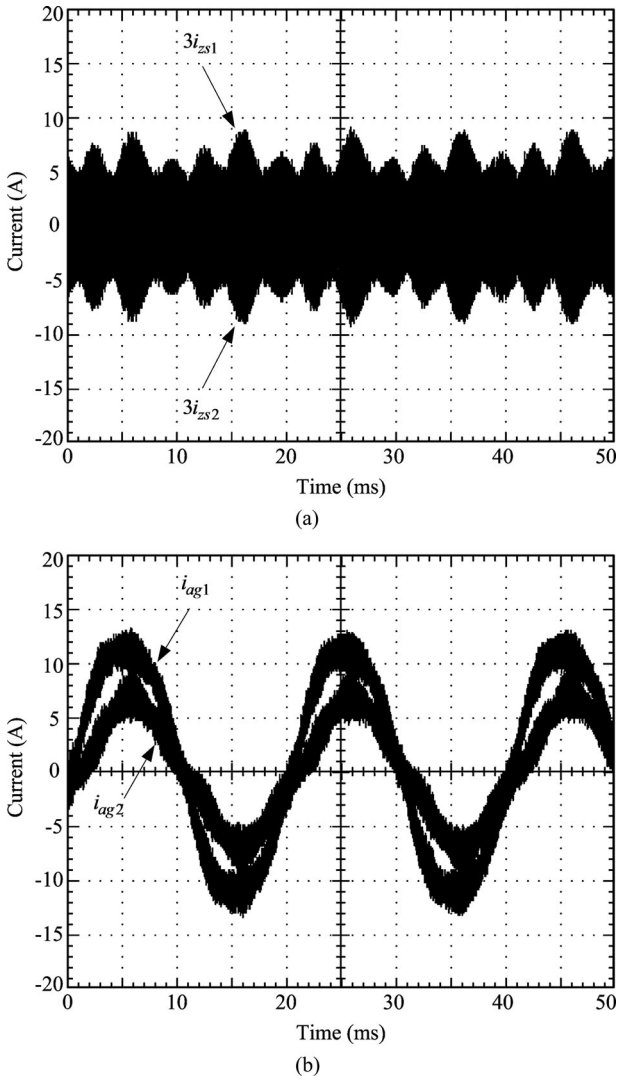

Fig. 15. Experimental waveforms with the conventional LCL filters (the first inverter is at full-load whereas the second inverter is at half-load with an interleaving angle of π). (a) The switching ZSCCs. (b) The grid-side currents.

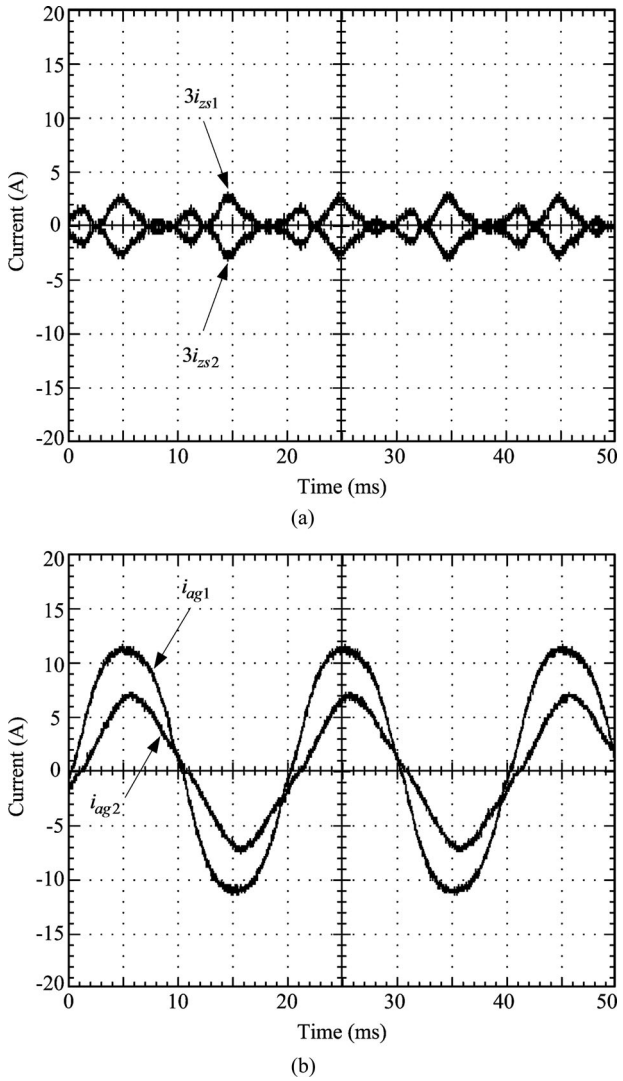

Fig. 16. Experimental waveforms with the modified LCL filters (the first inverter is at full-load whereas the second inverter is at half-load with an interleaving angle of π). (a) The switching ZSCCs. (b) The grid-side currents.

of the first order. Fig. 9 shows the Bode diagram of both $H_f(s)$ and $H(s)$ while the corresponding parameters designed based on the criteria given in [27] are listed in Table II. Note that n is assumed to be equal to 1, as its value has no effect on the plot slopes. It can be seen from Fig. 9 that, within the low-frequency range, the modified LCL filter has almost the same frequency-response characteristic as the conventional LCL filter. However, within the high-frequency range, the modified LCL filter has better attenuating effect on the high-frequency harmonics of the ZSCC.

Further proof comes from the simulated results of the grid-side current spectra shown in Fig. 10 on the condition that two 3LT^{2}Is with the parameters listed in Table II are in parallel and the neutral points are all clamped at half of the dc-bus voltage. Thus, $\Delta V_1 = \Delta V_2 = \cdots = \Delta V_n = 0$, and no hybrid ZSCC will be generated. It can be observed that the elimination of the high-frequency switching ZSCCs can be achieved by applying the modified LCL filters.

In addition, the resonance of $H_f(s)$ is attenuated by the damping resistor at the cost of a decay of the high-frequency attenuating effect from -60 to -42 dB/dec.

C. Elimination of the Low-Frequency Switching ZSCCs

Since the high-frequency harmonics are eliminated by the modified LCL filters, the low-frequency harmonics turn to be the main elements of the switching ZSCCs. Zero-sequence control loops are developed to suppress the low-frequency ZSCCs in the parallel two-level inverters [25]; however, so far, application of this approach in the parallel 3LT^{2}Is has not been mentioned to our knowledge in published reports.

u_{kj}^* is defined as the phase-k sinusoidal modulation function of the jth inverter; u_{zj}^* is defined as the zero-sequence modulation function of the jth inverter. Ignoring the high-frequency harmonics of the switching source shown in (12), and using u_{kj}^*

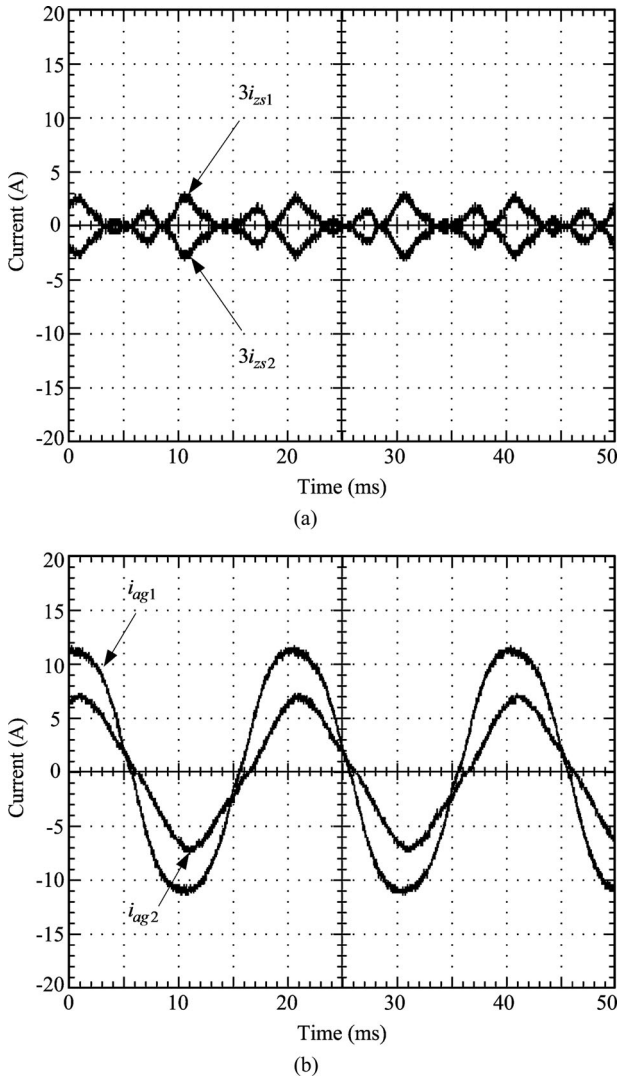

Fig. 17. Experimental waveforms without the zero-sequence control loops (the first inverter is at full-load and the second inverter is at half-load). (a) The switching ZSCCs. (b) The grid-side currents.

and u^*_{zj}, we can obtain the following equation:

$$u_{zsj} = \frac{V_{\rm dc}}{2} \sum_{i=1;i\neq j}^{n} \left(u^*_{zj} - u^*_{zi}\right). \tag{21}$$

According to the unified voltage modulation technique, the zero-sequence modulation function of the jth inverter u^*_{zj} can be regulated by a distribution factor as follows [28], [29]

$$u^*_{zj} = 2f_{zj} - 1 - f_{zj}u^*_{j\max} + (f_{zj} - 1)\, u^*_{j\min} \tag{22}$$

where f_{zj} is the distribution factor of u^*_{zj}; $0 \le f_{zj} \le 1$; $u^*_{j\max}$ and $u^*_{j\min}$ represent the maximum and minimum values among u^*_{aj}, u^*_{bj}, and u^*_{cj}.

By letting $u^*_{1\max} = u^*_{2\max} = \cdots = u^*_{n\max}$ and $u^*_{1\min} = u^*_{2\min} = \cdots = u^*_{n\min}$, we can obtain from (21) and (22) the following result:

$$u_{zsj} = \frac{V_{\rm dc}}{2}\left(2 - u^*_{j\max} + u^*_{j\min}\right) \sum_{i=1;i\neq j}^{n} (f_{zj} - f_{zi}). \tag{23}$$

It is seen from (23) that the low-frequency switching ZSCC is relevant to the variable $f_{zj} - f_{zi}$ (difference of the distribution factors). As is known, the distribution factor can vary without affecting the control objectives, such as the inverter-side currents and the dc bus voltage. This indicates that the low-frequency switching ZSCCs can be controlled by regulating the distribution factors. It should be pointed out that the neutral point potential of the 3LT^{2}I varies from the center potential of the dc-bus voltage. Several strategies have been presented to control the neutral point potential also through regulating the distribution factor [28]–[30]. f_{npj} is defined as the distribution factor of the neutral point potential control for the jth inverter. Thus, f_{npj} affects the limit of f_{zj}, and the sum of f_{npj} and f_{zj} cannot exceed 1. As a result, the distribution factor in (22) should be limited within the range of

$$0 \le f_{zj} \le 1 - f_{npj}. \tag{24}$$

Accordingly, zero-sequence control loops based on the distribution factors are shown in Fig. 11. For the jth inverter with conventional LCL filter, three inverter-side current sensors are enough because the sum of three inverter-side currents always represents the ZSCC. For the proposed modified LCL filter, a grid-side ZSCC sensor is needed. Simple PI controller is adopted in the proposed control loop, and the output of the controller is limited within the range of (24) and finally used in (22) to obtain the zero-sequence modulation function. The control bandwidth of the zero-sequence control loop can be designed to be high and a strong loop suppressing the ZSCC can be achieved. Note that each zero-sequence control loop is implemented within individual inverter, and does not need any additional interconnected circuitry, it allows modular design.

D. Elimination of the Hybrid ZSCCs

The hybrid ZSCCs are also unique circulating currents in the parallel 3LT^{2}Is, which are influenced by both the switching states and neutral point potentials of the parallel inverters. The hybrid ZSCCs can also be separated into low-frequency and high-frequency harmonics.

Equation (19) describes the ZSCC expression of the jth inverter with the modified LCL filter in complex frequency domain. According to the superposition theorem, we have $i_{zsj}(s) = H_f(s)u_{zsj}(s)$ and $i_{zhj}(s) = H_f(s)u_{zhj}(s)$, it means that the hybrid ZSCC has the same transfer function as the switching ZSCC. As the result, based on the conclusion in Section II-B, the elimination of the high-frequency hybrid ZSCC can also be achieved by applying the modified LCL filter.

As all the neutral points are connected directly and $\Delta V_1 = \Delta V_2 = \cdots = \Delta V_n$, ignoring the high-frequency harmonics of the hybrid source, then, the hybrid source u_{zhj} is transformed, as shown in (25). It is seen that u_{zhj} is proportional to the switching source u_{zsj}. If the zero-sequence control loops are implemented, the low-frequency switching ZSCCs will be controlled to zero, according to (25), the low-frequency hybrid ZSCCs will be

eliminated automatically

$$u_{zhj} = \frac{\Delta V_j}{V_{dc}} \sum_{i=1;i\neq j}^{n} \sum_{k=a,b,c} \left(u_{kj}^* + u_{ki}^*\right) \cdot u_{zsj}. \qquad (25)$$

V. Experimental Results

In order to validate the developed models and the proposed elimination schemes, experiments have been carried out on a prototype system, as shown in Fig. 12. The prototype is composed of two-parallel 3LT^{2}Is and the power rating of each inverter is 10 kW. The dc source is supplied by a photovoltaic simulator (Chroma 62150H-1000S) in the experiments. The control circuit is implemented on a DSP chip TMS320F28335. The parameters of the prototype are also shown in Table II.

A. Experiments for Elimination of the Conduction ZSCCs

Synchronized control is adopted to ensure the switching states of the parallel inverters are identical, thus, according to (12) and (13), no switching ZSCCs or hybrid ZSCCs exist in the experiments of Section V-A.

Fig. 13 shows the conduction ZSCCs and the grid-side currents without sharing neutral buses when the second inverter is switched to the grid from the standby mode at the fortieth millisecond. The conduction ZSCCs in Fig. 13(a) reach around 13 A at the switching instant, which cause the grid-side currents spikes, as shown in Fig. 13(b).

Fig. 14 shows experimental waveforms with sharing neutral buses with the same condition of Fig. 13. The conduction ZSCCs shown in Fig. 14(a) are reduced to less than 5 A at the switching instant and the grid-side currents spikes in Fig. 14(b) are no longer significant.

It is proven that the conduction ZSCCs are eliminated effectively by sharing neutral buses.

B. Experiments for Elimination of the High-Frequency Switching ZSCCs

The neutral buses are shared and the neutral points are both clamped at half of the total dc-bus voltage, so no conduction ZSCCs or hybrid ZSCCs are generated in the parallel inverters. Furthermore, the synchronized control is no longer adopted in the following experiments.

Fig. 15 shows the switching ZSCCs and the grid-side currents with the conventional LCL filters, when the first inverter is at full-load and the second inverter is at half-load with an interleaving angle of π. It is seen that an abundance of high-frequency harmonics exist in the switching ZSCCs in Fig. 15(a) and the grid-side currents in Fig. 15(b), which cause serious problems with EMI.

Fig. 16 shows experimental waveforms with the modified LCL filters with the same condition of Fig. 15. The high-frequency harmonics existing in the switching ZSCCs and the grid-side currents are almost gone, as shown in Figs. 16(a) and (b), respectively.

It is proven that the high-frequency switching ZSCCs are eliminated effectively by the modified LCL filters.

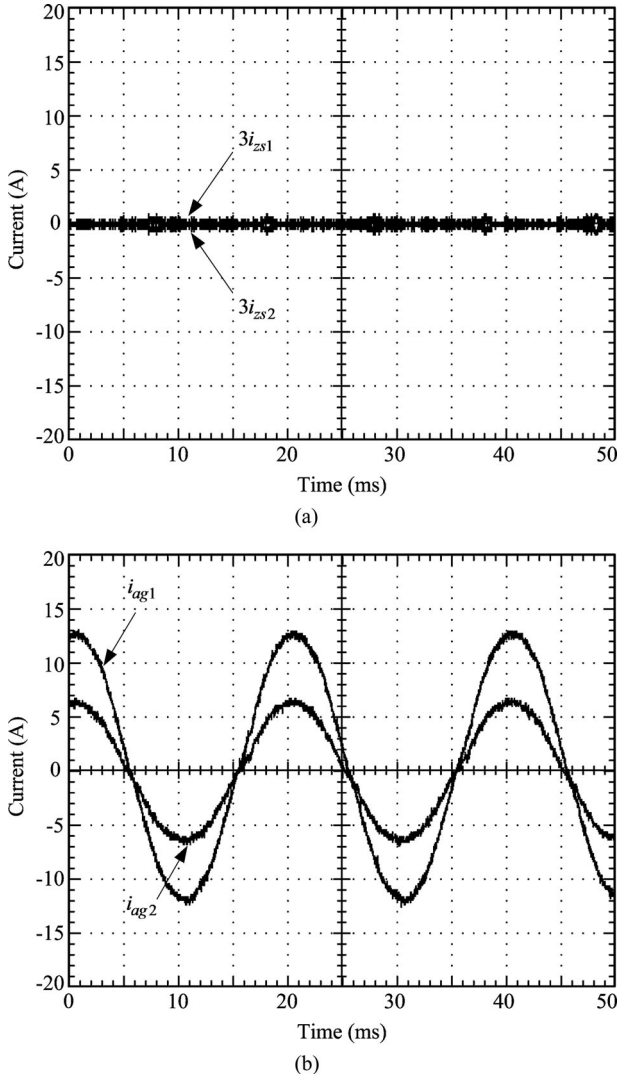

Fig. 18. Experimental waveforms with the zero-sequence control loops (the first inverter is at full-load and the second inverter is at half-load). (a) The switching ZSCCs. (b) The grid-side currents.

C. Experiments for Elimination of the Low-Frequency Switching ZSCCs

The experimental environment in Section V-C is the same as Section V-B. Meanwhile, the modified LCL filters are applied in the following experiments.

Fig. 17 shows the switching ZSCCs and the grid-side currents without the zero-sequence control loops. It can be seen from Fig. 17(a) that the low-frequency harmonics become the main elements of the switching ZSCCs, as the high-frequency harmonics are eliminated by the modified LCL filters. The low-frequency switching ZSCCs distort the grid-side currents waveforms, as shown in Fig. 17(b).

Fig. 18 shows the switching ZSCCs and the grid-side currents with the zero-sequence control loops in the same condition of Fig. 17. It can be seen that the low-frequency switching ZSCCs are almost gone and the grid-side currents performance is improved greatly.

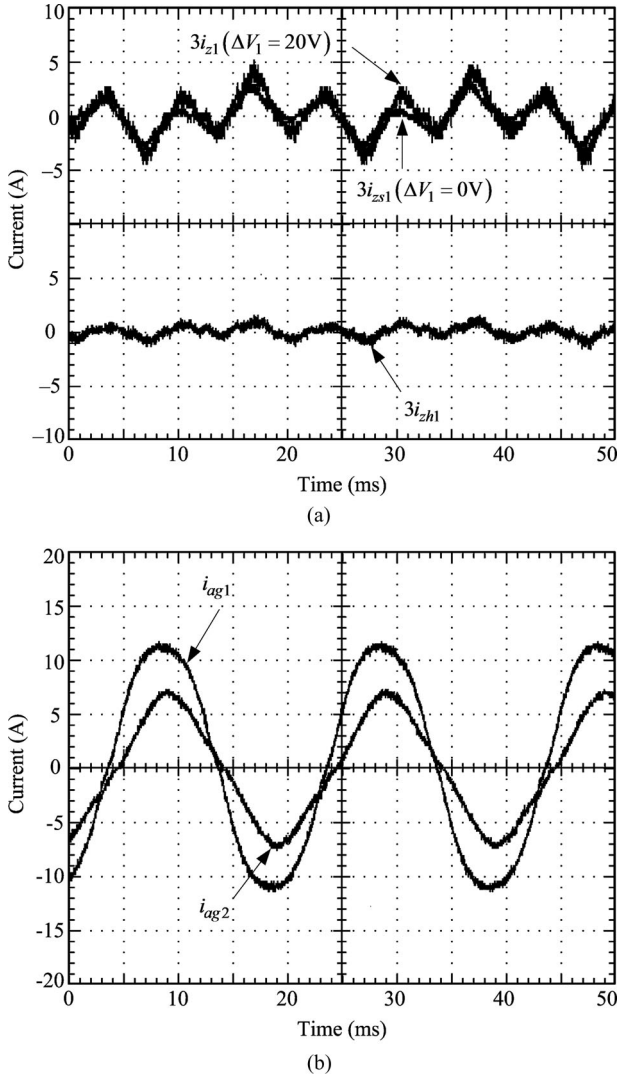

Fig. 19. Experimental waveforms of the hybrid ZSCC and the grid-side currents without the zero-sequence control loops when $\Delta V_1 = 20$ V. (a) The hybrid ZSCC represented by the difference between i_{z1} ($\Delta V_1 = 20$ V) and i_{zs1} ($\Delta V_1 = 0$ V). (b) The grid-side currents.

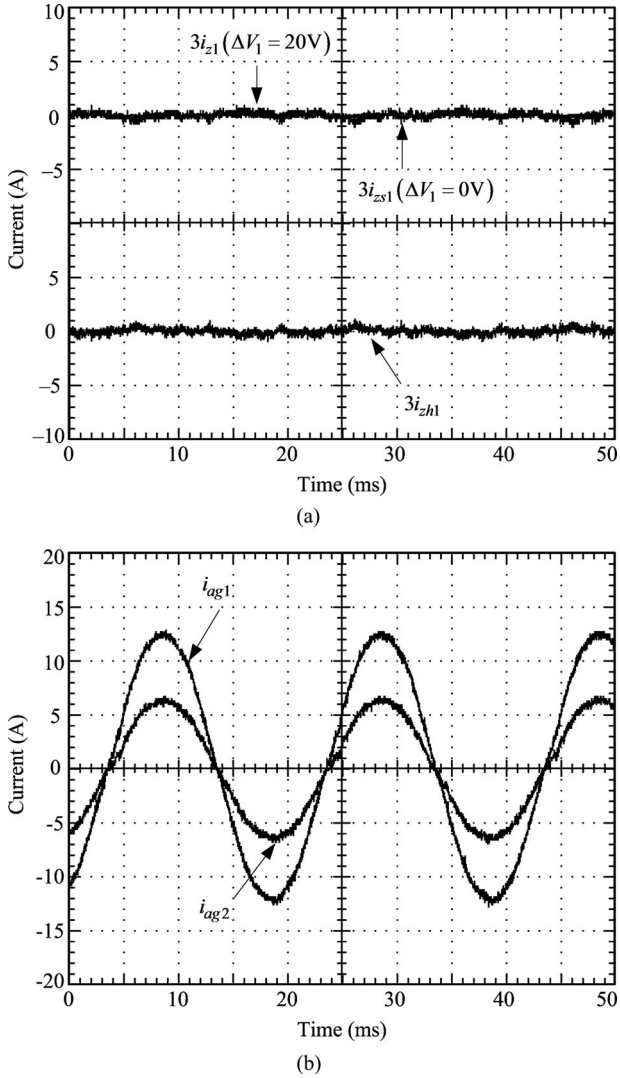

Fig. 20. Experimental waveforms of the hybrid ZSCC and the grid-side currents with the zero-sequence control loops when $\Delta V_1 = 20$ V. (a) The hybrid ZSCC represented by the difference between i_{z1} ($\Delta V_1 = 20$ V) and i_{zs1} ($\Delta V_1 = 0$ V). (b) The grid-side currents.

It is proven that the low-frequency switching ZSCCs are eliminated effectively by the zero-sequence control loops.

D. Experiments for Elimination of the Hybrid ZSCCs

In the experiments of Section V-D, the positive dc bus voltages are 20 V higher than the negative dc bus voltages, which means ΔV_1 and ΔV_2 are both clamped at 20 V. The other experimental environment is the same as Section V-C.

Fig. 19(a) shows the hybrid ZSCC of the first inverter, which is represented by the difference between i_{z1} ($\Delta V_1 = 20$ V) and i_{zs1} ($\Delta V_1 = 0$ V). It is observed that the high-frequency hybrid ZSCC is almost reduced by the modified LCL filter, and the low-frequency hybrid ZSCC is much smaller than the low-frequency switching ZSCC. The grid-side currents in Fig. 19(b) are distorted by the switching ZSCCs and the hybrid ZSCCs.

Fig. 20(a) shows the hybrid ZSCC of the first inverter with the zero-sequence control loop. It is observed that the low-frequency hybrid ZSCC is almost gone and the grid-side currents in Fig. 20(b) are improved greatly.

It is proven that the schemes aforementioned are also effective to the elimination of the hybrid ZSCCs.

VI. Conclusion

This paper has presented the paths and the equivalent model of the ZSCCs in the parallel 3LT^{2}Is. Then, the ZSCCs have been classified into conduction, switching, and hybrid components. In order to eliminate the conduction ZSCCs, an original sharing neutral bus structure was proposed. Meanwhile, to eliminate the high-frequency and low-frequency harmonics of both the switching and hybrid ZSCCs, the modified LCL filters and the zero-sequence control loops were applied, respectively. In order to validate the proposed elimination schemes, a prototype composed of two parallel 3LT^{2}Is was constructed and tested. The experimental results verified the validity of the proposed

models and schemes. The research results of this paper make it possible to manufacture the inverters with higher efficiency and power rating.

Analysis of ZSCC paths of parallel n-level ($n > 3$) inverters becomes complex and difficult, because the paths are proportional to the square of the inverter levels. However, the ZSCCs of parallel n-level inverters are also influenced by switching states or neutral point potentials, and can be divided into conduction, switching, and hybrid components as well. The proposed schemes are also effective.

This paper takes 3LT^{2}I as an example; actually NPC topology and ANPC topology are also applied in the parallel system. They are similar in commutation processes and switching states, and the proposed ZSCC elimination schemes are general. However, there is no dc-bus neutral point in flying capacitor topology, so the proposed schemes are no longer applicable. How to eliminate ZSCCs in parallel flying capacitor multilevel inverters will be future work for this project.

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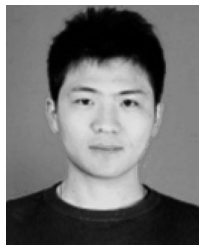

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