Maximum Power Extraction From Series-Connected Fuel Cell Stacks by the Current Compensation Technique

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***Abstract*—Fuel Cell stacks, due to their low voltage output, are usually connected in series to achieve higher voltages in typical high-power applications. Power from individual stacks varies dynamically during their operation because of variation in operating parameters such as temperature, humidity, flow rates, ageing, etc., which results in mismatch of electrical performance of the stacks. When one of the series-connected stacks is under performing, the current from the branch is affected leading to reduced power. This paper proposes a novel scheme, to extract maximum power from series-connected stacks by current compensation which also improves reactants economy. A minimal power-processing (compensating) power converter is used with each stack to achieve maximum power extraction. Since activation of compensation is not effective during low-power operation, an algorithm is developed to implement compensation only for the performance improvement zone. Compensating converters are designed using interleaved fly-back topology, for reduced ripple, with DSP TMS320F2812.The efficacy of the technique is analyzed using Simulink. Experimental results are presented to validate the proposed scheme.**

***Index Terms*—Compensation converter, interleaved fly-back converters, maximum power extraction, performance improvement zone (PIZ), series-connected fuel cell stacks.**

I. Introduction

INCREASED awareness over ever-increasing environmental pollution, depleting fossil fuel reserves, and the ongoing energy crisis have led to tremendous research efforts on renewable and nonconventional energy sources. In this context, a fuel cell power source (FCPS) has emerged as a relatively efficient and clean option for power generation because of its high efficiency and low emissions. Significant progress has been made in optimization of Fuel Cells (FCs) for their use in portable, stationary, and vehicular applications [1].

Being an emerging technology, FCPS incurs higher investments on development and involves high operating cost. Therefore, to get the best returns on the investment, it is necessary that the FCPS is utilized optimally under all operating conditions. The terminal voltage of a typical FC has a nonlinear relationship with load current as well as with other operating parameters such as temperature, fuel and oxidant flow rates, humidity, ageing etc. However, the maximum extractable power from an FCPS varies dynamically during the FC operation for varying load current requirements as the system parameters are also changing [2]. FCs are low voltage and high-current power sources. They are usually connected in series to get reasonable voltage for different applications.

A single stack can have only a limited number of series-connected cells because of the difficulties in achieving uniform reactant concentration, pressure distribution, humidity, and also due to thermal management issues [3]. Hence, to realize a higher power rating FC system, FC stacks must be connected in series. However, this leads to another issue. When one of the series-connected stack is under performing, the output power from the entire series-connected branch is affected. A condition might occur where individual cell voltage reversal and permanent cell damage can occur, because the same current is drawn from all the series-connected FC stacks. To overcome this problem, the current in the concerned branch should be reduced to keep the voltage of underperforming stacks at safe level. This leads to reduced power from the entire FC array.

Extracting maximum power from FCPS has been studied by many researchers [2]–[11]. Recursive estimation of maximum power point tracking (MPPT) for FCPS in vehicular applications has been proposed in [2]. A review of some of the MPPT schemes, including a new scheme based on adaptive extremum seeking algorithm, has been presented by Zhong *et al.* [4]. Various methods of MPPT based on P&O, InC, fractional V_{OC}, fractional I_{SC}, fuzzy logic control, neural network, etc. are described [5], [6] and compared in [7] in terms of speed, design, complexity, etc. Control and manipulation of the air flow rate to maximize net power output using the extremum seeking algorithm is proposed by Rourke *et al.* [8]. MPPT based on internal resistance and by control of concentration loss are described in [9] and [10], respectively. Kelouwani *et al.* [11] have proposed an adaptive control approach for maximum efficiency point tracking of a proton exchange membrane FC with online identification system for providing the best operating conditions. A control strategy to achieve the maximum fuel economy of the FC has been proposed in [12].

It is observed that all the researchers working on extracting maximum power from FCPS have either considered a single FC stack or multiple stacks with uniform power output.

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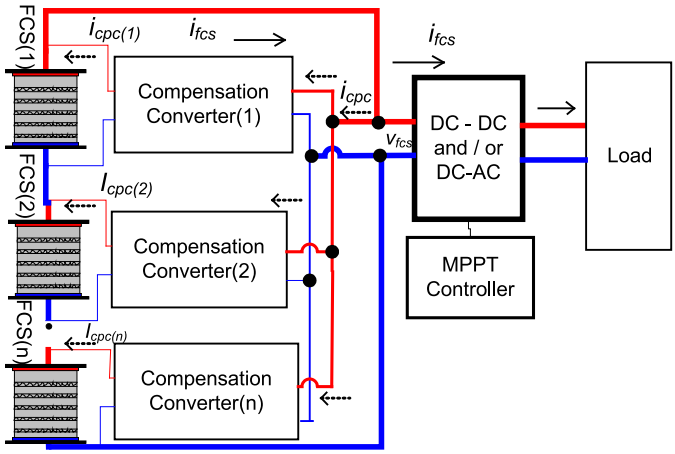

Fig. 1. Series FC stacks with compensation converters.

Nonuniform electrical performance of series-connected FC stacks is not considered for MPPT studies and this remains a challenging research area. Unfortunately, the diode bypass architectures used for certain sources (e.g., series-connected solar PV modules) to handle nonuniform electrical performance, cannot be used in FCPS because the power per FC stack is much higher and bypassing a stack would mean a significant reduction in FCPS output power. Distributed maximum power point tracking (DMPPT) concept has emerged as an effective concept to deal with nonuniform electrical performance and has already been attempted extensively to deal with mismatch and nonuniform electrical performance of series-connected PV modules [13]–[15]. Unfortunately, DMPPT has not been adequately explored with FC stacks to optimize their power output. A literature survey carried out by the authors led only to one paper [3], where an elegant idea of modular FC and modular power converter has been proposed for performance and reliability enhancement. The authors have proposed splitting of the FC stack with higher number of cells into multiple FC sections, each of which is connected to a separate dc–dc converter, all of whose outputs are connected in series. Unfortunately, each converter is required to be designed for full power rating of the respective FC section. Hence, the scheme is full power-processing architecture with multiple converters. Moreover, the authors have not demonstrated the capability of the proposed scheme to track MPP of the FC stack.

This paper presents a novel DMPPT scheme to extract maximum power from series-connected FC stacks. The scheme is shown in Fig. 1. A dc–dc converter is connected in shunt with each FC stack that provides "compensation" current to the underperforming FC stack in order to "equalize" its voltage with the rest of the series-connected FC stacks. Thus, unlike [3], only minimal power-processing compensating converters are required. For the branch current of "i_{fcs}," if the derated current of the nth FC stack is "$i_{fc(n)}$," then the compensating current provided by the nth converter is given by

$$i_{cpc(n)}(t) = i_{fcs}(t) - i_{fc(n)}(t). \tag{1}$$

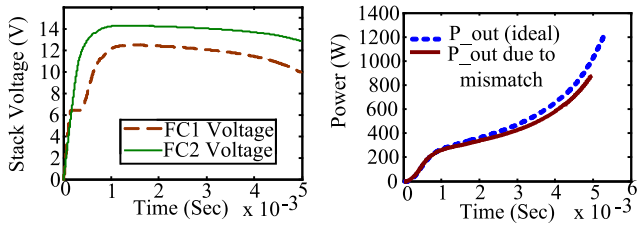

Fig. 2. Mismatch in performance of series-connected FC Stacks (a) Stack voltages, (b) output power.

In the proposed scheme, MPPT algorithm is also implemented in the overall branch power converter and the compensating converters contribute current in parallel with the underperforming FC stacks.

At lower power levels, the auxiliary power requirements of the converters become significant and the net power gain becomes trivial. Therefore, the activation of compensation is found to be ineffective for low-power operation. Hence, to optimize the scheme only for optimum power levels, an algorithm is developed to activate the DMPPT scheme only for the power improvement zone (PIZ). The procedure for PIZ identification is explained in Section II. All the details of this study are presented in the subsequent sections of this paper.

II. Proposed DMPPT Scheme for Series-Connected FC Stacks

The terminal voltage of the FC stacks varies with the load as well as with other operating parameters. The variation in these parameters results in variation of Ohmic resistance (internal resistance), limiting current, and/or the exchange current density. Various degradation phenomena caused by fuel and oxidant starvation related to the FC operation have been explained by Steiner *et al.* [16]. Occurrence of reverse voltage due to reactant starvation and uneven gas distribution is explained in [17]. The cell voltage reversal and permanent damage may occur during operational parameter mismatch conditions and hence, the stack current must be limited by monitoring the stack voltage.

Fig. 2 shows the mismatch in performance of two series-connected FC stacks (of same power rating) in terms of stack voltages along with the power output of the overall FCPS. Each stack has different internal resistance. The FC voltage and the limiting current of the underperforming FC stack restrict the power output from the branch and hence the overall performance deviates from the ideal performance as shown in Fig. 2(b).

This paper proposes a novel scheme based on current compensation to improve the performance of series-connected FC branch. The proposed current compensation scheme, to extract maximum power from series-connected FC stacks, is shown in Fig. 3. This scheme is an optimal power-processing compensation architecture. In this architecture, the current compensating power converters contribute current for equalizing FC stack voltage mismatch. Maximum power from the branch is extracted by implementing an MPPT controller in the power converter connected at the output of the FC stack array.

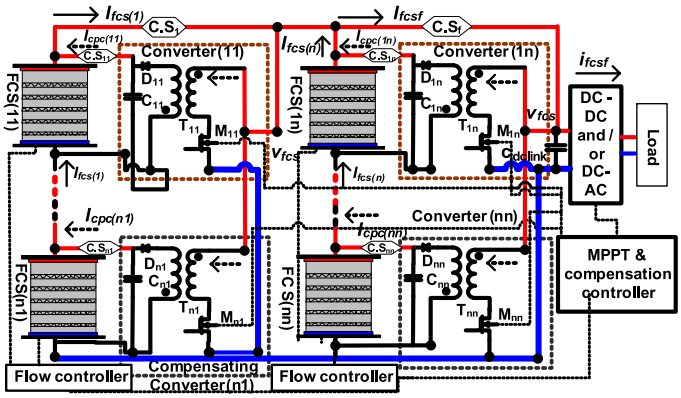

Fig. 3. Proposed current compensation scheme.

The terminal voltage of a FC is given by

$$V_{fc} = V_{\text{rev}} - \eta_{\text{anode}} - \eta_{\text{cahode}} - \eta_{\text{ohmic}} \tag{2}$$

where "V_{rev}" is the theoretical reversible potential, "η_{anode}" is the over voltage (loss) at the anode, "η_{cathode}" is the over voltage at the cathode, and "η_{ohmic}" is the Ohmic loss due to contact resistance and electrolyte resistance.

As per (2), the terminal voltage of FC stack is dependent on the polarization losses at electrodes and Ohmic drop which could result because of variations in different operating parameters, ageing, etc.

The MPPT controller monitors "v_{fcs}," "i_{fcs}" which are series branch voltage and current [Fig. 3], respectively. Hence,

$$v_{fcs}(t) = v_{fc(11)t+v_{fc(21)}(t)....+v_{fc(n1)}}(t) \tag{3}$$

where $v_{fc(11)}, v_{fc(21)}$, and $v_{fc(n1)}$ are the voltages of FC stack (11), FC stack (21), FC stack ($n1$), respectively.

In ideal conditions, the stack voltages are equal and the MPP controller tracks V_{FCSMPP}. However, when one of the series FC stacks exhibits higher Ohmic or polarization losses, the underperforming stack voltage will fall and individual cell voltage will revere, cell damage will occur during MPP tracking.

The compensating converters are connected in parallel with each FC stack. They contribute the current to the weaker FC stacks by power processing from the terminals of the series branch. To decide on the magnitude of current to be compensated by each converter, voltage equalization scheme is proposed. In this scheme, the converters shall try to maintain equal voltages across all the series-connected FC stacks' terminals. This is achieved by providing the average of FC stack voltages as the output voltage reference to the individual converters. The reference voltage to the compensating converters (v_{cpcref}), considering two FC stacks connected in series is given by

$$v_{\text{cpcref}}(t) = \frac{v_{fc(1)}(t) + v_{fc(2)}(t)}{2}. \tag{4}$$

If each branch has "m" number of series-connected FC stacks, the generalized reference voltage for each stack of the branch (1) is given by

$$\text{Hence,} \qquad v_{cpcref(\text{n1})}(t) = \frac{\sum_{n=1}^{m} v_{fc(n1)}(t)}{m}. \tag{5}$$

The output of the converter is regulated by controlling the duty ratio (d) as per the following relation:

$$v_{cpc(\text{nm})}(t) = \frac{d}{1-d} v_{fcs}(t) \tag{6}$$

where "$v_{cpc(\text{nm})}$" is the output voltage of the compensating converter (nm) and "v_{fcs}" is the terminal voltage of the branch. When more stacks are connected in series, the branch voltage will be very high and the higher conversion ratio may increase loss across the converters. However, in the proposed scheme, the compensating converters perform minimal power processing. Hence, the increased loss magnitude would not be significant.

The compensating current ($i_{cpc(\text{nm})}$) for converter (nm) is given by

$$i_{cpc(\text{nm})}(t) = i_{fcs(n)}(t) - i_{fc(\text{nm})}(t). \tag{7}$$

Using Faraday's electrochemical equations, the rate at which H_2 and O_2 are consumed is given as

$$g\text{H}_2(\text{nm}) = \frac{i_{fc(\text{nm})}}{2F},\ g\text{O}_2(\text{nm}) = \frac{i_{fc(\text{nm})}}{4F} \tag{8}$$

where "g" is the gas consumption rate (mols^{-1}), "$i_fc(nm)$" is current(Amps) from FC stack (nm), and "F" is Faraday's constant (=96485 Cmol^{-1}).

The underperforming FC stack current "$i_fc(nm)$" is less than the branch current "$i_{fcs(n)}$." Hence, the flow rate of reactants through the derated FC stack is reduced based on (8), which results in reactant fuel and oxidant economy.

Interleaved fly-back converters are designed to implement current compensation using "TMS320F2812" DSP controller. Interleaved operation increases effective operating frequency, reduces ripple current into FCs and results in smaller filter component values [18], [19].

The low-frequency current ripple propagation to FC is of concern for ac loads. The passive and active compensation techniques are studied to reduce the undesired low-frequency FC current ripple. Filters with passive elements can be used to reduce current ripple in the dc-link between the FC and the inverter. Approaches that do not require large-sized electrolytic capacitors to reduce current ripple have been proposed by many researchers [20]–[24].

A. MPPT Algorithm

The algorithm to track MPP from the overall stack array is required to be implemented either in the full power-processing converter or inverter as shown in Fig. 3.The popular P&O algorithm is used to implement MPPT, though any other MPPT scheme could also be used. In this scheme, a positive or negative perturbation ΔI) is applied to FC current based on observation of FC power output.

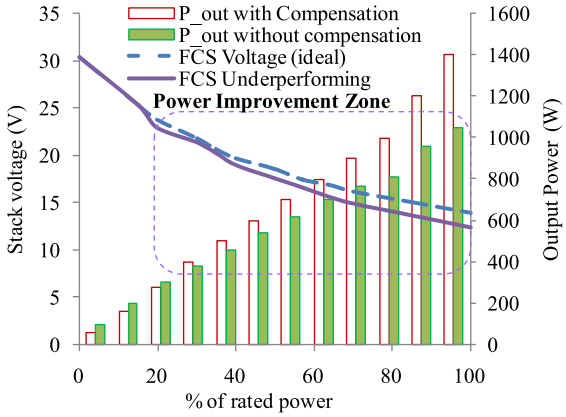

Fig. 4. PIZ identification.

B. Algorithm for the PIZ

The compensation is found to be ineffective at low-power operation as the auxiliary power of the converters becomes significant. Hence, to optimize the scheme only to optimum power levels, an algorithm is developed to activate the DMPPT scheme only for the PIZ. The algorithm identifies the PIZ based on the real-time electrical voltage and power characteristics and gives signal to the compensating converters either to start or stop the gate pulses to the power switches.

In the *V–I* characteristic curves of FCs, at low current, the activation voltage losses are dominant and as the current increases and the Ohmic losses get added up. When compensating converters are activated, their auxiliary power consumption becomes prominent and the output power with the compensating converters results in an overall low-output power at lower load current. At low-power level, the FC stacks operate in activation polarization region of *V–I* characteristics. In this region, the compensation is ineffective as the underperforming and ideal stacks have similar performance since low current is drawn from FC stacks. When the current is further increased, the characteristic curve moves into Ohmic region where the underperformance is dominant due to nonuniform reactant distribution and electrolyte resistance plays an important role. Hence, the PIZ is identified to be the Ohmic region.

The compensation is also not activated, when the system is operational with load and stack voltages are equal, i.e., no abnormality. The PIZ is found to be effective when the difference in underperforming stack voltage is greater than ≈2 V. This condition is checked at the initial activation of current compensation. As shown in Fig. 4, the PIZ is found to be approximately beyond 20% of the rated power (shown with dotted line). It is determined in real time during operation. An algorithm for "m" number of series-connected stacks,, as shown in Fig. 5, has been developed to activate the compensating converters in the PIZ. To prevent chattering at the boundary of PIZ, a lower limit (PIZ_UL) and an upper limit (PIZ_LL) is defined for hysteresis control.

III. Simulations

The current compensation technique for the series-connected FC stacks is analyzed by developing phosphoric acid fuel cells

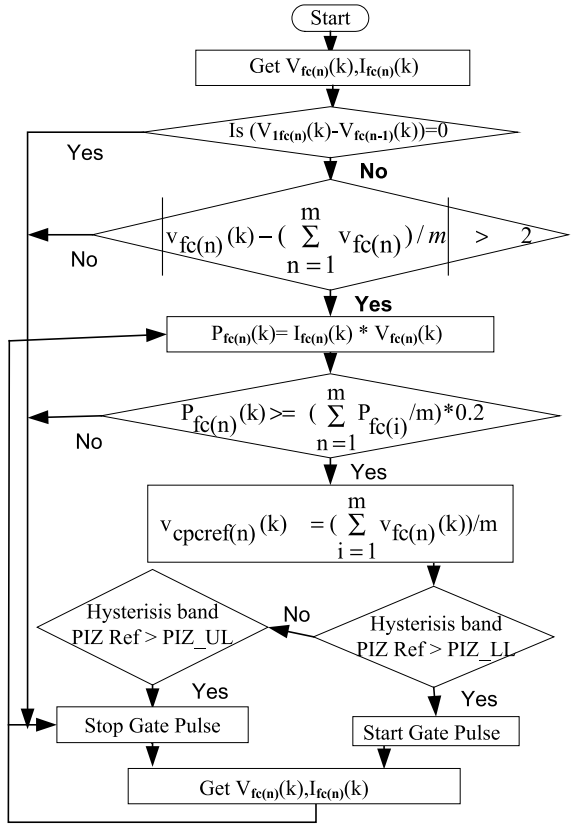

Fig. 5. Flowchart for compensation activation in PIZ.

TABLE I
Parameters of the FC Model

Parameter	Value
N (No. of cells)	30
$N.E^0$(Open circuit voltage)	24.5 (V)
K_{H2} (H_2 valve molar constant)	8.4×10^{-5} (kmol/s.atm)
K_{O2} (O_2 valve molar constant)	2.51×10^{-5} (kmol/s.atm)
K_{H20} (H_2O valve molar constant)	$2.8\text{x}10^{-6}$ (kmol/s.atm)
τ_{H2} (H_2 time constant)	1.25 (s)
τ_{O2} (O_2 time constant)	2.91(s)
τ_{H2o} (H_2O time constant)	7.83(s)
m (constant)	0.05
n (constant)	0.011
i_L (Limiting current)	90 (A)
R_{ohm} (Ohmic resistance)	0.185 (Ohms)
F (Faraday Constant)	96480 (C)

(PAFC) stack and converter models using Simulink. The valve constants for reactant flow are included in the model of PAFC for dynamic power characteristics. The parameter description and values used in the model are listed in Table I. The model equation of PAFC stack is given by

$$V_{FC} = N\cdot E^0 + \frac{RT}{nF}\ln\left(\frac{\left(q_{\mathrm{H}_2}^{\mathrm{in}} - 2K_rI\right)\bullet\left(q_{O_2}^{\mathrm{in}} - K_rI\right)}{(2K_rI)}\right) - T\,b\ln(I) - I\left(R_{\mathrm{ohm}0} + K_{RI}I - K_{RT}T\right) - \frac{RT}{nF}\ln\left(1-\frac{i}{i_L}\right) + \frac{3RT}{2F}\ln\mathrm{P}. \quad (9)$$

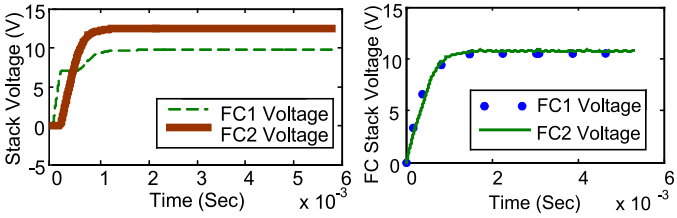

Fig. 6. Simulation results of FC stack voltages (a) without compensation, (b) with compensation.

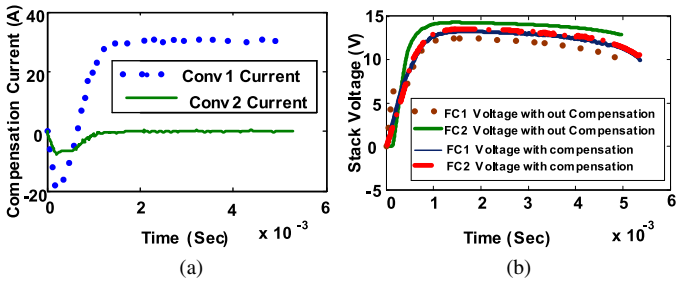

Fig. 7. Simulation results (a) compensation current with constant load (a) FCS voltages with and without compensation.

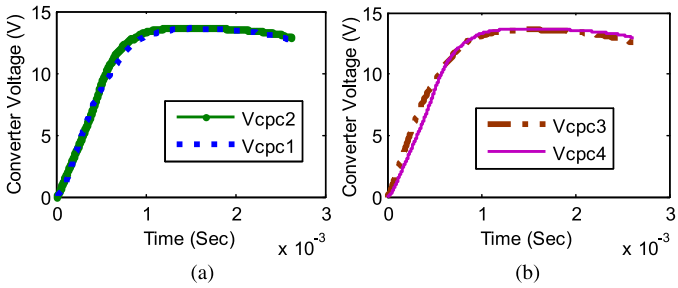

Fig. 8. Voltage waveforms with compensation (a) converters1, 2, and (b) converters 3, 4.

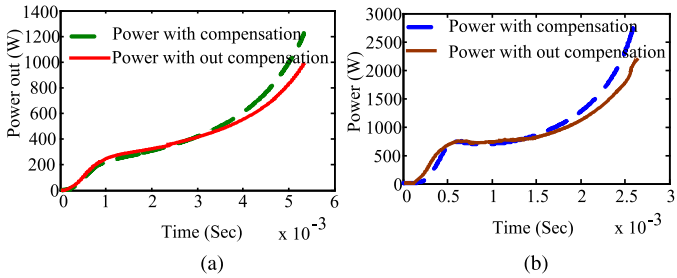

Fig. 9. Power output with and without compensation (a) for a 2×1 FC stack array, (b) for a 2×2 FC stack array.

A model of interleaved fly-back converters is also developed in MATLAB/ Simulink. When the switch "M_1" [see Fig. 3] is ON, the series voltage $V_{\rm FCS}$ is connected to the dotted end of the primary winding of the transformer and the current builds up in its magnetizing inductance, L_m. The induced voltage in the secondary makes the diode "D_1" reverse biased. When the power switch "M_1" is OFF, the voltage polarities across the windings get reversed as the current path in primary winding is broken and thus the diode D_1 gets forward biased. The stored energy in L_m causes current to flow in the output as well as charging current of the output capacitor C1 as shown in Fig. 3. The volt–second balance of the winding gives the expression for output voltage as follows:

$$v_o(t) = \frac{d}{1-d} r v_{fcs}(t) \tag{10}$$

where "d" is the duty cycle, "r" is the turn ratio ($=N_s/N_p$), where N_p is the number of primary winding turns and N_s is the number of secondary winding turns. The reference voltage for the converter (nm) output is given by

$$v_{\rm ref(nm)}(t) = v_{\rm cpcref(nm)}(t). \tag{11}$$

Simulations are carried out with 2 × 1 and 2 × 2 FC stack arrays. Initially, the simulation results of 2 × 1 array are presented. Two compensating converters are modeled based on interleaved fly-back topology using the branch terminal voltage as the input. One of them is modeled with an Ohmic resistance of 0.089 Ω ($R_{\rm ohmic}$) and the other stack with 0.001 Ω. For the same hydrogen flow rate of 20 l/min (l/min), the stack voltage levels for a constant load without compensation converters are shown in Fig. 6(a). The FC stack (FCS-1) is underperforming and hence, its voltage is less than that of FCS-2. When the interleaved converters are operated to compensate current, the equalized stack voltages and compensating currents are as shown in Fig. 6(b). The converters compensate the current and increase the voltage of the underperforming stack and equalize with the branch average voltage. The compensation current of converter 1 is more than that of converter 2 as higher current is required to compensate for the underperformance of FCS-1.

The compensation current for a constant load is shown in Fig. 7(a), and when MPPT algorithm is applied with changing load, the voltages of the series-connected FC stacks and the output power with and without current compensation are shown in Fig. 7(b).

Simulations are also carried out with 2 × 2 FC stack arrays. In column1, the FC stack1 and stack 2 described previously are used. In column 2, FC stack 3 is modeled with an Ohmic resistance of 0.055 Ω ($R_{\rm ohmic}$) and the stack 4 with 0.002 Ω. Hence, in the entire branch, FC stacks 1 and 3 are underperforming. When the compensation converters are activated, the equalized voltages are shown in Fig. 8.

The output power curves, shown in Fig. 9(a), reveal an improvement of up to 25% in the output power for 2 × 1 FC stack array and show an improvement of up to 23% in output power with compensating currents for the 2 × 2 FC stack array, shown in Fig. 9(b).

The output power per stack with and without compensation, shown in Fig. 10, reveal that the output power with compensation results in the reduction of produced power output at lower power operation of the FC system. It also reveals that the PIZ is located beyond 140 W.

The algorithm to initiate compensation, only in the PIZ, is implemented and compensation currents are shown in Fig. 11. The negative current (in Fig. 11) is due to the initial charging

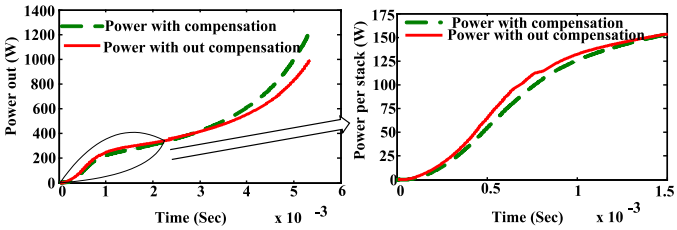

Fig. 10. Output power per stack of series-connected stacks with and without compensation.

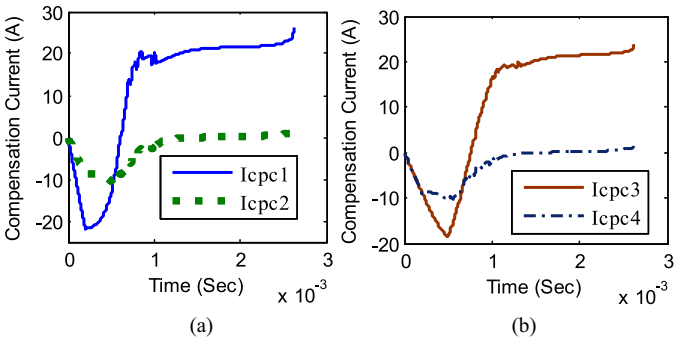

Fig. 11. Waveforms of compensation current (a) converters 1, 2, and (b) converters 2, 3.

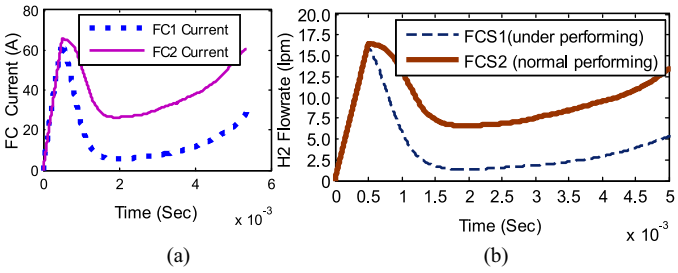

Fig. 12. Wave forms with compensation (a) FC stack currents, (b) H_2 flow rate for FC stacks.

current of the filter capacitors at the output of the compensating converters.

In the normal operation of series-connected FC stacks, as the same current is drawn from all the FC stacks, the reactant flow rates are required to be equal. The underperforming FC stacks cannot consume the same quantity of reactants equivalent to the better performing stacks. Since the current demand on the underperforming stack is reduced [see Fig. 12(a)] due to the additional current from compensating converters, the required flow rate is required to be reduced as compared to the normal performing stack. The reduced reactant gas flow is controlled based on (8). The underperforming stack FCS-1 flow rate is less than FCS-2, with current compensation, as shown in Fig. 12.

IV. Experimental Results

To verify the proposed scheme, PAFC stacks (rated 700 W) in the form of 2×1 array are considered due to the availability in the lab. However, the scheme can be extended to an "$m \times n$" array also. Current compensating prototype fly-back converters of rating 200 W are designed to implement the proposed scheme.

TABLE II
Design Parameters of the Converter

Parameter,unit	Value
V_{inmin}, V	24
V_{inmax} ,V	60
Switching Frequency (f_s) ,Hz	20000
Converter Output (V_o) ,V	20
Peak Input current (I_{pp}), A	26
Transformer Inductance (L_p), μH	550
Airgap (L_g), μm	150
Max. Secondary current (I_s), A	21
Primary Turns (N_p) ,Turns	7
Secondary Turns (N_s), Turns	2
Duty Cycle (max), D_{max}	0.75
Primary current ripple (ΔI)	20 %
Proportional gain (K_p)	0.006
Integral gain (K_I)	0.35

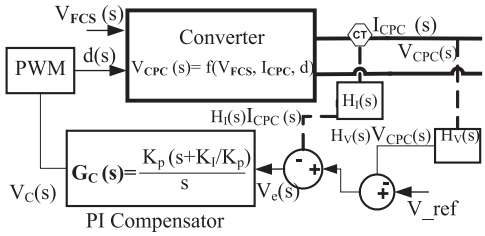

Fig. 13. Control scheme for the compensation converters.

Amorphous core AMCC16A is used for high-frequency transformer and IRF3710 MOSFET is used as the switching device in each converter. The design parameters of the converter are shown in Table II.

The TI DSP, TMS320F2812 controller was used to control the compensating current by varying the duty ratio of the gating pulses to MOSFET switches IRF3710. Average current mode control with PI compensator is implemented using the DSP. The compensator parameter values are included in Table II. The schematic of the current mode control is shown in Fig. 13. The average current mode control has the advantage of superior noise margin and better voltage and current regulation along with simple compensation [25]. The error amplifier output is compared with a saw tooth waveform to generate pulse width modulation signals. The converter current is controlled by forcing the output voltage to track the reference with suitable compensation of the error amplifier. To achieve high gain and output stability, compensation of error amplifier is needed. PI compensation increases the low-frequency loop gain, improves disturbance rejection, and reduces the steady-state error. Sufficient gain and phase margin is required to prevent overshoot and ringing. This is achieved with proper values of K_p and K_I, which are given in Table II.

The compensating converters were operated at 20-kHz switching frequency. Hall effect current transducers "HAS-50-P" from LEM are used for current sensing. The fly-back converters are operated at 180° phase shift to realize interleaved operation. The regulated dc voltage is applied to the individual stack terminals. The hardware setup of the converters for current compensation is shown in Fig. 14.

Fig. 14. Experimental setup: compensation converters along with TMS320F2812 controller.

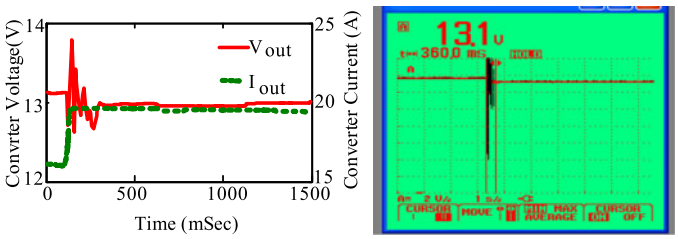

Fig. 15. Waveforms of converter step response (a) Simulation and (b) experimental.

The stability of the converter output using PI compensator is verified with step response by simulation and experimental study as shown in Fig. 15. As revealed from the figures, after step load variation, the compensation converters reach steady state within 250–350 ms. The output voltage of each converter is sensed and fed to the ADC channel of the TMS320F2812. The steady-state error after step load change (in Fig. 15) is due to the load regulation of the converter which is near about 1%. Hence, as the load is increased, there is a small steady-state error (fall) in converter output voltage.

The input to the converter is given from the stack array output. The PAFC stacks described in [22], are used for this study. The OCV of the FC stacks is 25 V and cutoff voltage is 10 V. Programmable electronic load has been used for changing load current.

The experimental *V–I* curves for the FC stacks, shown in Fig. 16(a), reveal that the load current cannot be increased beyond 37A as FC stack 1 has reached the cutoff voltage but FC stack 2 can still deliver more (higher) power. Since both the stacks are in series, FC stack 1 has become the power limiting member. When compensating converters are used, the resulting FC stack voltages are shown in Fig. 16(b).

The power that can be extracted from series-connected FC stacks is improved by nearly 25% with the current compensation as shown in Fig. 17(a). To avoid decremented output power at lower load currents, the algorithm shown in Fig. 5 is implemented and the activation of compensation in PIZ is achieved as shown in Fig. 17(b).

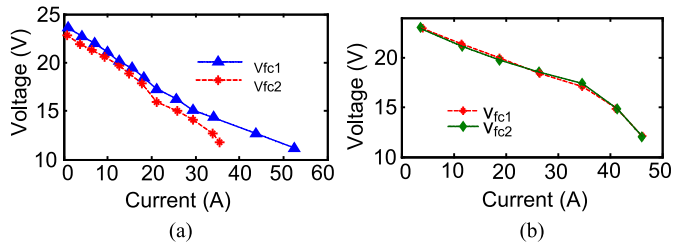

Fig. 16. Experimental *V–I* curves for series-connected FC stacks (a) without compensation (b) with compensation.

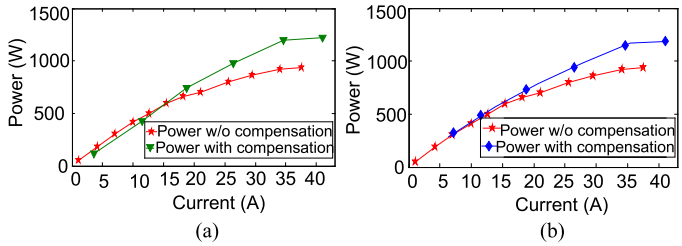

Fig. 17. Experimentally obtained power curves with (a) PIZ and (b) without PIZ algorithm activation.

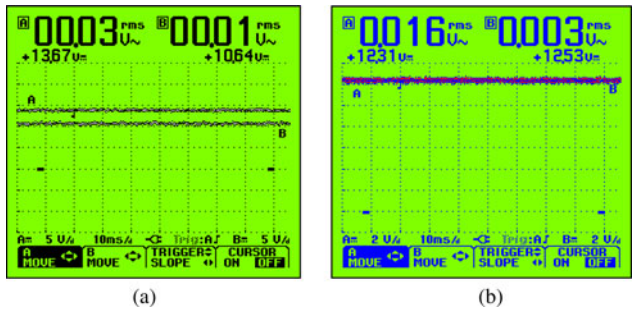

Fig. 18. Voltage waveforms of series FC Stacks (a) without and (b) with compensation.

FC stacks voltage waveforms with and without current compensation captured using scope meter (Fluke 124) are shown in Fig. 18. Without compensation converters, the voltage of the underperforming FC stack 2 drooped down to the lower limit of 10.64 V dc [see Fig. 18(a) waveform (B)]. But, by activating the compensation converters, the voltage has been improved to 12.53-V dc [see Fig. 18(b) waveform (B)].

V. Conclusion

Electrical performance of the series-connected stacks is usually nonuniform because of variations in operating parameters. Because of this, the underperforming FC stack(s) become the power limiting element(s) for the branch. In this study, a novel scheme is proposed to extract maximum power from series-connected stacks by current compensation and also to achieve reactant flow economy. As activation of compensating converters is ineffective during low power operation, an algorithm is developed to activate compensation only in PIZ. As the current demand from the underperforming FC stack is reduced, the

reactant flow rates are decreased with a flow controller which resulted in flow rate economy. Interleaved fly-back power converters are designed for implementing current compensation using TI DSP TMS320F2812. Interleaving technology is implemented in the converters as FCs prefer reduced ripple. Compensating converters of 30% of the FC stack power rating are used as the power converter with higher rating becomes uneconomical, inefficient, and bulky. The proposed scheme is analyzed and verified for a 2×2 FC stack array. However, it can be extended to a general "$m \times n$" array. The power that can be extracted from series-connected FC stacks is found to be improved by nearly 25% with the current compensation. As the compensation converters are not full power processing and their power rating is very less, the additional cost burden is comparatively negligible in comparison with the gain in output power. Also, as they are connected in shunt with the FC stack, the converter failure does not cause a breakdown of the system. Hence, the system reliability is not affected adversely.

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Authors' photographs and biographies not available at the time of publication.