Design and Analysis of Class E/F_3 Power Amplifier with Nonlinear Shunt Capacitance at Nonoptimum Operation

Mohsen Hayati, Akram Sheikhi, and Andrei Grebennikov, *Senior Member, IEEE*

***Abstract*—This paper presents analytical expressions for the Class-E/F_3 power amplifier with a nonlinear shunt capacitor for satisfying the nonoptimum condition at 50% duty ratio. The design parameters for achieving the nonoptimum condition are expressed as a function of the phase shift and dc supply voltage. The Class-E/F_3 amplifier with nonoptimum condition increases one design degree of freedom compared with the optimum conditions. Because of the increase in the design degree of freedom, one more relationship can be specified as a design specification. The following parameters series reactance, peak switch voltage, output power capability, and maximum operating frequency are presented. Based on analytical results, an example of the Class E/F_3 at operating frequency of 4 MHz is analyzed. The PSpice simulation and measured results agree with the analytical expressions, which show the validity of our analytical expressions at zero-voltage switching.**

***Index Terms*—Mixed mode, nonlinear capacitance, nonoptimum operation and zero-voltage switching (ZVS), power amplifier.**

I. Introduction

THE nonoptimum operation of the amplifier occurs when the zero-voltage switching (ZVS) condition is satisfied, but the zero-voltage-derivative switching (ZDS) is not equal to zero at the switch turns ON instant. The concept of nonoptimum operation of the Class-E amplifier was defined in the beginning of the Class-E history [1]–[4]. The first research on nonoptimum operation has been done by Raab [1]. In this paper, the degree of freedom for the design amplifier was increased, and the ZDS condition was removed. The mixed-mode power amplifiers are the good choice for obtaining high-power and high conversion efficiency. The optimum conditions of the mixed-mode power amplifier families with a shunt capacitor have been presented in [5]–[7]. But the exact analysis on switch mode PAs are not presented. However, all of the Class-E/F amplifier analyses focus on how to achieve the optimum operation. Many power electronic devices only need to ZVS or zero-current switching (ZCS) condition [8]–[20]. In order to reach a Class E power amplifier with good performance, some methods have been suggested and implemented. The first method employs the push/pull topology to Class E in order to short odd harmonic like inverse Class F (demonstrated Class E/F PA). This configuration improved the amplifier performance such as maximum operating frequency and caused the reduction of maximum switching voltage to have maximum output power capability [21], which only in the ZVS is considered. But the nonoptimum condition in the push/pull topology is considered with linear shunt capacitance. The second method is harmonic tuning in which a resonance network is inserted between the drain node and ground. In comparison with Class E amplifier, the performance of the power amplifier can be improved at the cost of the complicated circuit design [6]. Besides the aforementioned methods, some Class E amplifiers consist of resonance networks tuned at nonharmonic frequencies. Nonharmonic resonance network consists of parallel finite dc feed inductor and parallel drain to source capacitor [22], [23] and the series parallel resonance network at the drain node [24]. In [25], a parallel *LC* resonator, tuned to the second harmonic of the switching frequency, is added into the load network of the Class-E amplifier, in which the significant improvement in output power capability is achieved. Up to 10 MHz, the power amplifier with nonoptimum condition can reach high power conversion efficiency, so the analysis of the power amplifier at nonoptimum condition is very important.

In this paper, the analytical expressions of the Class-E/F_3 power amplifier with a shunt capacitor at the nonoptimum operation are presented. For the verification of our analytical expressions, design examples of the Class-E/F_3 ZVS amplifier are presented. The design equations, switch, and output waveforms are obtained as a function of the phase shift and dc supply voltage. By changing the peak switch voltage and the peak switch current, the phase shift is changed, so these two parameters can be considered as a design specification. The measurement and PSpice-simulation results are in good agreement with the analytical results. Design procedures are given for one example of Class E/F_3 amplifiers for nonoptimum operation. In the example, operating frequency, input dc supply voltage, load resistance, and peak switch voltage are given as design specifications. In the nominal circuit, only three parameters such as operating frequency, input dc supply voltage, and load resistance can be designated. On the contrary, the example procedures presented here have four given parameters. The additional parameters, peak switch voltage or peak switch current can be taken into account in the design procedure. This power amplifier is implemented with the IRF510 MOSFET. From the breakdown voltage

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M. Hayati and A. Sheikhi are with the Department of Electrical Engineering, Faculty of Engineering, Razi University, Tagh-E-Bostan, Kermanshah-67149, Iran (e-mail: mohsen_hayati@yahoo.com; akram.sheikhi2008@gmail.com).

A. Grebennikov is with the Bell Laboratories, Alcatel-Lucent, Dublin 15, Ireland (e-mail: grandrei@ieee.org).

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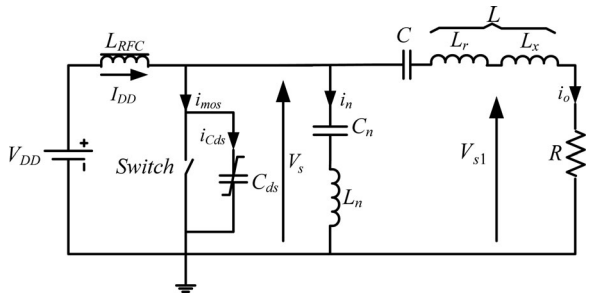

Fig. 1. Circuit and model of class-E/F$_n$ power amplifier analyzed in this paper.

point of view, it is proven that the IRF510 MOSFET is a proper device.

II. Circuit Analysis

The circuit analyzed in this paper is a Class E/F$_3$ amplifier which shown in Fig. 1. The shunt capacitance of the amplifier consists only of the MOSFET output parasitic capacitance which is nonlinear. The derivations of design equations are carried out under the following assumptions:

1) the inductance of the choke $L_{\rm RFC}$ is large enough to neglect its current ripple;
2) the loaded quality factor Q of the output resonance circuit is high enough so that the output current can be considered as a sine wave;
3) the on and off resistance of the MOSFET is zero and infinite, respectively;
4) the shunt capacitance C_{ds} is entirely composed of the MOSFET output capacitance. The grading coefficient of the MOSFET output capacitance is 0.5. The shunt capacitance is described by

$$C_{ds} = \frac{C_{j0}}{\sqrt{1+\frac{v_s}{V_{bi}}}} \tag{1}$$

where V_{bi} is the built-in potential, which changes from 0.5 to 0.9 V, v_s is the switch voltage, and C_{j0} is the capacitance at $v_s(0)=0$;

5) the loaded quality factor Q of the output resonant circuit is defined as

$$Q = \frac{\omega L}{R}. \tag{2}$$

The quality factor Q is high enough to generate a sinusoidal output current

$$i_o = I_M \sin(\theta+\varphi) \tag{3}$$

where I_M is the amplitude of the output current, $\theta=\omega t$, ω is the angular switching frequency, and φ is a phase-shift between the gate-to-source voltage and the output current. The current through the shunt capacitance produces the switch voltage. The switch-voltage waveform satisfies the ZVS conditions at the switch turn-on instant. We assume that the switch for $0<\theta<\pi$ is OFF, so we have

$$v_s(\pi) = 0. \tag{4}$$

The current through the MOSFET device is

$$i_{\rm MOS}(\theta) = I_{DD} - I_n \sin(n\theta) - I_M \sin(\theta+\varphi) \tag{5}$$

and on the other hand, the current of the MOSFET is depicted as

$$i_{\rm MOS}(\theta) = i_s(\theta) + i_{Cds}(\theta) \text{ for } 0<\theta<\pi. \tag{6}$$

So during the off-state, $0<\theta<\pi$, the current of the MOSFET is depicted as

$$i_{\rm MOS}(\theta) = i_{Cds}(\theta) = \frac{\omega C_{j0}}{\sqrt{1+\frac{v_s}{V_{bi}}}}\frac{dv_s}{d\theta} \tag{7}$$

where, $i_{Cds}(\theta)$ is the current through the MOSFET parasitic capacitance. From (7) and $v_s(0)=0$, we obtain

$$\int_0^\theta i_{\rm MOS}(\theta')\,d\theta' = \omega\int_0^{v_s}\frac{C_{j0}}{\sqrt{1+\frac{v_s'}{V_{bi}}}}\,dv_s', \text{ for } 0<\theta<\pi. \tag{8}$$

By substituting (6) into (8), we have

$$\int_0^\theta [I_{DD} - I_n\sin(n\theta) - I_M\sin(\theta+\varphi)]\,d\theta' = \omega\int_0^{v_s}\frac{C_{j0}}{\sqrt{1+\frac{v_s'}{V_{bi}}}}\,dv_s', \text{ for } 0<\theta<\pi. \tag{9}$$

From (9), we obtain

$$v_s(\theta) = V_{bi}[(h(\theta)+1)^2 - 1] \tag{10}$$

where

$$h(\theta) = \frac{I_{DD}\theta + \frac{I_n}{n}(\cos(n\theta)-1) + I_M(\cos(\theta+\varphi)-\cos(\varphi))}{2\omega V_{bi}C_{jo}}. \tag{11}$$

By substituting $\theta=\pi$ and (4) into (10), we obtain

$$I_{DD}\,\pi + \frac{I_n}{n}(\cos(n\pi)-1) - 2I_M\cos(\varphi) = 0. \tag{12}$$

The relative amplitude of the nth harmonic component for any n can be obtained [7] as

$$I_n = \frac{4I_{DD}}{n\pi}. \tag{13}$$

By substituting (13) into (12), for $n=3$, we have

$$I_{DD} = \frac{18\,\pi}{9\pi^2-8}\,I_M\,\cos(\varphi). \tag{14}$$

In power amplifier, the dc-supply power P_I

$$P_I = V_{DD}\,I_{DD} \tag{15}$$

and the output power P_o is

$$P_o = \frac{R\,I_M^2}{2}. \tag{16}$$

The power conversion efficiency is

$$\eta = \frac{P_o}{P_I} = \frac{R\,I_M^2}{2\,I_{DD}\,V_{DD}} = 1. \tag{17}$$

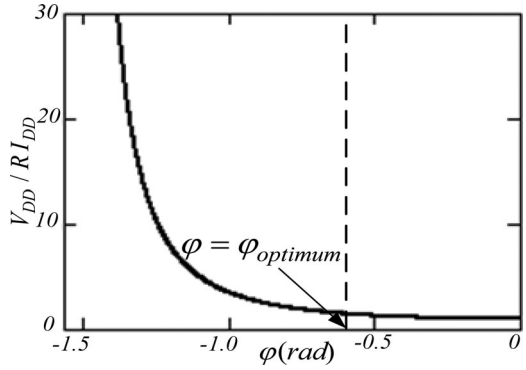

Fig. 2. Normalized input resistance V_{DD}/RI_{DD} as a function of φ.

It is assumed that there is no power losses in the circuit since, in any cases different from optimum Class E with zero-voltage and zero voltage-derivative conditions, there exists a nonzero value of current through the drain-source capacitance at $\omega t = \pi$, which means that the existing nonzero voltage across the capacitance should be discharged instantaneously through the ideal switch with zero resistance.

From (14) and (17), the amplitude of the output current is

$$I_M = \frac{36\,\pi}{9\pi^2 - 8}\,\frac{V_{DD}\,\cos(\varphi)}{R} \tag{18}$$

and the amplitude of the output voltage

$$V_M = RI_M = \frac{36\,\pi}{9\pi^2 - 8}\,V_{DD}\,\cos(\varphi) \tag{19}$$

and the dc-supply current is

$$I_{DD} = \left(\frac{18\,\pi}{9\pi^2 - 8}\right)^2 \frac{2V_{DD}\cos^2(\varphi)}{R}. \tag{20}$$

As can be seen from Fig. 2, the normalized input resistance is a function of the phase shift and it decreased as phase shift φ increased. The dc-supply and output power is

$$P_I = P_o = I_{DD}V_{DD} = \left(\frac{18\,\pi}{9\pi^2 - 8}\right)^2 \frac{2\,V_{DD}^2\cos^2(\varphi)}{R}. \tag{21}$$

The shunt capacitance current at the switch turn-on instant is obtained as

$$\begin{aligned} i_C(\theta)|_{\theta=\pi} &= I_{DD} - I_M\sin(\theta+\varphi) - I_n\sin(n\theta) = I_{DD} + I_M\sin(\varphi) \\ &= 2\left(\frac{18\,\pi}{9\pi^2 - 8}\right)\frac{V_{DD}}{R}\cos(\varphi)\left[\left(\frac{18\,\pi}{9\pi^2 - 8}\right)\cos(\varphi) + \sin(\varphi)\right]. \end{aligned} \tag{22}$$

The normalized switch voltage for different value of φ, is shown in Fig. 3. The switch turns ON with the switch voltage declining and the ZVS condition is satisfied. As can be seen from Fig. 3(a) and (b), when $\varphi < \varphi_{\rm optimum}$ and $\varphi > \varphi_{\rm optimum}$, the switch turns OFF and the ZVS condition is satisfied but ZDS condition is not satisfied. But at optimum condition $\varphi = \varphi_{\rm optimum}$, the ZVS and ZDS conditions are achieved. The normalized output current amplitude $I_M R/V_{DD}$, output power $P_o R/V_{DD}^2$, and shunt capacitance current Ri_C/V_{DD}

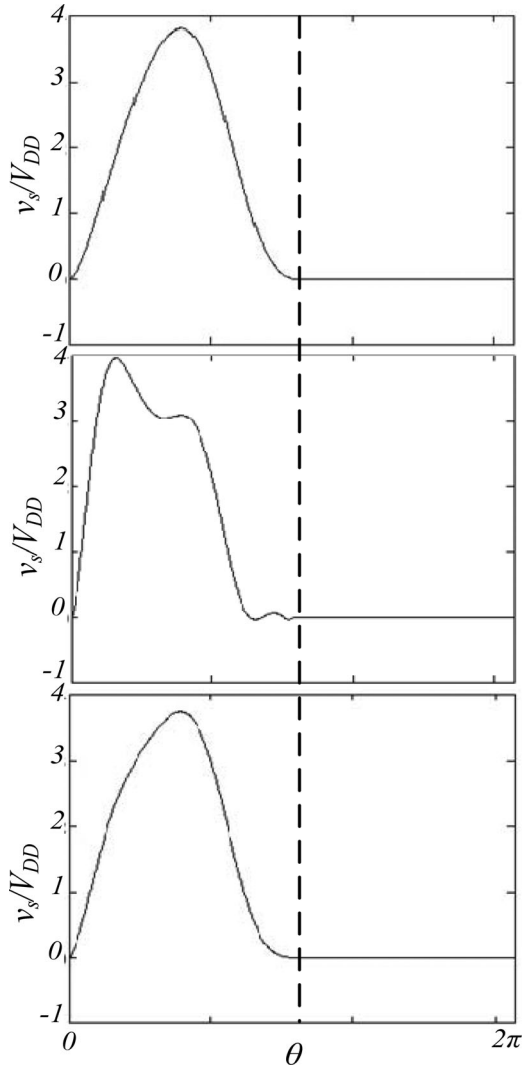

Fig. 3. Typical normalized switch voltage (a) for $\varphi < \varphi_{\rm optimum}$, (b) $\varphi > \varphi_{\rm optimum}$, and (c) $\varphi = \varphi_{\rm optimum}$.

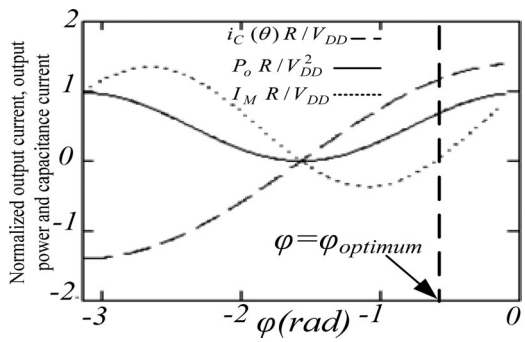

Fig. 4. Normalized output current amplitude $I_M R/V_{DD}$, output power $P_o R/V_{DD}^2$ and shunt capacitance current $R\,i_C/V_{DD}$ as a function of φ.

at the switch turn-on instant as a function of φ are shown in Fig. 4. For nonoptimum operation, the operating range is $-\pi/2 < \varphi < -0.61$ rad. The output power P_o is zero at $-\pi/2$. In this case, the dc input current I_{DD} is zero and the switch voltage waveform is a part of a sinusoidal waveform. The switch

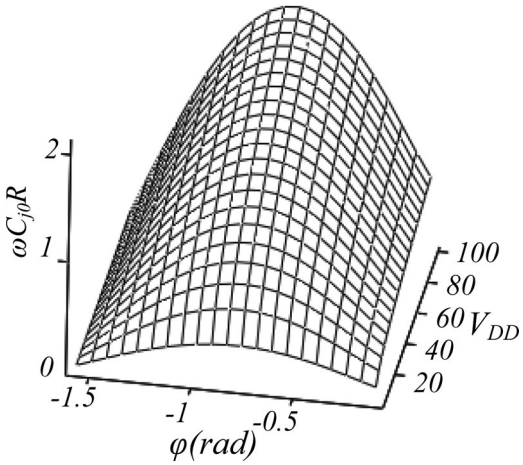

Fig. 5. Variation of $\omega C_{j0}R$ as a function of V_{DD} and φ.

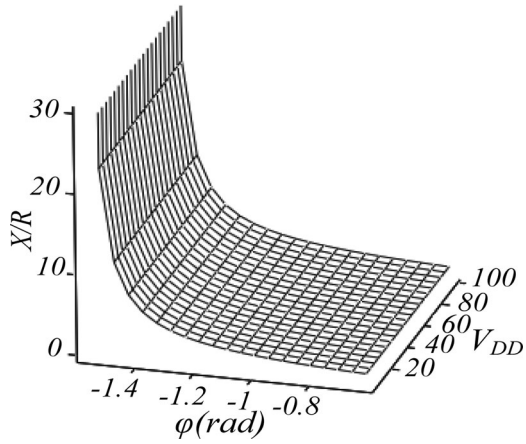

Fig. 6. Variation of *X/R* as a function of V_{DD} and φ.

voltage slope at the switch turn-on is zero when $\varphi = -0.61$ rad. In this case, the amplifier achieves the optimum operation and the product of the output power P_o and the load resistance R reaches the maximum value.

The average value of the switch voltage is equal to the dc-supply voltage V_{DD}

$$V_{DD} = \frac{1}{2\pi}\int_0^{2\pi} v_s(\theta)d\theta = \frac{1}{2\pi}\int_0^{\pi} V_{bi}[(h(\theta)+1)^2 - 1]d\theta. \tag{23}$$

Solving this equation, one obtains the $\omega C_{j0}R$ as a function of V_{DD} and φ. Equation (23) has two solutions. One solution is not suitable for this circuit because $\omega C_{j0}R$ is negative when $-\pi/2 < \varphi < -0.1$. The other solution of (23) for $\omega C_{j0}R$ is obtained as

$$\omega C_{j0}R = \frac{9\cos(\varphi)}{(9\pi^2-8)} \times \left\langle \begin{array}{l} 4\pi^2 V_{DD}\,(27\pi^4 - 198\pi^2 + 152) + \pi^2\, V_{DD}\,\cos(2\varphi) \\ \times(27\pi^4 - 648\pi^2 + 544) + 4\,(9\pi^2-8)^2\sin^2(\varphi) \end{array} \right\rangle^{0.5} - \frac{2\sin(2\varphi)}{(9\pi^2-8)}. \tag{24}$$

The variation of $\omega C_{j0}R$ as a function of V_{DD} and φ is shown in Fig. 5. The maximum value is obtained when V_{DD} is increased. On the other hand, when $V_{DD} = 100$ V and $\varphi = -0.83$, the maximum value for $\omega C_{j0}R$ is obtained. As can be seen from Fig. 1, the voltage across the reactance L_x is expressed as

$$v_{Lx} = \omega L_x \frac{di_o}{dt} = \omega L_x I_M \cos(\theta+\varphi) = \frac{\omega L_x V_M}{R}\cos(\theta+\varphi) \quad \text{for } 0 < \theta < 2\pi. \tag{25}$$

The voltage across the resonant circuit for $0 < \theta < 2\pi$ is

$$v_{s1}(\theta) = v_o(\theta) + v_{Lx}(\theta) = V_M\sin(\theta+\varphi) + \frac{\omega L_x V_M}{R}\cos(\theta+\varphi) = V_1\sin(\theta+\varphi_1) \tag{26}$$

where V_1 is the amplitude of v_{s1} and is expressed as

$$V_1 = V_M\sqrt{1+\left(\frac{\omega L_x}{R}\right)^2} \tag{27}$$

and φ_1 is

$$\varphi_1 = \varphi + \tan^{-1}\left(\frac{\omega L_x}{R}\right). \tag{28}$$

The output voltage of the resonant circuit v_{s1} has only the fundamental frequency component of the switch voltage v_s. Therefore

$$\frac{1}{\pi}\int_0^{2\pi} v_s(\theta)\cos(\theta+\varphi_1)d\theta = 0. \tag{29}$$

From (29), we obtain

$$\tan\varphi_1 = \frac{\int_0^{\pi} v_s(\theta)\cos(\theta)d\theta}{\int_0^{\pi} v_s(\theta)\sin(\theta)d\theta} = \frac{\int_0^{\pi} V_{bi}[(h(\theta)+1)^2-1]\cos(\theta)d\theta}{\int_0^{\pi} V_{bi}[(h(\theta)+1)^2-1]\sin(\theta)d\theta} \tag{30}$$

from (28), the reactance L_x is given by

$$L_x\omega = X = R\tan(\varphi_1 - \varphi). \tag{31}$$

In Fig. 6, X/R as a function of φ and V_{DD} is shown. It can be seen that the variation of V_{DD} cause a little change in *X/R*, but this ratio decreased when φ increased.

From the definition of the loaded quality factor Q, L is obtained as

$$L = \frac{RQ}{\omega}. \tag{32}$$

From (31) and (32), the inductor L_r is

$$L_r = L - L_x = \frac{R}{\omega}[Q - \tan(\varphi_1 - \varphi)]. \tag{33}$$

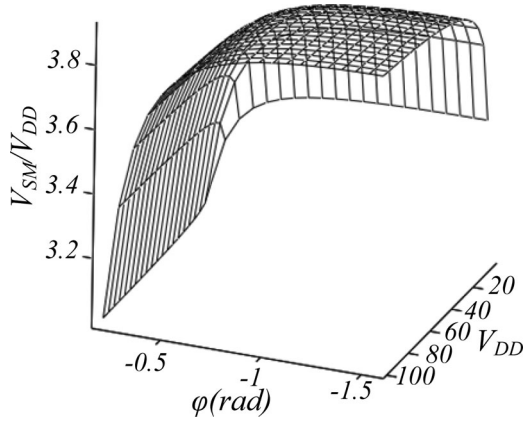

Fig. 7. Variation of V_{SM}/V_{DD} as a function of V_{DD} and φ.

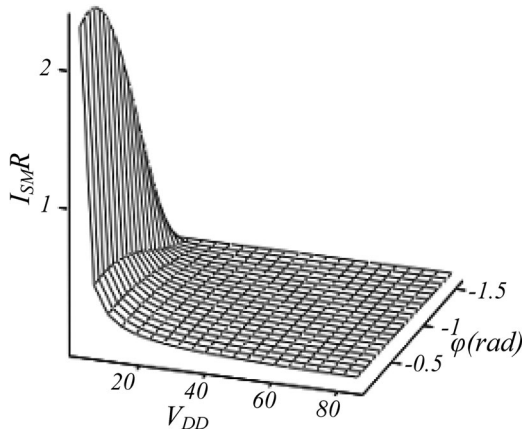

Fig. 8. Variation of $I_{SM}R$ as a function of V_{DD} and φ.

The resonant capacitor is obtained as

$$C = \frac{1}{\omega^2 L_r} = \frac{1}{\omega R[Q - \tan(\varphi_1 - \varphi)]}. \quad (34)$$

III. Output Power Capability

The definition of output power capability C_p is

$$C_p = \frac{V_{DD} I_{DD}}{|V_{s\max}|I_{s\max}||} = \frac{1}{\frac{|V_{s\max}|}{V_{DD}}\frac{|I_{s\max}|}{I_{DD}}} \quad (35)$$

where $V_{s\max}$ and $I_{s\max}$ are the peak value of voltage and current at the MOSFET. The peak switch voltage appears in the range of $0 < \theta < \pi$. Therefore, we have

$$\frac{|V_{s\max}|}{V_{DD}} = \frac{|v_s(\theta_{\max})|}{V_{DD}} = \frac{V_{bi}}{V_{DD}}[(h(\theta_{\max})+1)^2 - 1]. \quad (36)$$

In the peak value of the voltage, the derivative value of the switch voltage is zero. So, from (6) and (8) for $n = 3$, we obtained

$$I_{DD} - I_3 \sin(3\,\theta_{\max}) - I_M \sin(\theta_{\max} + \varphi) = 0. \quad (37)$$

By substituting (13), (18), and (20) into (37), we have

$$1 - \left(\frac{4}{3\pi}\right)\sin(3\theta_{\max}) + \frac{9\pi^2 - 8}{18\pi}\sin(\theta_{\max} + \phi) = 0. \quad (38)$$

Fig. 7 shows the ratio V_{SMAX}/V_{DD} as a function of φ and V_{DD}. This ratio increases from 3.5 to about 3.8 as V_{DD} increases from 0 to 100 V. On the other hand, the peak switch current appears during the on-state. So, we have

$$\frac{I_{SMAX}}{I_{DD}} = 1 - \frac{I_3}{I_{DD}}\sin(3\theta) - \frac{I_M}{I_{DD}}\sin(\theta + \varphi). \quad (39)$$

The normalized switch current I_{SMAX}/I_{DD} is function of φ. Fig. 8 shows normalized maximum switch current $I_{SM}R$ as a function of φ. It can be seen that the normalized maximum switch current $I_{SM}R$ increase as φ increases from -1.57 to -0.61 rad. Fig. 9 shows the output power capability C_p as a function of φ and V_{DD}. It can be seen that C_p increases as φ increases. The other parameter to evaluate the amplifier performance is maximum operating frequency. This parameter causes the limitation on all the parameters of the power amplifier.

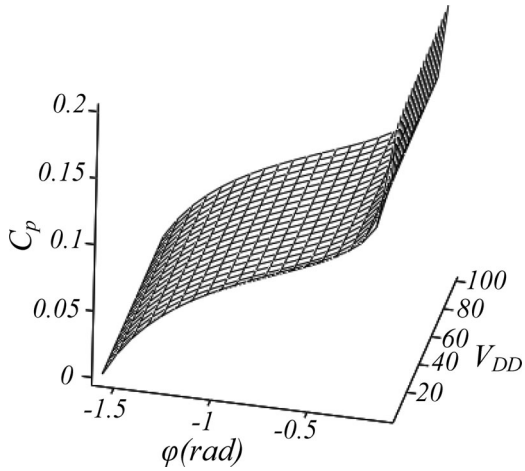

Fig. 9. Variation of C_p as a function of V_{DD} and φ.

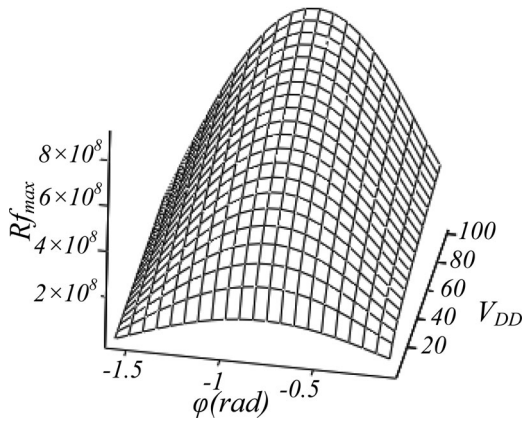

Fig. 10. Variation of $Rf_{\max}$ as a function of V_{DD} and φ.

As can be seen from Fig. 10, the maximum operating frequency increases as V_{DD} increases. On the other hand, it is increased as φ increase up to –0.61 rad and decreased from –0.61 up to –0.1 rad.

TABLE I
THE VALUES OF THE ELEMENTS FOR THE NONOPTIMUM DESIGN EXAMPLE

	Before optimization	After optimization
$R(\Omega)$	54.58	54.58
$L_3(\mu H)$	14	14.1
$C_3(pF)$	12.56	11.86
$L(\mu H)$	21.72	21.72
$C(pF)$	78.96	78.96
$L_{RFC}(\mu H)$	30	30

IV. DESIGN EXAMPLE

A. Design Peocessure

The design specifications for the amplifiers are $f = 4$ MHz, $V_{DD} = 25$ V, $P_{\rm out} = 10.7$ W, $V_{SM} = 98$ V, $Q = 10$, *and* $D = 0.5$.

From (36), we have $\varphi = -0.21$ rad. From (24), R is calculated as 54.58 Ω. From (32), L is obtained 21.72 μH. From (31), we obtained $L_x = 1.68$ μH. From (33), $L_r = 20.05$ μH. From (34), the resonant capacitor is obtained $C = 78.96$ pF. The series resonant circuit C_3–L_3 has the effect on shaping the transistor current and voltage waveforms. The initial value for resonant circuit C_3–L_3 is obtained as: $L_3 = 14$ μH and $C_3 = 12.56$ pF. The practical transistor is not an ideal switch, so an optimization process should be done. The parameters before and after optimization is shown in Table I. The inductance of the RF choke was selected as $L_f = 30$ μH. From (45), $I_{SMAX} = 0.62$ A could be obtained. From (23), we obtained $I_{DD} = 0.42$ A.

B. Simulation and Experimental Results

The theoretical results have been verified experimentally using the circuit of Class E/F$_3$ in Fig. 11(a). The photograph of the fabricated power amplifier is shown in Fig. 11(b). In the PSpice simulation, the device model of IRF510 from the vendor's website [26] is used. It is driven by the gate-driver IC 1XDN414P, its dc supply passes through two parallel capacitors 100 μF and 10 nF. The transistor is mounted directly to a backside aluminum heatsink. The equivalent series resistance (ESR) values of passive elements were measured by a HP-4284A, and the on resistance of the IRF510 was obtained from PSpice model.

The following results were obtained: $L_{\rm RFC} = 30$ μH (ferrite core inductor with air gap), $RL_{\rm RFC} = 0.2$ Ω (dc parasitic resistance), $C_3 = 11.89$ pF (silver mica capacitors), $L_3 = 14.1$ μH (ferrite core inductor with air gap), $RL_3 = 0.116$ Ω (parasitic resistance at 12 MHz) $C = 78.96$ pF (silver mica capacitors), $L = 21.72$ μH (ferrite core inductor with air gap), $RL = 44.67$ mΩ (parasitic resistance measured at 4 MHz), and $R = 54.7$ Ω (resistance of load network). The power losses of all capacitors were negligible. A Tektronix TDS3014B digital oscilloscope was used for recording voltage waveform. The output power $P_{\rm Out}$ can be obtained based on the dc power P_{DC}, the transistor losses P_T, the supply current I_{DC}, the currents IC_3 and $I_{\rm Out}$, and the parasitic resistances $RL_{\rm RFC}$, RL, and RL_3.

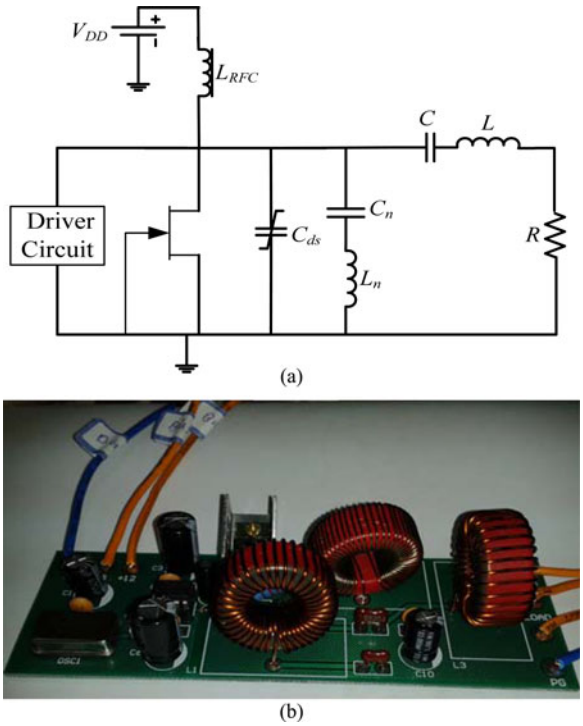

Fig. 11. (a) Class E/F$_3$ power amplifier used for the nonoptimum operation. (b) The photograph of the fabricated power amplifier.

TABLE II
THE VALUES OF THE ELEMENTS AND POWER RELATION FOR THE DESIGN EXAMPLE AT NONOPTIMUM CONDITION

	Theoretical	Simulated	Measured
$R(\Omega)$	54.58	54.58	54.7
D	0.5	0.5	0.5
$V_{DD}(V)$	25	25	25
$f(MHz)$	4	4	4
$V_{SM}(V)$	98	92	91.2
$I_{SM}(A)$	2.51	2.5	2.5
$V_o(V)$	34	33	33
$I_o(mA)$	620	620	620
$L(\mu H)$	21.72	21.72	21.7
$C(pF)$	78.96	78.96	79
$L_3(\mu H)$	14	14.1	14.1
$C_3(pF)$	12.56	11.86	12
$L_{RFC}(\mu H)$	30	30	30
$P_o(W)$	10.7	10.3	10
$P_{in}(mW)$	-	-	31
$G(dB)$	-	-	25.38
$THD(\%)$	0.00	4.25	4.35
$\eta(\%)$	100	95.93	93.45

The output power is obtained as

$$P_{\rm Out} = P_{\rm DC} - P_{L3} - P_L - P_T = 10.7\,{\rm W} - 0.02\,{\rm W} - 0.5\,{\rm W} - 0.282\,{\rm W} = 10\,{\rm W}.$$

The power gain is obtained as

$$G = 10\log_{10}\left(\frac{P_o}{P_{\rm in}}\right) \tag{40}$$

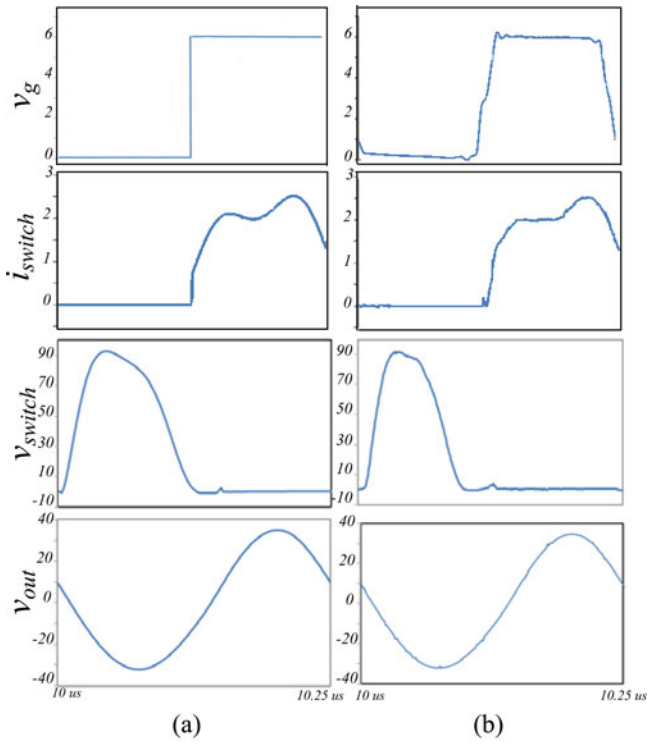

Fig. 12. Waveforms obtained from (a) the PSpice Simulation, and (b) the experimental results for the nonoptimum operation.

where $P_{\rm in}$ and $P_{\rm out}$ are the input and output power, respectively. Also, the total harmonic distortion (THD) is

$$\text{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} V_{\rm on}^2}}{V_{o1}} \tag{41}$$

where $V_{\rm on}$ is a root-mean-square value of the nth harmonic in the output voltage v_o. The measured values of the power gain and THD are 25.38 dB and 4.35%, respectively. The value of the elements, and all the powers are shown in Table II. The waveform obtained from Pspice and measured results are shown in Fig. 12(a) and (b), respectively.

V. Conclusion

This paper has introduced analytical expressions of the Class-E/F$_3$ power amplifier with shunt capacitance for the nonoptimum operation. The design values for achieving the nonoptimum condition are expressed as a function of the phase shift between the input and output voltage and dc-supply voltage. The Class-E/F$_3$ amplifier with nonoptimum condition increases one design degree of freedom. Because of the increase in the design degree of freedom, peak switch voltage and current can be specified as a design specification. This paper has given the circuit design example based on our proposed design expression by specifying the peak switch voltage. The measurement and PSpice simulation results are in agreement with the analytical expressions quantitatively, which show the validity of our analytical expressions. In the circuit simulation and experiments, the Class-E/F$_3$ ZVS amplifier achieves 95.93% and 93.45% power conversion efficiency at 4 MHz and output power 10.3 and 10 W, respectively. We will address the analysis of the Class-E/F$_n$ amplifier for any n with nonlinear shunt capacitance in the future works.

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Mohsen Hayati received the B.E. degree in electronics and communication engineering from Nagarjuna University, Guntur, India, in 1985, and the M.E. and Ph.D. degrees in electronics engineering from Delhi University, Delhi, India, in 1987 and 1992, respectively.

He joined the Department of Electrical Engineering, Razi University, Kermanshah, Iran, as an Assistant Professor in 1993, and currently, as an Associate Professor. He has published more than 140 papers in international and domestic journals and conferences. His current research interests include microwave and millimeter wave devices and circuits, application of computational intelligence, artificial neural networks, fuzzy systems, neuro-fuzzy systems, electronic circuit synthesis, and modeling and simulations.

Akram Sheikhi received the B.E. degree from Shariaty University, Tehran, Iran, in 2007, and the M.Sc. degree in electronics engineering from the Department of Electrical Engineering, Razi University, Kermanshah, Iran, in 2010. She is currently working toward the Ph.D. degree in electronics engineering in the Razi University,.

Her research interests include microwave filter, high-frequency high-efficiency switching mixed-mode power amplifiers, and numerical analysis of nonlinear circuits.

Andrei Grebennikov (M'99−SM'04) received the Dipl. Eng. degree in radio electronics from Moscow Institute of Physics and Technology, Moscow, Russia, in 1980, and the Ph.D. degree in radio engineering from Moscow Technical University of Communications and Informatics, Moscow, Russia, in 1991.

He obtained a long-term academic and industrial experience working with the Moscow Technical University of Communications and Informatics; the Institute of Microelectronics, Singapore; M/A-COM, Cork, Ireland; Infineon Technologies, Munich, Germany, and Linz, Austria; and Bell Labs, Alcatel-Lucent, Dublin, Ireland, as an Engineer, Researcher, Lecturer, and Educator. He has lectured as a Guest Professor with the University of Linz, Linz, Austria, and presented short courses and tutorials as an Invited Speaker at the IEEE Microwave Theory and Techniques Society (MTT-S) International Microwave Symposia (IMS), European and Asia-Pacific Microwave Conferences, the Institute of Microelectronics, Singapore, Motorola Design Centre, Penang, Malaysia, the Tomsk State University of Control Systems and Radio electronics, Tomsk, Russia, and the Aachen Technical University, Aachen, Germany. He is an author and coauthor of more than 100 papers, holds 30 European and US patents and patent applications, and authored six books dedicated to RF and microwave circuit design.