Decoupled Control of Modular Multilevel Converters Using Voltage Correcting Modules

Baljit S. Riar, *Student Member, IEEE*, and Udaya K. Madawala, *Senior Member, IEEE*

***Abstract*—Historically, cascaded H-bridge, capacitor-clamped, and neutral point-clamped topologies have been used for medium- to high-voltage applications but the modular multilevel converter (M2LC) is becoming a popular alternative. However, in comparison to other topologies, control of the load current, which is inherently coupled with circulating currents, is more difficult in the M2LC topology. This paper proposes a modified M2LC topology that allows for decoupled control of circulating currents from the load current. Each arm of the modified topology comprises a plurality of half-bridge modules and one full-bridge module. The full-bridge module minimizes harmonic currents within the converter without affecting the load current. A state-space model, which is generalized per arm with an N number of half-bridge modules and one full-bridge module, is presented to accurately predict the behavior of the proposed topology. Theoretical as well as experimental results of a single-phase three-level 800-VA prototype converter are presented with a discussion to demonstrate the viability of both the proposed mathematical model and modified topology. A comparative investigation with respect to a conventional topology reveals that the proposed topology offers superior performance.**

***Index Terms*—Circulating currents, decoupled control, high-voltage direct current (HVDC), modular multilevel converter (M2LC), voltage balancing, voltage correcting module (VCM).**

I. Introduction

MODULAR multilevel converter (M2LC) topology, which features modularity, scalability, reduced voltage rating of the switches, and redundant switching operations, has recently become popular in medium- to high-voltage applications [1], [3]. A number of advantages associated with these features make M2LC suitable for a variety of applications, such as high-voltage direct current transmission [4], [5], motor drives [6], traction motors, [7] and static synchronous compensator [8].

There are, however, disadvantages associated with the topology, which include the need for both balancing capacitor voltages and controlling circulating currents, and the increased complexity of the overall control scheme [9]. Sorting algorithms, which are based on the polarity of the arm current, have commonly been used to balance the capacitor voltages [1]. Circulating currents are inherent to the M2LC topology and manifest from the variations in capacitor voltages and in combination with the modulation scheme [2], [10]. These currents do not affect the load current, but cause variations in capacitor voltages while increasing the converter losses.

Various methods, both hardware and control based, have been proposed to minimize circulating currents. In [11], each phase-leg incorporates a filter that is tuned to block second harmonic of the circulating current. In situations where the number of modules is increased without changing the number of voltage levels, active redundancies of the modules have been used to reduce the capacitor voltage variations and circulating currents [12]. In [13], capacitor voltages have been maintained within tight bounds around the nominal value to control the circulating currents. Model predictive direct current control scheme has also been adopted to control the currents [14], [15]. In contrast, circulating currents have been minimized by employing cascaded control loops, during which the modulation index of each arm or module is modified [6], [16]–[19]. Furthermore, currents can also be minimized by adding a common-mode voltage term to the reference of the arm voltages [20], [21].

This paper presents a M2LC topology that employs voltage correcting modules (M2LC-VCMs), as shown in Fig. 1, to minimize circulating currents while reducing the complexity of control. In the proposed topology, one full-bridge VCM, which has a lower voltage rating than a half-bridge module is included in each arm of the converter to minimize circulating currents [3]. The VCM can be considered as an active filter, which minimizes harmonic currents within the converter. The M2LC-VCM allows for decoupled control of load and circulating currents, where the load current is controlled by the half-bridge modules and the circulating current is controlled by the full-bridge modules. A generalized state-space model is presented to accurately characterize the dynamic behavior of the proposed M2LC-VCM topology. Theoretical results are presented in comparison to experimental results of a single-phase three-level 800-VA prototype M2LC converter to demonstrate the accuracy of the model and validate the proposed decoupled control philosophy. Results clearly indicate that the circulating currents can significantly be reduced even when the switching frequency is equal to the fundamental frequency of the load current.

II. Proposed M2LC with VCMs (M2LC-VCMs)

A. Configuration

Fig. 1 shows the proposed M2LC-VCM topology. Each arm consists of N half-bridge modules, which are represented as

Manuscript received December 22, 2013; revised February 12, 2014; accepted March 13, 2014. Date of publication March 25, 2014; date of current version October 7, 2014. This work was supported by the University of Auckland Doctoral Scholarship. Recommended for publication by Associate Editor F. Gao.

The authors are with the Department of Electrical and Computer Engineering, University of Auckland, 1052 Auckland, New Zealand (e-mail: bria001@aucklanduni.ac.nz; u.madawala@auckland.ac.nz).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2014.2313613

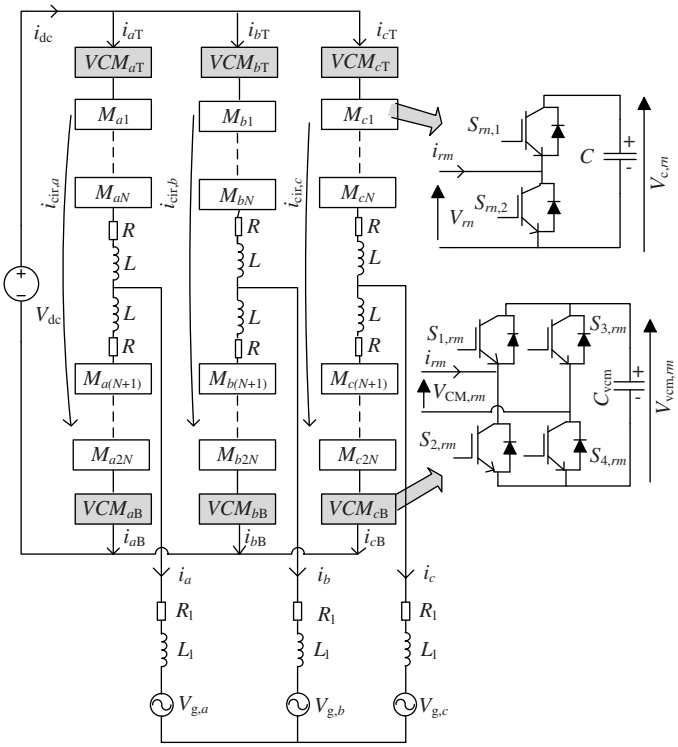


Fig. 1. Proposed topology (M2LC-VCM).

$M_{rn}, r \in \{a, b, c\}, n \in \{1, 2, \ldots 2N\}$, a resistor, R, that models conduction losses, and an arm inductor, L. The individual half-bridge module has two switching states $u_{rn} \in \{0, 1\}$. State 1 corresponds to switch $S_{rn,1}$ being on, connecting the capacitor in the circuit. Generally, the M2LC is driven in a manner that N half-bridge modules are connected in series across the dc link and capacitor voltages, $V_{c,rn}$, are balanced around $\frac{V_{dc}}{N}$, which results in at least $2N + 1$ line–line voltage levels. The proposed M2LC-VCM has at least one VCM in each arm to control the circulating currents. The VCM has three switching states $u_{vcm,rm} \in \{-1, 0, 1\}, m \in \{T, B\}$, which are associated with the polarity of the VCM output voltage, $V_{CM,rm}$. Hereafter, the half-bridge modules and full-bridge modules are termed as power-modules and VCMs, respectively.

B. Circulating Currents

The circulating current in a phase-leg is related to arm currents as follows:

$$i_{cir,r} = \frac{i_r\mathrm{T}}{2} + \frac{i_r\mathrm{B}}{2} = \overline{i_{cir,r}} + \sum_{h=1}^{\infty} i_{h,r}. \tag{1}$$

The circulating currents consist of a dc, $\overline{i_{cir,r}}$, and harmonic, $i_{h,r}$, current components [10]. The dc component of the current is in proportion to the power delivered or load current. For a three-phase system, the input and output power are related as follows:

$$V_{dc} i_{dc} = 3 V_{ph} i_{ph} \cos(\phi) \tag{2}$$

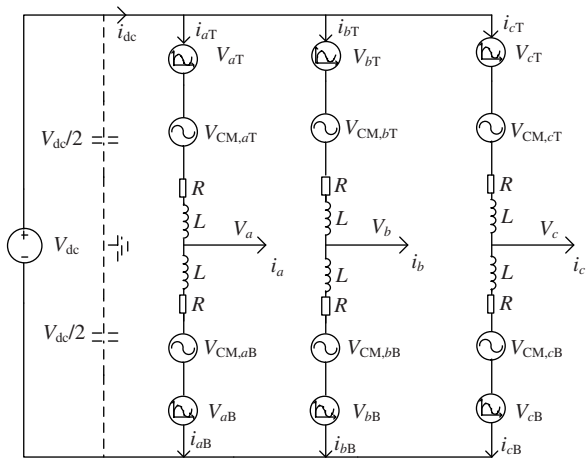


Fig. 2. Equivalent circuit of the M2LC-VCM.

where V_{dc} and i_{dc} are the dc-link voltage and current, respectively. ϕ denotes the phase angle between the phase-voltage, V_{ph}, and phase-current, i_{ph}. If circuit parameters of all the three phase-legs are symmetrical and there is a uniform power flow between them, then the dc value of the circulating current in a phase-leg is given by

$$\overline{i_{cir,r}} = \frac{i_{dc}}{3} = \frac{V_{ph} i_{ph} \cos(\phi)}{V_{dc}}. \tag{3}$$

The harmonic currents are inherent to the M2LC topology and manifest from the variations in capacitor voltages in combination with the modulation scheme [10]. This relationship between the circulating current, modulation scheme, capacitor voltages, and VCMs can be represented mathematically, using the equivalent circuit of the proposed topology in Fig. 2. The power-modules are represented as a controllable voltage source, V_{rm}, given as follows:

$$V_r\mathrm{T} = \sum_{n=1}^{N} u_{rn} V_{c,rn} \tag{4}$$

$$V_r\mathrm{B} = \sum_{n=N+1}^{2N} u_{rn} V_{c,rn}. \tag{5}$$

VCMs are represented as $V_{CM,rm}$ in the equivalent circuit and the mid-point of the dc-link voltage is used as the reference voltage. The output voltage of the converter, V_r, arm current, i_{rm}, and the voltages of the VCMs, $V_{CM,rm}$, and power-modules, V_{rm}, can be related as follows:

$$\frac{V_{dc}}{2} - V_r\mathrm{T} - V_{CM,r}\mathrm{T} - V_r = R i_r\mathrm{T} + L\frac{\mathrm{d}i_r\mathrm{T}}{\mathrm{d}t} \tag{6}$$

$$\frac{V_{dc}}{2} - V_r\mathrm{B} - V_{CM,r}\mathrm{B} + V_r = R i_r\mathrm{B} + L\frac{\mathrm{d}i_r\mathrm{B}}{\mathrm{d}t}. \tag{7}$$

Adding (6) and (7), and using (1), the relationship between the circulating currents and various voltages in a phase-leg can be established as

$$2L\frac{\mathrm{d}i_{cir,r}}{\mathrm{d}t} + 2R i_{cir,r} = (V_{dc} - V_r\mathrm{T} - V_r\mathrm{B}) - (V_{CM,r}\mathrm{T} + V_{CM,r}\mathrm{B}). \tag{8}$$

It is clear from (8) that harmonics in the circulating currents can be controlled through the voltage that is injected by VCMs, $(V_{\mathrm{CM},r}\mathrm{T} + V_{\mathrm{CM},r}\mathrm{B})$. Subtracting (6) from (7), the output voltage of the converter can be found as

$$V_r = \frac{V_r\mathrm{B} - V_r\mathrm{T}}{2} + \frac{V_{\mathrm{CM},r}\mathrm{B} - V_{\mathrm{CM},r}\mathrm{T}}{2} + \frac{R}{2}\left(i_r\mathrm{B} - i_r\mathrm{T}\right) + \frac{L}{2}\left(\frac{\mathrm{d}i_r\mathrm{B}}{\mathrm{d}t} - \frac{\mathrm{d}i_r\mathrm{T}}{\mathrm{d}t}\right). \quad (9)$$

VCMs have only minor impact on the output voltage due to two reasons. First, as described in the forthcoming section, the magnitude of the voltage inserted by each VCM is smaller than the voltage-step of the output voltage. Second, VCMs are controlled in a manner that the inserted voltages are equal in respective arms. Therefore, the voltage difference, $(V_{\mathrm{CM},r}\mathrm{B} - V_{\mathrm{CM},r}\mathrm{T})/2$, in (9) is almost zero.

III. Mathematical model

The state-space model is derived by using an M2LC-VCM topology with N power-modules and one VCM in an arm. State-variables of the model, where the load is connected in star-configuration, are the arm currents in phases a and b, dc-link current, grid voltages in the alpha/beta coordinate system, and capacitor voltages of the power-modules and VCMs. The state-vector of the model is defined as

$$\boldsymbol{x} = [i_a\mathrm{T}\, i_a\mathrm{B}\, i_b\mathrm{T}\, i_b\mathrm{B}\, i_{\mathrm{dc}} V_{g,\alpha} V_{g,\beta} V_{\mathrm{c},a1} V_{\mathrm{c},a2} \ldots V_{\mathrm{c},c2N} \; V_{\mathrm{vcm},a}\mathrm{T} V_{\mathrm{vcm},a}\mathrm{B} \ldots V_{\mathrm{vcm},c}\mathrm{B}]^{\top}. \quad (10)$$

The input vector is denoted as follows:

$$\boldsymbol{u} = [u_{a1} u_{a2} \ldots u_{c2N}\, u_{\mathrm{vcm},a}\mathrm{T} u_{\mathrm{vcm},a}\mathrm{B} \ldots u_{\mathrm{vcm},c}\mathrm{B}]^{\top} \quad (11)$$

where $u_{rn} \in \{0, 1\}$ is the switching state of a power-module and $u_{\mathrm{vcm},rm} \in \{-1, 0, 1\}$ is the switching state of a VCM.

The complete system can be expressed in the standard state-space form as

$$\frac{\mathrm{d}\boldsymbol{x}}{\mathrm{d}t} = \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}\boldsymbol{u} + \boldsymbol{V}. \quad (12)$$

The definitions of the system matrices $\boldsymbol{A}$, $\boldsymbol{B}$, and $\boldsymbol{V}$ are given in the Appendix.

IV. Decoupled control of the M2LC using VCMs

The control scheme for driving the switches of power-modules and VCMs is split into two concurrent loops, which are labeled as loops 1 and 2 in Fig. 3. The first loop, loop 1, controls the load current and determines a switching pattern to balance the capacitor voltages. Control schemes, such as staircase modulation (SCM) and optimized pulse patterns [16], [22], are appropriate for reducing the switching frequency for a given load current distortion and can also be part of this loop.

The number of power-modules, which are connected in an arm, controls the load-current, whereas selection of these modules balances the capacitor voltages. The capacitor voltages are balanced by using a simple and commonly used method, the sorting algorithm [1]. With this algorithm, all the capacitor voltage measurements are sorted in either ascending or descending order of their voltage magnitudes and the capacitors are selected to be connected or bypassed. For example, for a positive arm current, the capacitors with the lowest voltage are selected first, and conversely, the capacitors with the highest voltage are prioritized for a negative arm current.

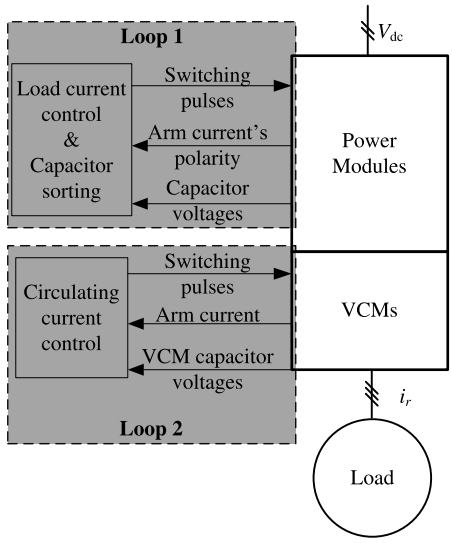


Fig. 3. Block diagram of the decoupled control scheme.

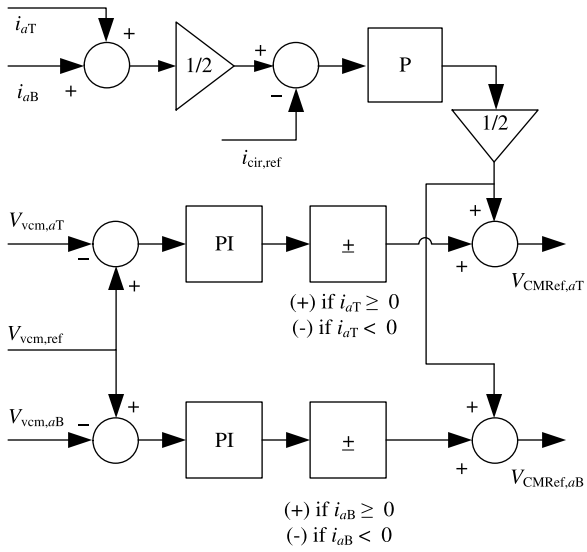


Fig. 4. Control of VCMs in phase-leg a.

The second loop, loop 2, controls the circulating currents by controlling the VCMs. The circulating currents, as given by (1), consist of a number of harmonics, which can be minimized by inserting an appropriate voltage in accordance with (8). The control scheme of the VCMs, as shown in Fig. 4 for phase-leg a, controls the circulating currents and maintains the capacitor voltage of each VCM at its nominal value.

In each phase-leg, the circulating current is compared with a reference, $i_{\mathrm{cir,ref}} = \frac{i_{\mathrm{dc}}}{3}$, and then proportional (P) controller is used to generate a voltage reference of the VCM modules. This

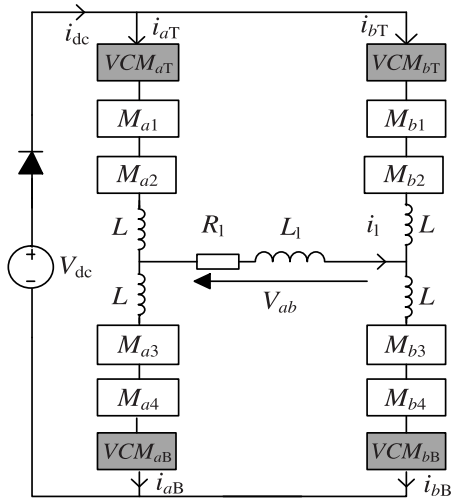
TABLE I
PARAMETERS OF A SINGLE-PHASE M2LC-VCM SETUP

Parameter		SI	p.u.
Output frequency	f	50 Hz	1
Supply voltage	$V_{\rm dc}$	280 V	1.56
Load current	$i_{\rm l}$	4.35 A	0.71
Power-module capacitance	C	1.72 mF	15.82
VCM capacitance	$C_{\rm vcm}$	1.72 mF	15.82
Load resistance	$R_{\rm l}$	40 Ω	1.37
Load inductance	$L_{\rm l}$	30 mH	0.32
Arm inductance	L	1.2 mH	0.01
Number of modules	N	2	

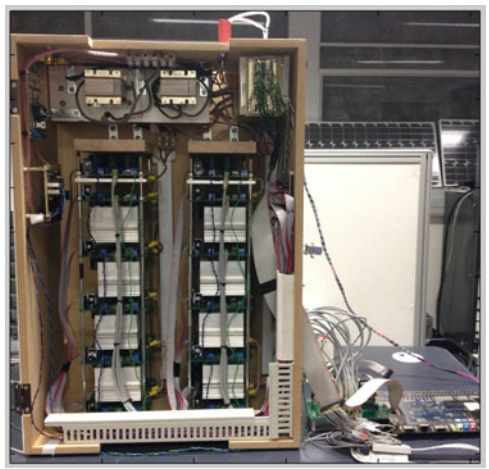
voltage reference is equally divided and added to reference of the top and bottom VCM in a phase-leg to minimize the effect of VCMs on the output voltage (9).

A proportional-integral (PI) controller is used to regulate the capacitor voltage of the VCM module at its nominal value, $V_{\rm vcm,ref}$. The output of the PI controller is multiplied with a sign function that is based on the polarity of the arm current. For a positive arm current, the sign is positive and vice versa. Finally, the voltage references, $V_{\rm CMRef,}{}_{rm}$, are compared against carrier waveforms to generate pulse patterns for switches $S_{1,rm}$–$S_{4,rm}$.

The VCMs do not excessively increase the switching losses even when their switching frequency is higher than the power-modules, because of the lower voltage ratings. With the higher switching frequency, the bandwidth of the circulating current control loop (loop 2) can be much larger than the load current control loop (loop 1). From the control perspective, the modified topology has two main advantages. First, a simple control scheme can be used to control the load current or the output voltage. Second, the control of the circulating current is decoupled from the load current. The load current and circulating currents are controlled by the power-modules and VCMs, respectively. Moreover, the output voltage or the number of the output voltage levels of the converter is not affected as explained before.



(a)



(b)

Fig. 5. Experimental setup of the M2LC. (a) Circuit diagram. (b) Prototype M2LC.

V. RESULTS

A. M2LC-VCM Prototype

In order to verify the viability of the proposed topology, a single-phase three-level 800-VA prototype M2LC was constructed. The experimental setup is shown in Fig. 5 and the circuit parameters of the system are summarized in Table I. Base quantities for the p.u. system are $V_{\rm b} = 180$ V, $I_{\rm b} = \sqrt{2} I_{\rm rat} = 6.15$ A, and $f_{\rm b} = 50$ Hz. The control scheme was implemented on a TMS320F28335 Digital Signal Controller (DSC). The DSC has an on-board analog-to-digital converter (ADC), which was used to measure the arm currents and the capacitor voltages. Altera's DE2 board was used to generate dead-time for the switching signals of modules and to safely shut down the converter in the unlikely event of a fault. IGBT, IKW20N60H3, and MOSFET, IRFP250MPBF are used for switches in the power-modules and VCMs, respectively. The use of MOSFETS also helps to decrease the effect of dead-time. Moreover, methods discussed in [23] can also be used to compensate the effect of dead-time in each switch.

At startup, a resistor was connected in series with the dc-supply to charge the capacitors and it was bypassed during the normal operation of the converter. The diode, as shown in Fig. 5(a), is part of the dc-supply that was used in the experiments. The diode also ensures that the dc-current is unidirectional and this feature is congruent with the six-pulse or 12-pulse diode rectifiers that are commonly used in power converter applications.

B. Performance Evaluation Using PWM Switching of Power-Modules

Three case studies were considered to experimentally evaluate the performance of the proposed topology and its state-space model. Case I evaluates the performance of the conventional topology, which is used to benchmark the performance of the other cases. In Case I, the VCMs as shown in Fig. 5(a) were bypassed during the experiments. Case II evaluates the performance of the proposed topology. The mathematical model, as presented in Section III, was modified to characterize the

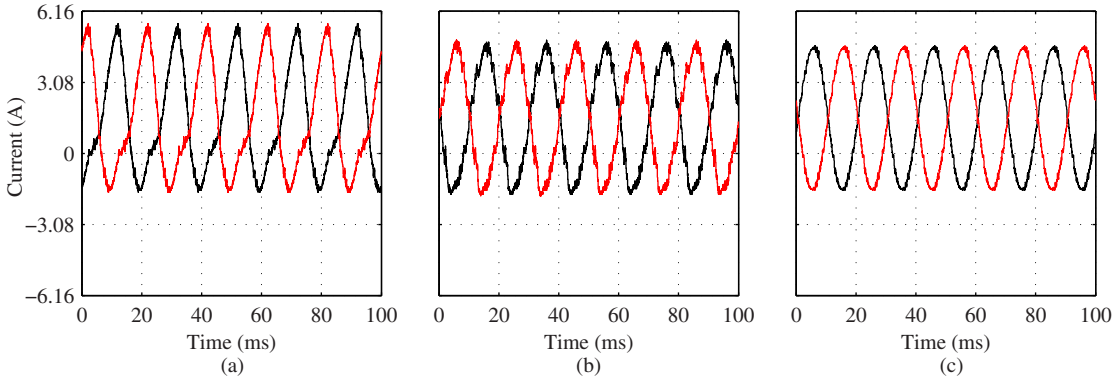


Fig. 6. Arm currents in phase-leg a using PWM. (a) Case I. (b) Case II. (c) Case III.

behavior of the single-phase M2LC-VCM, as shown in Fig. 5(a). Case III was formed to investigate the viability of the modified model.

In all cases, pulse patterns of the power-modules were computed offline by comparing a sinusoidal reference with carrier waveforms in phase-disposition. The resulting pulse-width modulation (PWM) based patterns were stored in a look up table and used for controlling power-modules. With all the cases, the system was operated at its rated conditions as given in Table I. The sorting algorithm, as explained in the previous section, was used in all the cases to balance the capacitor voltages. The switching frequency of the power-modules in these three cases was approximately 380 Hz. The control scheme, as described in Section IV, was used to control the VCMs, and switching frequency of the VCMs was 2 kHz.

Fig. 6 shows the waveforms of the arm currents in phase-leg a. In Case I, the second harmonic of the arm current prevails because of a lack of circulating current control. The VCMs reduce the second harmonic of the arm current with the proposed topology, i.e., Cases II and III. Relative to Case I, the rms arm current is reduced by 3% in Cases II and III. Both analytical (Case III) and experimental (Case II) waveforms are similar and confirm the validity of the mathematical model.

Fig. 7 shows the waveforms of the dc-link current to demonstrate that the ripple in the dc-link current or the harmonic circulating currents are significantly reduced with the proposed topology. In comparison to Case I, the magnitude of the current ripple is reduced by 65% and 82.5% in Cases II and III, respectively. It is evident that the VCMs minimize the harmonic circulating currents within the converter.

Fig. 8 shows that capacitor voltages of the power-modules are balanced around their nominal value. The average of the capacitor voltages, which is slightly lower than $V_{\rm dc}/2 = 140$ V is due to the voltage drop across the various resistors within the converter. Nonetheless, the waveforms in these cases show a similar trend.

Capacitor voltages of the VCMs, as shown in Fig. 9, are balanced around an average value of 6 V, which is about 5% of the voltage across the power-modules. Both analytical and experimental waveforms are similar.

Overall, experimental and analytical results are in good agreement both in values and trend, thus validating the accuracy of the model. The small discrepancy in the waveforms is due to a number of factors, such as the model does not consider delays associated with the ADCs and filters. Moreover, the resistive elements that were considered in the model, as constant losses, were all estimated values and also add to the slight discrepancy in the waveforms.

C. Performance Evaluation Using SCM Switching of Power-Modules

The SCM method was used to evaluate the performance of the converter at a lower switching frequency of the power-modules. With this method, the pulse patterns that eliminate the fifth harmonic of the output voltage waveform were generated as described in [23] and used to control power-modules. The experiments were conducted using circuit parameters listed in Table I. In addition, the dc-link voltage, $V_{\rm dc}$, was reduced to 268 V so that the converter delivers the rated load current with the given patterns. The sorting algorithm was used to balance the capacitor voltages and the control scheme, as described in Section IV, was used to control the VCMs. The switching frequency of the power-modules and VCMs was 50 Hz and 2 kHz, respectively.

Experimental waveforms of the arm and dc-link currents using SCM are shown in Figs. 10 and 11, respectively. The rms arm current reduces by 2% relative to the conventional topology. In comparison to the conventional topology, the magnitude of the dc-link current, as shown in Fig. 11, is reduced by 58%. These results clearly demonstrate that the circulating currents can be reduced even at a lower switching frequency of power-modules.

It can be seen from Figs. 8 and 12 that the reduced switching frequency of the power-modules, however, increases the voltage variations of the capacitor voltages.

VI. Improvement in Performance—Altering Parameters

The state-space model, which is proven to accurately describe the behavior of the converter, is further used to evaluate the performance of a grid-connected three-phase M2LC-VCM. Each arm of the three-phase converter comprises four power-modules and one VCM. The circulating currents or voltage-discrepancy in a phase-leg is a function of circuit parameters [10]. Therefore,

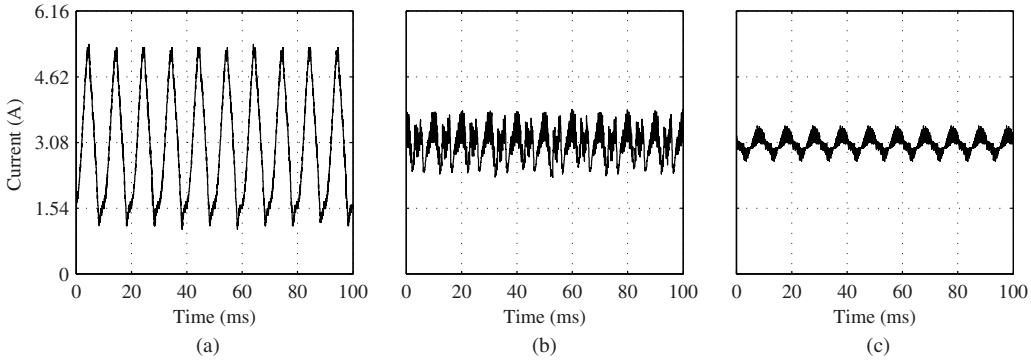


Fig. 7. DC-link current using PWM. (a) Case I. (b) Case II. (c) Case III.

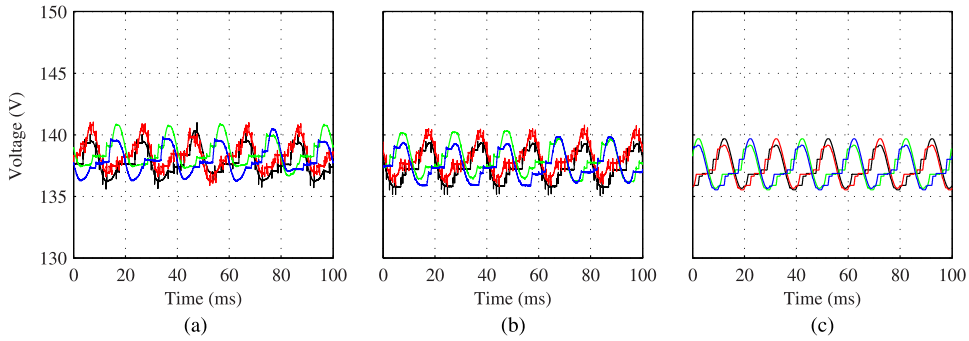


Fig. 8. Capacitor voltages of power-modules in phase-leg a using PWM. (a) Case I. (b) Case II. (c) Case III.

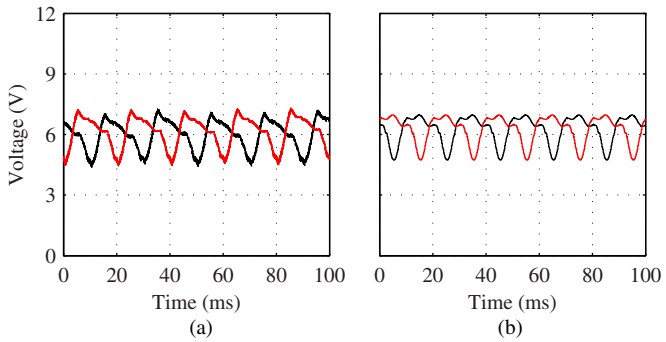


Fig. 9. Capacitor voltages of VCMs in phase-leg a using PWM. (a) Case II. (b) Case III.

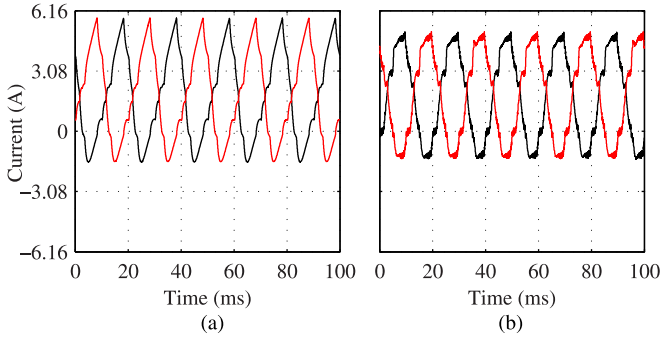


Fig. 10. Arm currents in phase-leg a using SCM. (a) Conventional. (b) Proposed.

the parameters, which result in an increased voltage discrepancy, were selected to investigate the performance of the proposed topology. The parameters of the system are summarized in Table II using $V_{\rm b} = \sqrt{2/3}V_{ll} = 2449.49$ V, $I_{\rm b} = \sqrt{2}I_{\rm rat} = 516.19$ A, and $f_{\rm b} = 50$ Hz as base quantities for the p.u. system.

A vector control (VC) scheme with PWM, where carrier waveforms at 750 Hz were in phase disposition, was used to control the rated load current at unity power factor. The capacitor voltages were balanced by using the aforementioned sorting algorithm. The VCMs were controlled using the scheme which is described in Section IV and switching frequency of the VCMs was 600 Hz. In addition, the average voltage of the VCM capacitors was 3.85% of the dc-link voltage. In the following discussion, the performance of the M2LC-VCM is compared against the conventional M2LC topology that was also controlled using the VC scheme.

TABLE II
PARAMETERS OF A THREE-PHASE M2LC-VCM SETUP

Parameter		SI	p.u.
Output frequency	f	50 Hz	1
Supply voltage	$V_{\rm dc}$	5.2 kV	2.12
Grid voltage	V_{ll}	3 kV	1.22
Load current	i_r	365 A	0.71
Power-module capacitance	C	5 mF	7.45
VCM capacitance	$C_{\rm vcm}$	5 mF	7.45
Load inductance	$L_{\rm l}$	5.23 mH	0.35
Arm inductance	L	1.5 mH	0.09
Number of modules	N	4	

Fig. 13 shows the waveforms of the arm currents in phase a and the dc-link current with the conventional and proposed

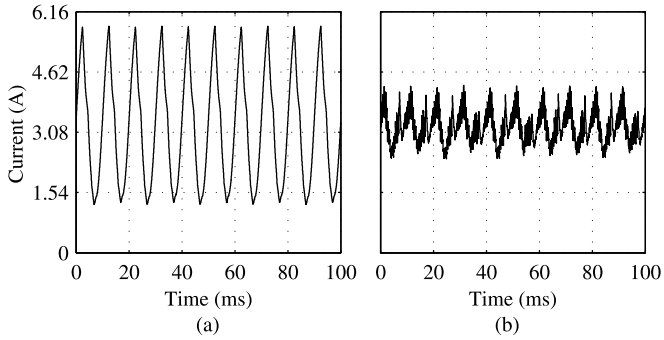


Fig. 11. DC-link current using SCM. (a) Conventional. (b) Proposed.

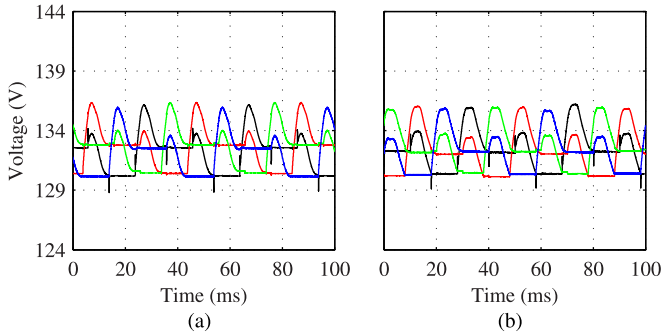


Fig. 12. Capacitor voltages of power-modules in phase-leg a using SCM. (a) Conventional. (b) Proposed.

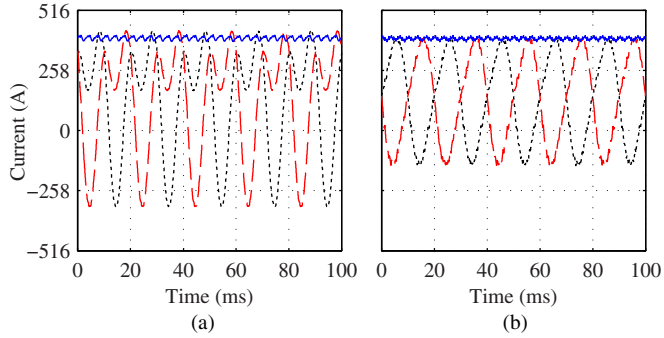


Fig. 13. DC-link current (solid line) and arm currents in phase-leg a (dashed and dotted lines). (a) Conventional. (b) Proposed.

topology. The rms arm current reduces by more than 16% relative to the conventional topology. The average dc-link current is unaffected in both the cases, however, the ripple of the dc-link current is slightly reduced with the proposed topology.

The arm current spectrum is shown in Fig. 14. As expected, the second harmonic of the arm and, thus the circulating current, is significantly reduced with the proposed topology. As can be seen from Fig. 14, the fundamental and dc components of the arm current are not changed which means that the VCMs do not affect the load or the dc-link current. The control scheme, as presented in Section IV, uses a proportional regulator for controlling the circulating currents. It is evident from Fig. 14 that the proportional regulator is unable to suppress all the harmonic currents. However, this inherent limitation of the proportional regulator can be overcome by using proportional-resonant regulator or by the PI scheme as described in [3].

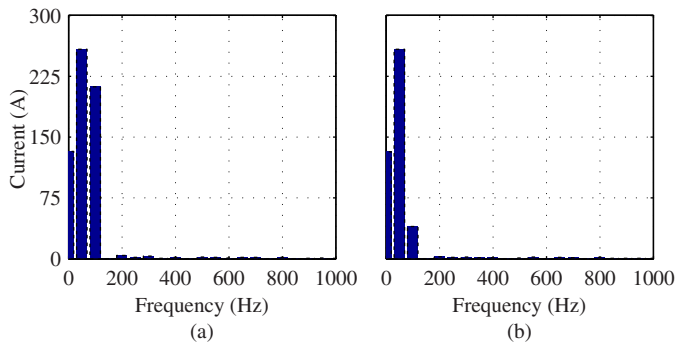


Fig. 14. Arm current spectrum. (a) Conventional. (b) Proposed.

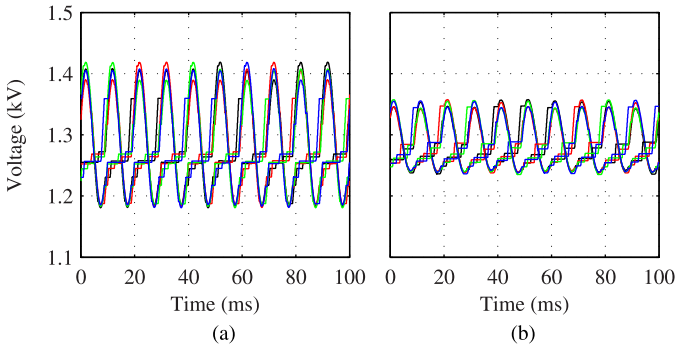


Fig. 15. Power-module capacitor voltages in phase-leg a. (a) Conventional. (b) Proposed.

Fig. 15 shows the waveforms of the capacitor voltages that are balanced around their nominal value. With the proposed topology, the variation in the capacitor voltages is approximately 9% of the average value, which is one-half of the variation with the conventional topology.

In general, the rms arm current is a function of the load current and circuit parameters [10]. With the choice of circuit parameters, the ratio of the rms arm current and load current with the three-phase setup is greater than the single-phase setup. VCMs of the three-phase setup, therefore, allow for further improvements in the performance. Moreover, the results also show that the improvement in the performance of the three-phase M2LC-VCM is greater than the single-phase M2LC-VCM.

VII. Discussion

The circulating currents, which are driven by a small voltage difference in a phase-leg, can be reduced by increasing the size of passive components such as arm inductance, resistance, or capacitance of the power-module [10]. Increasing the arm resistance, however, will reduce the efficiency of the converter. Increasing the capacitance, where the voltage rating of the capacitor is equal to the step size of the output voltage, could increase the monetary cost and footprint of the converter. Similarly, inductors, which are designed to operate in the low-frequency range, are bulky and increase the footprint of the converter. As presented in this paper, the circulating currents can also be reduced by the VCMs in a phase-leg. The VCM is

an active filter and, unlike the passive components, can adapt rapidly to the varying operating conditions of the converter.

Dimensioning of the VCM modules can be performed after selecting the capacitance of the power-modules and the arm inductance, where the latter can be selected using the guidelines, such as [24] and [25]. The voltage rating of the VCM switches is equal to the average voltage of the VCM capacitors and the voltage is primarily governed by the voltage discrepancy in a phase-leg (8). This discrepancy or the average voltage, which is a function of the circuit parameters, can be determined using the state-space model. Consequently, circulating currents can only be suppressed if the average voltage of the VCM capacitor is sufficient to minimize the voltage discrepancy.

Because the arm current flows through the VCM switches, the current rating of the VCM switches is the same as that of the power-modules. Moreover, variation in the VCM capacitor voltages is a function of the VCM capacitance and arm currents. The capacitance, which yields an appropriate voltage variation, can also be determined using the model.

The switching frequency of the VCM depends on the frequency of the harmonic currents to be minimized. Typically, frequencies of the most dominant harmonics are 100 Hz (second harmonic) and 200 Hz (fourth harmonic). Therefore, the switching frequency for which VCMs yield an appropriate performance can also be selected using the model. At present, no effort has been made to optimize the performance of the converter and the chosen frequency of 2 kHz is not an optimal selection.

VIII. Conclusion

A modular multilevel converter with voltage correcting modules, M2LC-VCM, has been proposed to decouple and simplify the control of the load and circulating currents. The circulating currents are controlled by a full-bridge module which is included in each arm of the converter. A mathematical model has been formulated and used for investigating the performance of the proposed topology. Validity of the proposed concept has been verified both analytically and experimentally using a single-phase three-level 800-VA prototype M2LC-VCM. The experimental results have shown that the M2LC-VCM achieves an appropriate control of the circulating currents even at a lower switching frequency of the half-bridge modules.

Appendix

The matrices and vectors of the state-space model (12) are given as follows:

$$\boldsymbol{A} = \begin{bmatrix} \boldsymbol{T}_1 & \boldsymbol{0}_{7\times 6N} & \boldsymbol{0}_{7\times 6} \\ \boldsymbol{0}_{6N\times 7} & \boldsymbol{I}_{6N} & \boldsymbol{0}_{6N\times 6} \\ \boldsymbol{0}_{6\times 7} & \boldsymbol{0}_{6\times 6N} & \boldsymbol{I}_6 \end{bmatrix}^{-1} \begin{bmatrix} \boldsymbol{F}_1 & \boldsymbol{0}_{7\times 6N} & \boldsymbol{0}_{7\times 6} \\ \boldsymbol{0}_{6N\times 7} & \boldsymbol{F}_2 & \boldsymbol{0}_{6N\times 6} \\ \boldsymbol{0}_{6\times 7} & \boldsymbol{0}_{6\times 6N} & \boldsymbol{F}_3 \end{bmatrix} \tag{13}$$

$$\boldsymbol{B} = \begin{bmatrix} \boldsymbol{T}_1 & \boldsymbol{0}_{7\times 6N} & \boldsymbol{0}_{7\times 6} \\ \boldsymbol{0}_{6N\times 7} & \boldsymbol{I}_{6N} & \boldsymbol{0}_{6N\times 6} \\ \boldsymbol{0}_{6\times 7} & \boldsymbol{0}_{6\times 6N} & \boldsymbol{I}_6 \end{bmatrix}^{-1} \begin{bmatrix} \boldsymbol{G}_1(\boldsymbol{x}) & \boldsymbol{G}_2(\boldsymbol{x}) \\ \boldsymbol{G}_3(\boldsymbol{x}) & \boldsymbol{0}_{6N\times 6} \\ \boldsymbol{0}_{6\times 6N} & \boldsymbol{G}_4(\boldsymbol{x}) \end{bmatrix} \tag{14}$$

$$\boldsymbol{V} = \begin{bmatrix} \boldsymbol{T}_1 & \boldsymbol{0}_{7\times 6N} & \boldsymbol{0}_{7\times 6} \\ \boldsymbol{0}_{6N\times 7} & \boldsymbol{I}_{6N} & \boldsymbol{0}_{6N\times 6} \\ \boldsymbol{0}_{6\times 7} & \boldsymbol{0}_{6\times 6N} & \boldsymbol{I}_6 \end{bmatrix}^{-1} [V_{\mathrm{dc}} V_{\mathrm{dc}} V_{\mathrm{dc}} \boldsymbol{0}_{6N+10}]^{\top} \tag{15}$$

where $\boldsymbol{0}_{p\times q}$ is a $p \times q$ zero matrix, and $\boldsymbol{I}_{6N}$ and $\boldsymbol{I}_N$ are $6N \times 6N$ and $N \times N$ identity matrices, respectively

$$\boldsymbol{T}_1 = \begin{bmatrix} L & L & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & L & L & 0 & 0 & 0 \\ -L & -L & -L & -L & 2L & 0 & 0 \\ -L_{\mathrm{l}} & L+L_{\mathrm{l}} & L_{\mathrm{l}} & -L-L_{\mathrm{l}} & 0 & 0 & 0 \\ 2L_{\mathrm{l}} & -2L-2L_{\mathrm{l}} & L_{\mathrm{l}} & -L-L_{\mathrm{l}} & L & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{16}$$

$$\boldsymbol{F}_1 = \begin{bmatrix} -R & -R & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -R & -R & 0 & 0 & 0 \\ R & R & R & R & -2R & 0 & 0 \\ R_{\mathrm{l}} & -R-R_{\mathrm{l}} & -R_{\mathrm{l}} & R+R_{\mathrm{l}} & 0 & \frac{3}{2} & \frac{-\sqrt{3}}{2} \\ -2R_{\mathrm{l}} & 2(R+R_{\mathrm{l}}) & -R_{\mathrm{l}} & R+R_{\mathrm{l}} & -R & \frac{-3}{2} & \frac{-\sqrt{3}}{2} \\ 0 & 0 & 0 & 0 & 0 & 0 & -\omega \\ 0 & 0 & 0 & 0 & 0 & \omega & 0 \end{bmatrix} \tag{17}$$

$$\boldsymbol{F}_2 = -\frac{1}{CR_{\mathrm{cap}}}\boldsymbol{I}_{6N} \tag{18}$$

$$\boldsymbol{F}_3 = -\frac{1}{C_{\mathrm{vcm}}R_{\mathrm{c}}}\boldsymbol{I}_6 \tag{19}$$

$$\boldsymbol{G}_1 = \begin{bmatrix} \boldsymbol{V}_{a\mathrm{T}} & \boldsymbol{V}_{a\mathrm{B}} & \boldsymbol{0}_N & \boldsymbol{0}_N & \boldsymbol{0}_N & \boldsymbol{0}_N \\ \boldsymbol{0}_N & \boldsymbol{0}_N & \boldsymbol{V}_{b\mathrm{T}} & \boldsymbol{V}_{b\mathrm{B}} & \boldsymbol{0}_N & \boldsymbol{0}_N \\ \boldsymbol{0}_N & \boldsymbol{0}_N & \boldsymbol{0}_N & \boldsymbol{0}_N & \boldsymbol{V}_{c\mathrm{T}} & \boldsymbol{V}_{c\mathrm{B}} \\ \boldsymbol{0}_N & \boldsymbol{V}_{a\mathrm{B}} & \boldsymbol{0}_N & -\boldsymbol{V}_{b\mathrm{B}} & \boldsymbol{0}_N & \boldsymbol{0}_N \\ \boldsymbol{0}_N & -\boldsymbol{V}_{a\mathrm{B}} & \boldsymbol{0}_N & \boldsymbol{0}_N & \boldsymbol{0}_N & \boldsymbol{V}_{c\mathrm{B}} \\ \boldsymbol{0}_N & \boldsymbol{0}_N & \boldsymbol{0}_N & \boldsymbol{0}_N & \boldsymbol{0}_N & \boldsymbol{0}_N \\ \boldsymbol{0}_N & \boldsymbol{0}_N & \boldsymbol{0}_N & \boldsymbol{0}_N & \boldsymbol{0}_N & \boldsymbol{0}_N \end{bmatrix} \tag{20}$$

with

$$\boldsymbol{V}_{r\mathrm{T}} = [-V_{\mathrm{c},r1} - V_{\mathrm{c},r2} \ldots - V_{\mathrm{c},rN}] \tag{21}$$

$$\boldsymbol{V}_{r\mathrm{B}} = [-V_{\mathrm{c},r(N+1)} - V_{\mathrm{c},r(N+2)} \ldots - V_{\mathrm{c},r2N}] \tag{22}$$

$$\boldsymbol{G}_2 = \begin{bmatrix} V_{\mathrm{vcm},a\mathrm{T}} & V_{\mathrm{vcm},a\mathrm{B}} & 0 & 0 & 0 & 0 \\ 0 & 0 & V_{\mathrm{vcm},b\mathrm{T}} & V_{\mathrm{vcm},b\mathrm{B}} & 0 & 0 \\ 0 & 0 & 0 & 0 & V_{\mathrm{vcm},c\mathrm{T}} & V_{\mathrm{vcm},c\mathrm{B}} \\ 0 & V_{\mathrm{vcm},a\mathrm{B}} & 0 & -V_{\mathrm{vcm},b\mathrm{B}} & 0 & 0 \\ 0 & -V_{\mathrm{vcm},a\mathrm{B}} & 0 & 0 & 0 & V_{\mathrm{vcm},c\mathrm{B}} \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{23}$$

$$\boldsymbol{G}_3 = \frac{1}{C}\text{diag}(i_{a\text{T}}\boldsymbol{I}_N, i_{a\text{B}}\boldsymbol{I}_N, i_{b\text{T}}\boldsymbol{I}_N, i_{b\text{B}}\boldsymbol{I}_N, i_{c\text{T}}\boldsymbol{I}_N, i_{c\text{B}}\boldsymbol{I}_N) \tag{24}$$

$$\boldsymbol{G}_4 = \frac{1}{C_{\text{vcm}}}\text{diag}(i_{a\text{T}}, i_{a\text{B}}, i_{b\text{T}}, i_{b\text{B}}, i_{c\text{T}}, i_{c\text{B}}) \tag{25}$$

and $\mathbf{0}_y$ is a zero vector of length y. The parameters used in the above equations are the inductance and resistance of both the load and arm, L_l, L, R_l, and R, respectively. Moreover, diag(. . .) is a square diagonal matrix with entries inside the brackets at its main diagonal [$\diagdown$].

ACKNOWLEDGMENT

The authors would like to thank Dr. D. J. Thrimawithana, M. J. Neath, and J. Scoltock of the University of Auckland for their advice on the experiment setup and implementation.

REFERENCES

[1] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Power Tech Conf.*, 2003, vol. 3, p. 6.
[2] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modelling, simulation and analysis of a modular multilevel converter for medium voltage applications," in *Proc. IEEE Int. Conf. Ind. Technol.*, 2010, pp. 775–782.
[3] B. S. Riar and U. K. Madawala, "A novel modular multi-level converter topology with voltage correcting modules (M2LC-VCMs)," in *Proc. IEEE Int. Conf. Ind. Technol.*, 2013, pp. 451–456.
[4] M. M. C. Merlin, T. C. Green, P. D. Mitcheson, D. R. Trainer, R. Critchley, W. Crookes, and F. Hassan, "The alternate arm converter: A new hybrid multilevel converter with dc-fault blocking capability," *IEEE Trans. Power Del.*, vol. 29, no. 1, pp. 310–317, Feb. 2014.
[5] R. Feldman, M. Tomasini, E. Amankwah, J. C. Clare, P. W. Wheeler, D. R. Trainer, and R. S. Whitehouse, "A hybrid modular multilevel voltage source converter for HVDC power transmission," *IEEE Trans. Ind. Appl.*, vol. 49, no. 4, pp. 1577–1588, Jul. 2013.
[6] M. Hagiwara, I. Hasegawa, and H. Akagi, "Start-up and low-speed operation of an electric motor driven by a modular multilevel cascade inverter," *IEEE Trans. Ind. Appl.*, vol. 49, no. 4, pp. 1556–1565, Jul. 2013.
[7] M. Winkelnkemper, A. Korn, and P. Steimer, "A modular direct converter for transformerless rail interties," in *Proc. IEEE Int. Symp. Ind. Electron.*, 2008, pp. 174–179.
[8] M. Hagiwara and H. Akagi, "Negative-sequence reactive-power control by a PWM STATCOM based on a modular multilevel cascade converter (MMCC-SDBC)," *IEEE Trans. Ind. Appl.*, vol. 48, no. 2, pp. 720–729, Mar. 2012.
[9] J. Wang, R. Burgos, and D. Boroyevich, "A survey on the modular multilevel converters—Modeling, modulation and controls," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2013, pp. 3984–3991.
[10] K. Ilves, A. Antonopoulos, S. Norrga, and H-P. Nee, "Steady-state analysis of interaction between harmonic components of arm and line quantities of modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 57–68, Jan. 2012.
[11] K. Ilves, S. Norrga, L. Harnefors, and H-P. Nee, "Analysis of arm current harmonics in modular multilevel converters with main-circuit filters," in *Proc. 9th Int. Multi-Conf. Syst., Signals, Devices*, Mar. 2012, pp. 1–6.
[12] G. Konstantinou, J. Pou, S. Ceballos, and V. G. Agelidis, "Active redundant submodule configuration in modular multilevel converters," *IEEE Trans. Power Del.*, vol. 28, no. 4, pp. 2333–2341, Oct. 2013.
[13] B. S. Riar, U. K. Madawala, and D. Thrimawithana, "Analysis and control of a three-phase modular multi-level converter based on inductive power transfer technology (M2LC-IPT)," in *Proc. IEEE Int. Conf. Ind. Technol.*, 2013, pp. 475–480.
[14] B. S. Riar, T. Geyer, and U. K. Madawala, "Model predictive direct current control of modular multilevel converters: Modelling, analysis and experimental evaluation," in *Proc. IEEE Trans. Power Electron.*, doi: 10.1109/TPEL.2014.2301438.
[15] M. A. Perez, J. Rodriguez, E. J. Fuentes, and F. Kammerer, "Predictive control of AC-AC modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 7, pp. 2832–2839, Jul. 2012.
[16] K. Ilves, A. Antonopoulos, L. Harnefors, S. Norrga, and H.-P. Nee, "Circulating current control in modular multilevel converters with fundamental switching frequency," in *Proc. 7th Int. Power Electron. Motion Control Conf.*, Jun. 2012, pp. 249–256.
[17] R. Darus, J. Pou, G. Konstantinou, S. Ceballos, and V. G. Agelidis, "Circulating current control and evaluation of carrier dispositions in modular multilevel converters," in *Proc. IEEE Energy Convers. Congr. Expo. Asia Downunder (ECCE Asia)*, 2013, pp. 332–338.
[18] Y. Zhou, D. Jiang, J. Guo, P. Hu, and Y. Liang, "Analysis and control of modular multilevel converters under unbalanced conditions," *IEEE Trans. Power Del.*, vol. 28, no. 4, pp. 1986–1995, Oct. 2013.
[19] Z. Li, P. Wang, Z. Chu, H. Zhu, Y. Luo, and Y. Li, "An inner current suppressing method for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 28, no. 11, Nov. 2013.
[20] L. Angquist, A. Antonopoulos, D. Siemaszko, K. Ilves, M. Vasiladiotis, and H.-P. Nee, "Open-loop control of modular multilevel converters using estimation of stored energy," *IEEE Trans. Ind. Appl.*, vol. 47, no. 6, pp. 2516–2524, Nov. 2011.
[21] A. Antonopoulos, L. Angquist, and H-P. Nee, "On dynamics and voltage control of the modular multilevel converter," in *Proc. 13th Eur. Conf. Power Electron. Appl.*, 2009, pp. 1–10.
[22] G. Konstantinou, M. Ciobotaru, and V. Agelidis, "Selective harmonic elimination pulse-width modulation of modular multilevel converters," *IET Power Electron.*, vol. 6, no. 1, pp. 96–107, Jan. 2013.
[23] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*. Piscataway, NJ, USA: IEEE Press, 2003.
[24] J. Kolb, F. Kammerer, and M. Braun, "Dimensioning and design of a modular multilevel converter for drive applications," in *Proc. 15th Int. Power Electron. Motion Control Conf.*, 2012, pp. LS1a-1.1-1–LS1a-1.1-8.
[25] M. Zygmanowski, B. Grzesik, and R. Nalepa, "Capacitance and inductance selection of the modular multilevel converter," in *Proc. 15th Eur. Conf. Power Electron. Appl.*, Sep. 2013, pp. 1–10.

Baljit S. Riar (S'10) received the B.E. (Hons.) degree in electrical and electronic engineering from the University of Auckland, Auckland, New Zealand, in 2011, where he is currently working toward the Ph.D. degree in electrical and electronic engineering.

His research interests include power electronics, model predictive control, and inductive power transfer.

Udaya K. Madawala (M'95–SM'06) received the B.Sc. (Hons.) degree in electrical engineering from the University of Moratuwa, Moratuwa, Sri Lanka, and the Ph.D. degree in power electronics from the University of Auckland, Auckland, New Zealand, in 1987 and 1993, respectively.

After working in industry, he joined the Department of Electrical and Computer Engineering, University of Auckland as a Research Fellow in 1997, where he is an currently an Associate Professor, and his research interests include power electronics, inductive power transfer, and renewable energy.

Dr. Madawala is an active IEEE volunteer, he serves as an Associate Editor for IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and the IEEE TRANSACTIONS ON POWER ELECTRONICS. He is a Member of the Power Electronics Technical Committee of Industrial Electronics Society and the Sustainable Energy Systems Committee of IEEE Power Electronics Society.