A Fast Settling Oversampled Digital Sliding-Mode DC–DC Converter

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***Abstract*—An all-digital sliding-mode (ADSM) controlled dc–dc converter, utilizing single-bit oversampled frequency domain digitizers in its feedback path is proposed. Sliding-mode control provides several benefits over the traditional PID control in terms of fast transient response, robustness to parameter and component variations, and low sensitivity to loop disturbances. However, analog implementations of sliding-mode control require several amplifiers in the controller and suffer from process, voltage, and temperature variations. In the proposed approach, the sliding-mode controller (SMC) is implemented digitally; utilizing a first order single-bit $\Sigma\Delta$ frequency to digital converter ($\Sigma\Delta$FDC)-based feedback and reference digitizing ADCs, running at 32-MHz sampling rate. The ADSM regulator achieves 1% settling time in less than 5 μs for a load variation of 600 mA. The SMC uses a high-bandwidth hysteretic differentiator and an integrator to perform the sliding control law in digital domain. The proposed approach overcomes the steady-state error (or dc offset), and band limits the switching frequency, which are the two common problems associated with SMCs. The IC is designed and fabricated on a 0.35-μm CMOS process occupying an active area of 2.72 mm^2.**

***Index Terms*—Buck converter, digital switching regulator, hysteretic control, sigma-delta, sliding-mode control, variable structure system.**

I. Introduction

SWITCHED-MODE voltage regulators are an essential part of low-voltage battery operated electronic systems. From hand-held devices like mobile phones to the complex communications systems, processors and microcontrollers require a well-regulated voltage to work efficiently. The voltage conversion from the primary power source can be performed in more than one stage for better efficiency. Whether a single step-down converter is used or a multiple stages of step-down converters are implemented, the last stage must be able to reject the variations of the line and load due to fast transients in the state of the art processors.

Replacing the analog building blocks with their mixed-mode and digital counterparts makes switching regulators more robust to component variations and interest in digitally controlled switching converters have been increasing [1].

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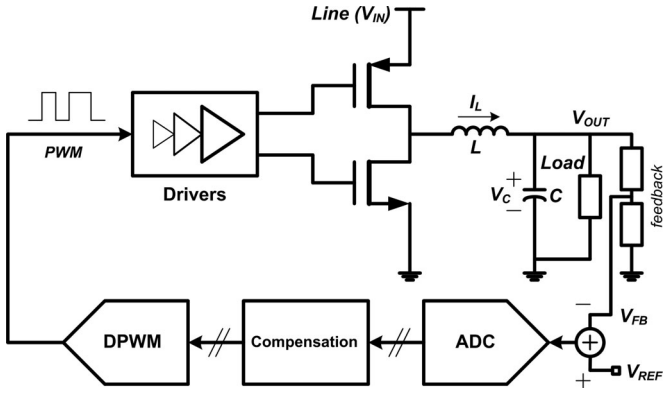

Fig. 1. All digital dc–dc buck converter.

Fig. 1 shows the basic structure of an all-digital controlled dc–dc buck converter. The error voltage between the scaled output voltage and a reference voltage is digitized by an analog-to-digital (ADC) converter. The digitized error undergoes a specific compensation scheme, and the duty cycle control word is used to control the power train by a digital pulse width modulator (DPWM).

Minimizing analog complexity associated with digitization of the output and reference voltages is a challenging design problem in low-power digitally controlled dc–dc converters [2], [3]. Another cha associated with digitally controlled dc–dc converters is the need for a digitally controlled PWM generator (DPWM) block, which is needed to create the duty cycle control command for the power train. A necessary but not sufficient condition is that the accuracy or resolution of the DPWM must be better than the feedback ADC. If the resolution of the DPWM is less than the resolution of the ADC, the loop may not be able to lock into one or more of the codes and the digital converter will toggle between two levels, a phenomenon known as limit cycle oscillation [4]. This problem could be remedied by increasing the resolution of the DPWM. The drawback of this approach is that the higher dynamic range in the ADC (which in turn determines the accuracy or sensitivity of the control loop) requires even higher number of bits in DPWM, which means more power consumption and more complexity in the DPWM core. The DPWM also causes delay and phase lag, which is not desirable in feedback control systems.

In order to eliminate the need for DPWM, prior approaches utilized sliding-mode-controller (SMC) or different forms of hysteretic controller. There are only limited digital implementations of the SMCs. In [5], analog error voltage is sampled and a digital sliding-mode controller (DSMC) is used to adjust the duty cycle. This approach works on a fixed switching frequency.

The fixed frequency approach slows down the transient response significantly. In [6], voltage error is translated from voltage to frequency and SMC is implemented in frequency domain by reformulating the sliding control. This method does not address the dc offset error associated with practical SMC implementations; therefore, the output voltage changes based on the output load current, impacting the load regulation. In [7], a digital approach similar to [6], which translates voltage to frequency and reformulates the sliding control law are used. However, the dynamic response shows large transients.

In this paper, a nonlinear controller based on a single-bit oversampling feedback ADCs and a DSMC is presented. The rest of the paper is organized as follows. The sliding-mode control theory is reviewed in Section II. The proposed DSMC and circuit level implementations are described in Section III. Experimental results are presented in Section IV, and Section V closes with conclusions.

II. Sliding-Mode Control Theory

Most of the state of the art switching-mode power supply controllers are designed by using a state-space averaging method, which is essentially a small-signal optimization [8]. Although this procedure works very well at steady-state operation, it has poor settling performance during large transient load variations. On the other hand, most switching regulators operate in one of the two structural modes, where one of the two switches is ON. Due to the nonlinear nature of the switching operation used in the design of these regulators, they are classified as variable structure systems (VSS). The SMC is a nonlinear controller that is suitable for variable structure systems. Therefore, it is a natural fit to utilize them in switched-mode power supplies like dc–dc step-down buck converters [9], [10].

Fundamental principle of the controller is to employ a certain sliding surface in the state space as a reference path such that the controlled state variable's trajectory can be directed toward a desired equilibrium point. Implementation of a sliding surface as a stabilizing reference path can be fully achieved by meeting the following three conditions [11]:

1) *the hitting condition:* whatever the initial conditions, the trajectories must reach the sliding surface;
2) *the existence condition:* the trajectories are directed/ forced toward the sliding surface when they are close to it;
3) *the stability condition:* the sliding surface will always direct the state trajectories toward a stable equilibrium point.

Fig. 2 shows the VSS-based switching behavior of a dc–dc converter along with its phase portraits in state space. The analog sliding surface based on the error signal e is defined in (2) as

$$e = V_{\mathrm{REF}} - V_C \tag{1}$$

$$S_a = K_{1a} \cdot e + K_{2a} \cdot e' = 0 \tag{2}$$

where V_{REF} represents the reference voltage, V_C is the capacitor voltage, and e is the error voltage between the reference and capacitor voltage in analog domain. The coefficients K_{1a} and K_{2a} are the analog controller coefficient, and S_a is the analog sliding law.

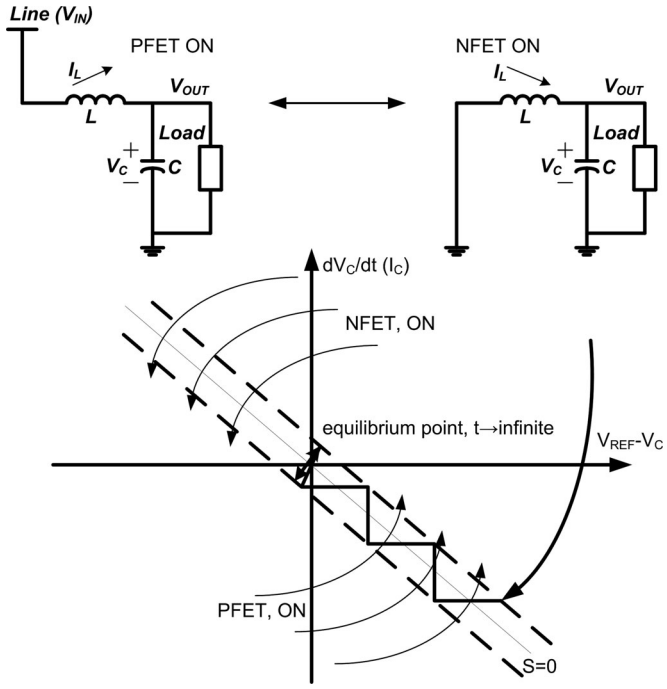

Fig. 2. Two distinct structural modes of a step-down buck converter, the *LC* filter, the trajectories, and the sliding surface in the state space.

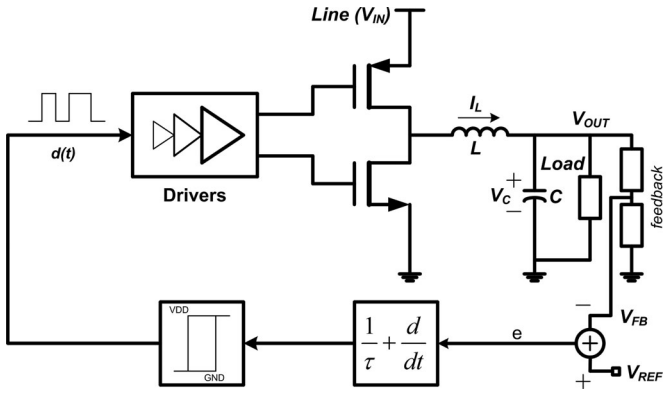

Fig. 3. Analog implementation of sliding-mode control in a step-down buck converter.

Fig. 3 presents the conceptual implementation of sliding-mode control in a buck converter [12]. If the system forces the error and its derivative to zero (the proportional and differential block in Fig. 3) under any conditions and disturbances, the system is stable. However, a switching regulator like a buck converter needs switch driver control pulses to regulate the output voltage. The ideal operation on the sliding surface and reaching the equilibrium point requires an infinite switching frequency besides the aforementioned three conditions, which is impractical. The hysteresis block shown in Fig. 3 (represented with dashed lines in Fig. 2) limits the switching frequency, and as a result, ripple about the desired steady-state operating point is generated.

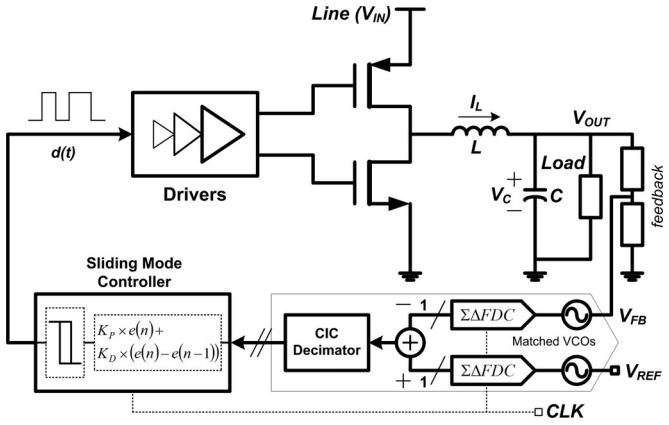

Fig. 4. Proposed oversampled, digital sliding-mode control buck converter.

III. Proposed Digital Sliding-Mode Control

The proposed DSMC is presented in Fig. 4. Compared to Fig. 1 (a conventional digitally controlled dc–dc buck converter), the small signal digital PID compensation block and DPWM block are replaced by a DSMC. Similar to the analog implementation of sliding mode in a buck converter shown in Fig. 3, the digital difference between the output voltage (or scaled version of it) and a reference voltage is processed by the DSMC. The structure and circuit implementation of the ADC and sliding mode are presented in the following sections, followed by a discussion on optimization of the feedback loop due to oversampling nature of the feedback ADC.

A. Analog to Digital Conversion

As described earlier, one of the critical components of a digitally controlled dc–dc converter is a feedback signal digitizer. The ADCs used for the digital dc–dc converter applications should be low power with high conversion efficiency. In the proposed DSM controller, a frequency domain $\Sigma\Delta$ ADC approach is adopted. One key property of FDSM is its much reduced hardware complexity and die area in comparison to flash (which requires 2^B comparators for a B-bit converter), pipelined (which requires a residue amplifier for each 1.5 bits) and SAR (which requires a large cap area). Overall, SDM-based approaches have a high resolution at lower frequencies, and frequency domain implementation allows for a low analog complexity design. Due to a single-bit comparator, their DNL/INL is superior to any Nyquist rate converter, such as SAR, pipelined or flash. The reference voltage and the output capacitor voltage are fed to two matched current-starved VCOs followed by $\Sigma\Delta$ frequency discriminators based on [13]. The difference between these bit-streams is decimated (or down-sampled) by an SINC filter to create a digital error signal. The benefits associated with two matched ADCs instead of a single multiplexed ADC includes elimination of an advisory circuit to decide when and how often to switch back and forth between the reference and output voltage, and better common mode noise rejection [2], [3].

As shown in Fig. 5, with the help of a VCO, two D flip–flops and one X-OR block, a first order $\Sigma\Delta$ frequency discriminator can be designed. Fig. 6 presents the voltage to frequency gain

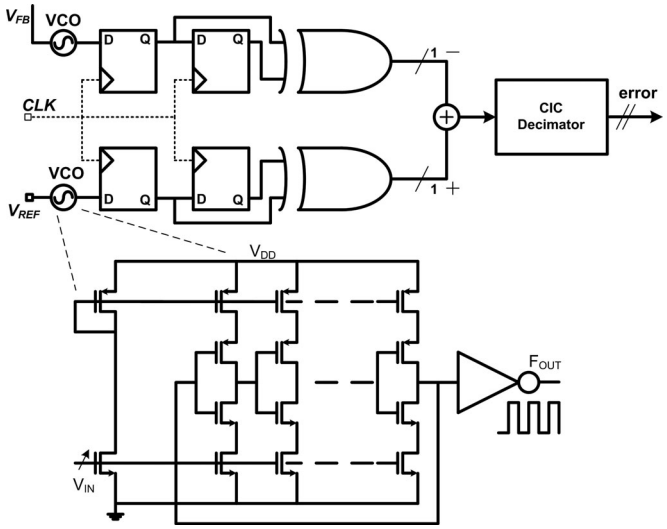

Fig. 5. Proposed frequency domain $\Sigma\Delta$ ADC, and current-starved VCO used as a voltage-to-frequency converter.

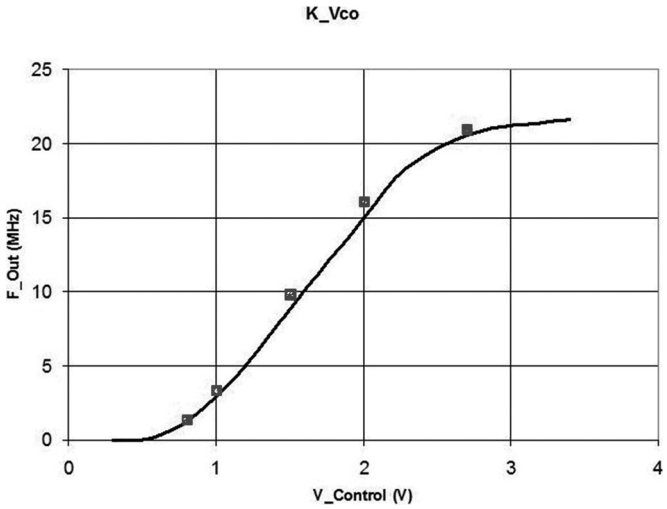

Fig. 6. VCO voltage-to-frequency gain (K_{VCO}), simulated (dots) and measured (smooth line).

(K_{VCO}) curve of the VCOs used in the design. The benefit of the proposed approach (and any other SMC) lies beneath the fact that the resolution of the ADC is only mandated by the dc–dc output voltage ripple requirement not the DPWM, and the lack of DPWM block lowers the risk of limit cycle oscillation stated earlier. Fig. 7 shows the measured FFT plot of the standalone ADC for an input frequency of $F_{\mathrm{IN}} = 7.395$ kHz, input peak-to-peak voltage swing of $V_{\mathrm{IN\_pk\text{-}pk}} = 200$ mV. The proposed frequency domain ADC can achieve effective number of bits (ENOB) of 8 bits, and signal-to-noise ratio (SNDR) of 50 dB. The proposed ADC has minimum analog complexity and can enable design reuse across different process technologies.

B. Digital Sliding Mode Controller

The proposed oversampled $\Sigma\Delta$ digital sliding-mode dc–dc converter enables an all-digital, fast response regulator without the need for a digital PWM generator. An improved digitized

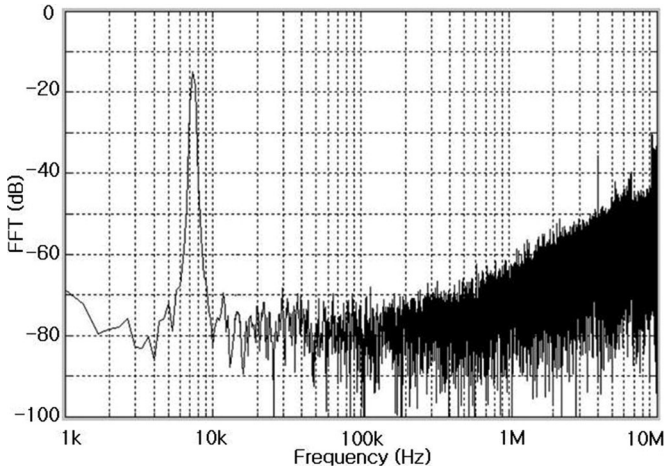

Fig. 7. Measured FFT at: $f_{\rm in}$=7.395 kHz, $V_{\rm in\_p}$=100 mV, ENB $\approx$ 8, SNDR $\approx$ 50.

version of a "hysteretic differentiator" made from an integrator inside a high-gain loop is employed in the proposed design based on [14]. In the proposed approach, the error-word takes two paths; one attenuation path to suppress the ripple at the output voltage and only passing the large transients acting as D (differential), and another path to set the duty cycle and frequency acting as PI (proportional, integral), which cancels the dc offset. Ultimately the comparator (shown at right end of Fig. 8) converts the scaled small-signal variations of the derivative of error signal into variation in the dc–dc converter switching duty cycle (or switch on-time) and also the frequency. The DSMC block also ensures stability of the system.

Practical SMC controllers [11] have a disadvantage of steady-state dc error. This error is not systematic and it changes with load and input conditions. In the proposed approach a dc error canceling integrator (shown in the dashed box in Fig. 8) is added to the controller with minimum impact on the system dynamics.

Even though in typical SMCs, the switching frequency of the converter is variable, by utilizing a digital switching frequency limiter block noted as $F_{\rm SW}$-Limiter in the PID path, the switching frequency can be limited. In this approach, the error is limited by an upper and lower bound, shown in Fig. 8. The limiter block is basically a digital clamp that is linear around zero and has hard limits on both sides, and it limits the wide variation of the switching frequency by limiting the error feeding the differentiator and forces a band around the desired center frequency. Approximately 7% of full-scale input dynamic range of the ADCs (2.0 V in the proposed IC) limits the switching frequency to 800 kHz–1.2 MHz range. Fig. 9 shows the variation of switching frequency $F_{\rm SW}$ (kHz) versus the $F_{\rm SW}$-limiting block range with respect to full-scale. For a higher percentage of full-scale, the switching frequency deviation is bigger and it provides greater range for line regulations and also faster responses for both line and load regulations. The drawback is that the frequency contents at the output have a wider band. Conversely, a smaller range of the full-scale has less frequency contents at the output with the price of having slower response time.

Fig. 10 presents high level simulations for similar SMCs with and without the integrator to show the presence of steady-statedc error.

In the proposed design, the capacitor voltage is chosen [6] as the state variable to be controlled. The discrete-time sliding control law is derived as follows:

$$e(n) = V_{\rm REF}(n) - V_C(n) \tag{3}$$

$$e(n) = e(n) - e(n-1) \tag{4}$$

$$S_d = K_P \cdot e(n) + K_D \cdot e(n) = 0 \tag{5}$$

where $V_{\rm REF}(n)$, $V_C(n)$, and $e(n)$ are reference voltage, capacitor voltage, and the error between them at the time sample of *n*, respectively. K_P and K_D are the controller coefficients in digital domain. The sliding surface is created by the error voltage and its derivative in digital domain.

A hysteresis band around the sliding surface (shown in Figs. 3 and 8) not only reduces the switching frequency to a practical one, it also divides the state space into two regions. The controller toggles back and forth between two regions with a frequency mostly set by the hysteresis band based on the following [14]:

$$f_{\rm SW} \approx K/(T_{\rm CLK} \cdot 4 \cdot |\Delta|) \tag{6}$$

where $f_{\rm SW}$ is the dc–dc converter switching frequency, $T_{\rm CLK}$ is the oversampling clock, K is a constant, and Δ is the hysteresis band. The values of K, Δ, and $T_{\rm CLK}$ for the prototype are: 2–4, 0.4, and 1/32e6, respectively. Fig. 11 shows simulated results for various conditions such as: different switching frequencies and duty cycles based on the proposed controller and (6), and measured data verifies (6) and it is presented in Section IV.

The overall transfer function of the controller in Laplace-domain, considering oversampling can be approximated as [14]

$$\text{Switching\_Control}\,(s)/e(s) \approx (K_P + (K_D \cdot s)) + (K_I \cdot s^{-1}) \tag{7}$$

where K_P is the proportional coefficient, K_D is the differential coefficient, K_I is the integral coefficient, and $e(s)$ is the error voltage and Switching_Control is the desired pulse train.

The first part of the transfer function is the PD function representing the sliding surface, and the second part of the transfer function is the integrator added to reduce the dc offset error without loss of generality.

C. Quantization Noise Filtering Versus Phase Margin Optimization

Quantization noise shaping associated with $\Sigma\Delta$ modulation pushes the quantization noise to higher frequencies; on the other hand, nonlinear systems such as the DSMC can fold high frequency high power out of band noise to in-band. In addition to noise folding, higher frequency tonal content can intermodulate and bring the tones in-band, causing ripple at the converter output. In case of a typical decimation filter, the filter zeros are selected such that the signal images in the spectral folding regions are suppressed, and have no in-band folding effect after decimation. In the SINC filter approach we used, there are

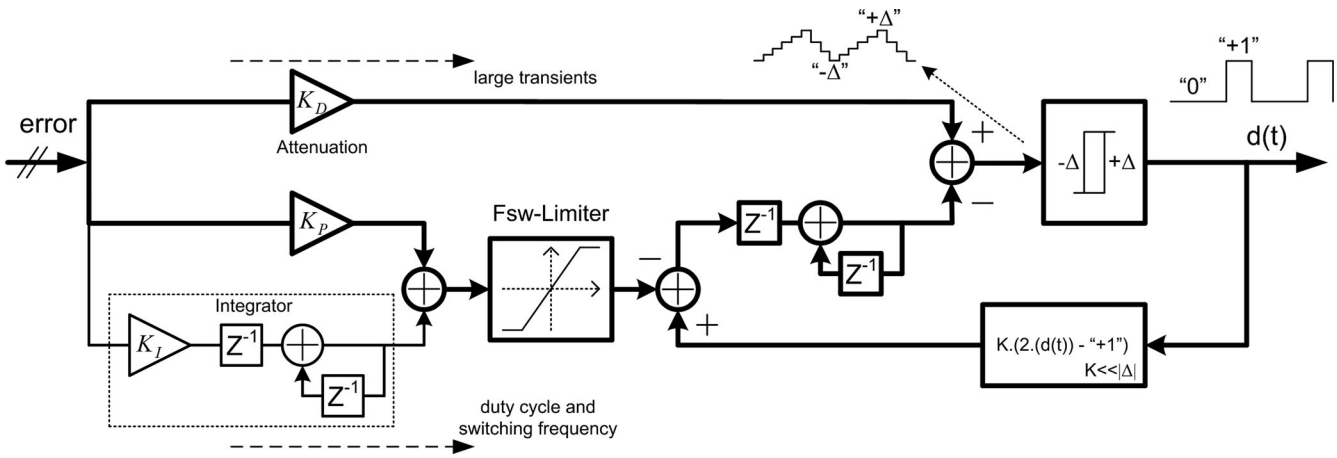

Fig. 8. Proposed digital SMC: two separate paths for error, dc offset cancelation integrator, and switching frequency $F_{\rm sw}$-limiting block.

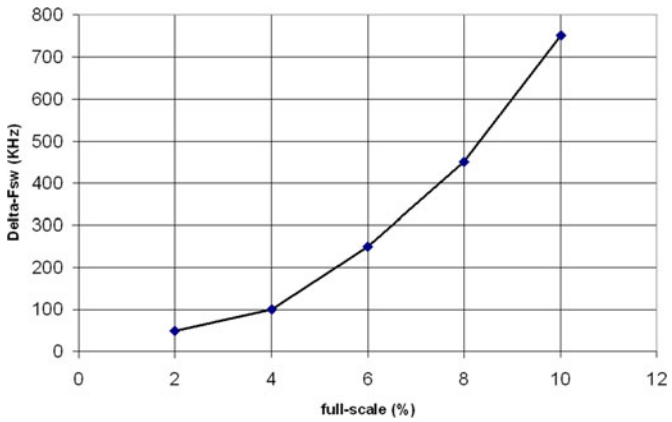

Fig. 9. Variation of switching frequency $F_{\rm SW}$ (kHz) versus the $F_{\rm sw}$-limiting block range with respect to full-scale.

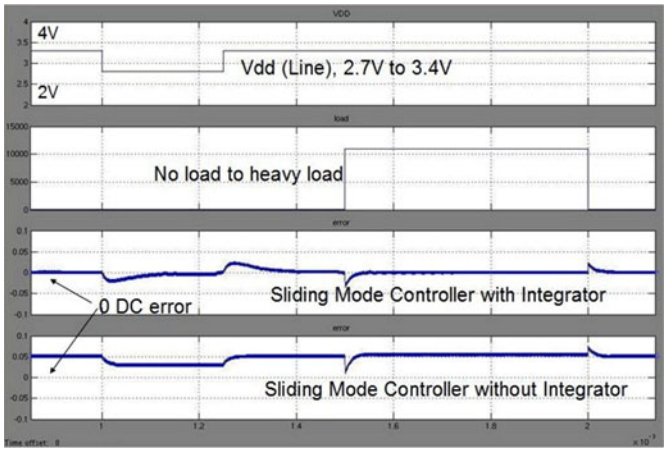

Fig. 10. Elimination of the steady-state dc error in a sliding mode controller compared with a similar controller without an integrator (simulations).

filtering zeros at the exact folding regions of the input signal. Nonlinearity impact is not similar to decimation. As an example, two quantization noise tones at a much higher frequencies f_1 and f_2, their odd harmonic product after a nonlinear operation would be $2f_1 +/- f_2$.This could fold noise and tones very close to dc, causing high ripple content. Therefore, limiting spectral content before any nonlinear operation is necessary. If decimation filtering is not used at the ADC output, the aliased noise within the converter bandwidth can leak to the regulator output.

This problem can be reduced by optimum filtering of the output of the noise shaped ADCs using high-order SINC filtering with minimum phase delay. SINC decimation filters provide effective sampling rate reduction with minimum hardware complexity. On the other hand, higher order decimation filtering can cause excessive phase delays, causing stability problems. For a typical order-N, decimate-by-M SINC filter, the phase delay could be derived as [15]

$$\angle H\left(f\right) = \pi \cdot N \cdot \left(f/f_{\rm CLK}\right) \cdot \left(1 - M\right) \tag{8}$$

where $H(f)$ is transfer function of the SINC filter. In order to suppress the first-order shaped noise, typically a second-order decimation filtering is required. An order-B $\Sigma\Delta$ modulator generates a shaped quantization noise as follows [15]:

$$E_q(z) = \varepsilon_q . \left(1 - z\right)^B \tag{9}$$

where ε_q is the quantization error noise density. In a DSMC application, the controller requires a high SNDR estimation of digitized values of the state of interest (and its derivative) at every switching cycle. Therefore, an optimum decimation ratio must be derived for a given switching frequency range.

The critical nonlinearity of the proposed DSMC occurs at the input of the nonlinear hysteresis block; therefore, it is critical to minimize quantization noise at that point. The quantization noise spectral density at the input of the nonlinear hysteresis block shown is represented as

$$E_q\left(z\right) \cdot H\left(z\right) \cdot {\rm TF}\left(z\right) = \varepsilon_q \cdot \left(1 - z^{-1}\right) \cdot \left[\frac{1}{M^2}\left(\frac{1-z^{-M}}{1-z^{-1}}\right)^2\right]\left(K_D - K_P\frac{1}{1-z^{-1}} + K\frac{1}{1-z^{-1}}\right) \tag{10}$$

where $H(z)$ is the second-order SINC response and ${\rm TF}(z)$ is the SMC transfer function, the coefficients were described earlier, and for simplicity, the integrator was not included in this calculation. Total integrated noise power at the input of the nonlinear

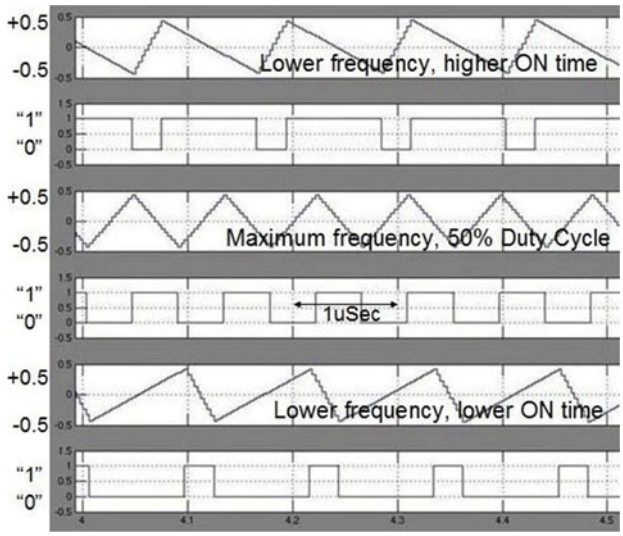

Fig. 11. Switching control pulses per (6) for various conditions, the top waveform of each pair shows the input to the comparator in Fig. 8 and the bottom waveform of each pair shows the output of the comparator for each of three conditions (simulations).

hysteresis block $\varepsilon^2_{q,\mathrm{RMS}}$ is represented as

$$\varepsilon^2_{q,\mathrm{RMS}} = \int_0^{(f_{\mathrm{CLK}})/2} CO_1 \cdot \varepsilon_q^2 \sin^2\left(\pi f / f_{\mathrm{CLK}}\right) \cdot \left(\frac{\sin\left(\pi M f / f_{\mathrm{CLK}}\right)}{\sin\left(\pi f / f_{\mathrm{CLK}}\right)}\right)^2 \cdot \left(CO_2 + CO_3 f\right)^2 \cdot df \tag{11}$$

where CO_1 reflects the products of constants, and CO_2 and CO_3 are just consolidated coefficients when moved from Z domain to S domain. Optimum filtering of the output of the noise shaped ADCs using SINC filtering requires minimum phase delay with maximum noise suppression. Higher decimation ratio gives rise to a higher phase delay, eventually causing instability in the feedback operation. On the other hand, lower decimation ratio cannot suppress out-of-band quantization noise, and effects of aliased noise and spurs can start showing up in-band. This increases in-band noise at the converter output. In both high quantization case, as well as high delay case, there is considerable risk associated due to nonlinearity of the system: in the high quantization noise case, high-frequency quantization noise due to noise shaping would fold in-band due to nonlinearities in the feed-forward case and impact overall noise floor. In the case of high decimation ratio, the group delay of the decimation filter would degrade the phase margin of the system. Degraded phase margin would cause load dependent stability issues that may not necessarily show up in a linearized model. Based on heuristic transient simulations, it was found that minimizing the product of both design variables yields the most robust stability margin, which can be formulated as

$$g = \min\left\{e_{q,\mathrm{RMS}} \cdot \left(\pi N \left(f / f_{\mathrm{CLK}}\right)\left(1 - M\right)\right)\right\}. \tag{12}$$

In Fig. 12, the product of the delay times the integrated quantization noise associated with lower oversampling at the differentiator input for the proposed design is plotted versus decimation ratio. Based on the figure of merit shown in Fig. 12, a decimation ratio of 16 gives the optimum noise and delay product and also it provides simplicity of hardware design.

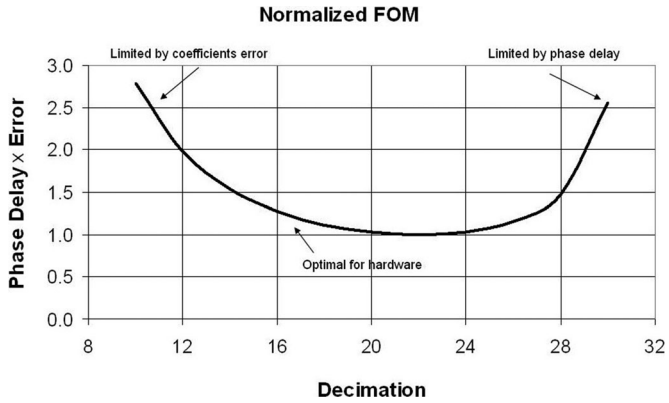

Fig. 12. Optimization of decimation ratio.

D. Comparison of SMC to Existing Control Schemes

Since most available designs, and particularly, most of the commercial products in power management are based on small signal approximation [8] approach and they require PID compensation, difference between these approaches and the proposed large signal PD or PID should be described. Other fast transient controllers like Hysteretic controllers will be compared with sliding-mode approach for their similarities and differences.

1) Large Signal and Small Signal PID: The proposed design of PD (or PID with the added integrator) is a large-signal PID, as opposed to the small-signal PID utilized in typical dc–dc converters. In a typical small signal PID, the controller is responsible for stability only and it is significantly slow since it is designed based on local linearization of a nonlinear system. In SMCs (and the proposed approach), the PD or PID are the main part of the controller. Although adding integration operation to any loop makes the system slower to respond to disturbances, in practice [16], the integral action in this approach (and in SMCs) is enabled only when the system is on the sliding line/surface, and only PD is in charge of the large transients. It is not possible to obtain similar performance from a typical small signal PID controller [17], [18].

2) Hysteretic and Sliding-Mode Controls: Hysteretic controllers are in fact a simplified version of SMC (or generally speaking hysteretic controllers and SMCs are in the larger category of "Bang–Bang" nonlinear controllers). Hysteretic controllers are fast since similarly to SMCs they do not require a fixed frequency clock. However, hysteretic controllers do not provide the wide range of robustness for line and load variations, since they simply make the current (or in a few cases voltage) toggle between two predefined values [19], [20]. They provide poor load and line regulations and mostly being used as a secondary controller (along with a fixed frequency main controller) when there is a need to respond to a large transient, or they are used as a second stage following a low drop-out regulator (LDO)

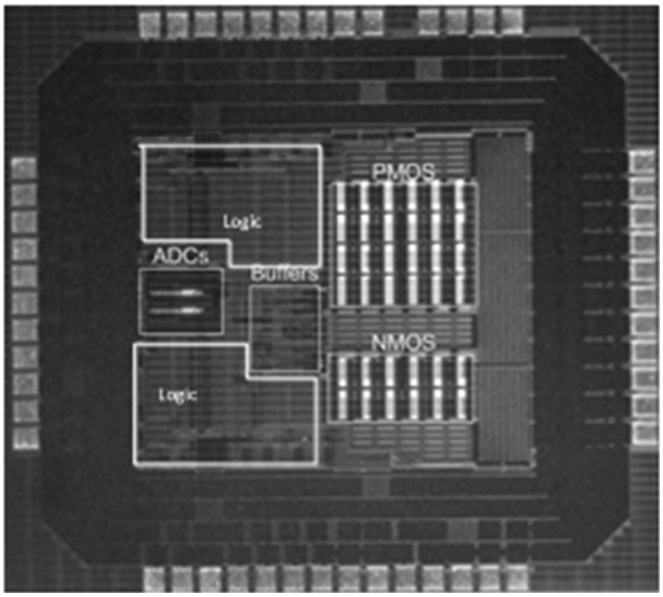

Fig. 13. Die micrograph.

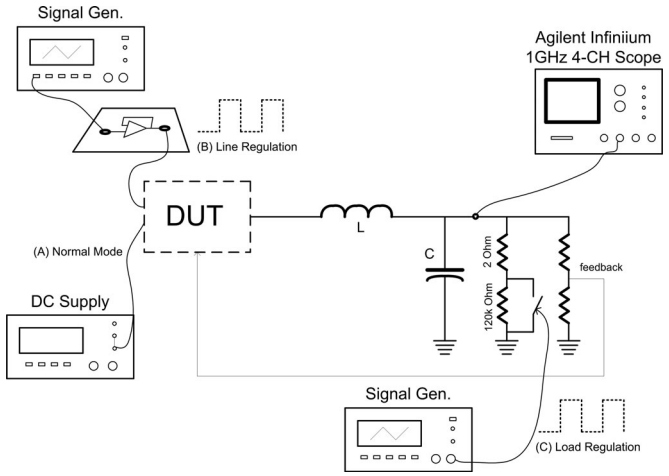

Fig. 14. Test setup for normal mode of operation, line regulation, and load regulation.

or another buck converter to provide fast tracking of a reference as adaptive power supplies. One should consider the true efficiency when comparing these types of hysteretic controllers to a complete controller such as a self-sufficient sliding-mode buck converter. The SMCs, on the other hand, work on the states of the system and bring the system to a zero error constantly upon power up and any other disturbances and they provide excellent line and load regulations.

3) Sliding-Mode Control Shortcomings: It is important to distinguish a practical SMC's shortcomings and issues with its implementation in buck converters [5]. Wide variation of switching frequency and dc offset error are the shortcomings associated with sliding mode in general, since ideal sliding mode based on the Lyapunov theory [12] is difficult (impractical) to achieve. Problems with the ESR of the filter capacitor, which makes the difference between the capacitor's voltage (the state of interest) and output voltage bigger, and therefore, causing accuracy errors at the output, is a trait that belongs to buck converters and the way sliding mode is implemented. If one can measure or estimate the values of the states of interests (or the value of the state and its derivative) for every switching cycle, the accuracy error or dependence of the output voltage on the ESR of the capacitor is no longer an issue. In many implementations of sliding mode such as this study, the value of the output voltage is being taken in lieu of the filter capacitor voltage; therefore, a low ESR capacitor is required. This does not project any practical limitations or drawbacks in these implementations.

IV. Experimental Results

The IC is fabricated on a five-layer metal, one-level poly, 0.35-μm radiation hardened CMOS process. Fig. 13 shows the die micrograph. Of the three conditions that are required for the implementation of a sliding surface as a stabilizing reference path as stated earlier, the hitting condition in a buck converter is satisfied due to its alternating structural modes (see Fig. 3). To meet the existence condition, the ratio of the proportional to differential coefficient should be as much as twice the natural frequency of the *LC* filter to maintain the sliding condition [6]. To achieve this K_P and K_D were set to the values of 0.06 and 6.8e-6, respectively, and K_I was set to a value of 32, along with an inductor value of 1.5 μH, and a capacitor value of 220 μF (typical ESR $= 0.012\ \Omega$), and the values of K, Δ, and T_{CLK} for the prototype are: 2^{-4}, 0.4, and 1/32e6, respectively. The ADCs provided about 7.5 bits resolution, enough to get LSB of 12 mV (from a 2-V full scale reference).

The manufactured chip was tested and measured for various conditions, and its performance matched the theoretical results. In order to observe the load regulations as shown in Fig. 14, the load consists of a low impedance resistor in series with a high impedance resistor, and a power FET in parallel with the high impedance resistor. The power FET is switched OFF and ON with a pulse generator to change the loading from no-load condition (low output current) to heavy load condition (high output current).

Most dc supplies do not provide pulsed outputs or V_{DD}, and most (if not all) signal generators cannot tolerate heavy loading on them. In order to observe the line regulations, a separate board was designed. A power amplifier was designed in buffer mode, and the signal generator was used as its input. The amplifier output was pulsed accordingly and used as V_{DD} or line.

Fig. 15 shows line regulation for $V_{\mathrm{IN}} = 3.6$ V, and $V_{\mathrm{OUT}} = 1.2$ V. The input voltage (line) is changed to 20% of its value at a frequency of 1 kHz. The controller settles 1% accuracy within 20 μs with less than 3% overshoot/undershoot.

Fig. 16 presents load regulation (zoomed in for a better observation). The converter achieves 1% settling in 5 μs with an average switching frequency of 1 MHz, and maximum undershoot of 5% for $V_{\mathrm{IN}} = 3.6$ V, $V_{\mathrm{OUT}} = 1.2$ V.

The measured peak efficiency of the converter for: $V_{\mathrm{IN}} = 3.6$ V, $V_{\mathrm{OUT}} = 2.5$ V, oversampling clock frequency of 32 MHz, and switching frequency of $\sim$1 MHz was 83%. The efficiency

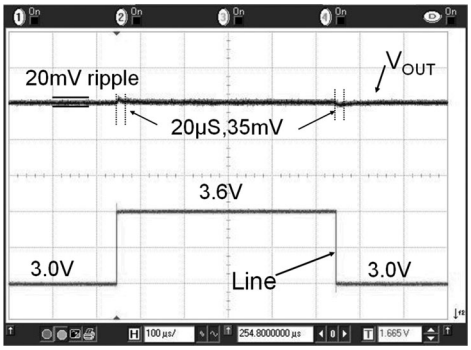

Fig. 15. Line regulation, $V_{\rm out}$ (top trace, 100 mV/div), Line (bottom trace, 300 mV/div), and time (100 μs/div).

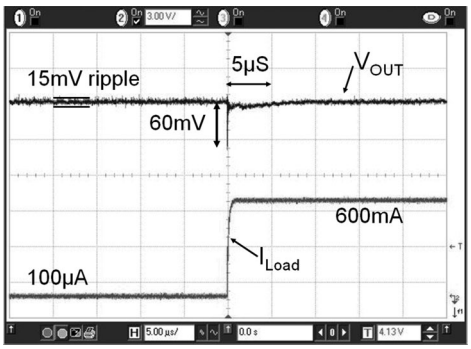

Fig. 16. Load regulation, $V_{\rm out}$ (top trace, 50 mV/div), Load change command (bottom trace, 0.1 mA–600 mA), and time (5 μs/div).

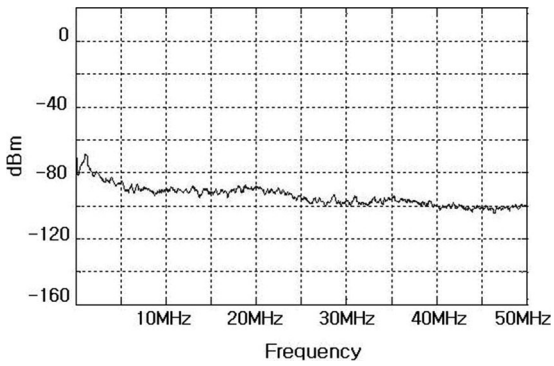

Fig. 17. PSD of the output shows no spurs repeated on the switching frequency and its multiples.

can be enhanced by a fine geometry process with reduced power supply voltage.

The measured output voltage PSD is shown in Fig. 17, and as stated earlier, due to the novelty of this approach not only the switching frequency and its harmonics' tones are not present, there is only a small hump due to the band-limited $F_{\rm SW}$.

The measured output ripple for a wide range of oversampling clock frequency of 22 MHz–42 MHz, which translates to a typical switching frequency of 900 kHz—1.7 MHz is 23 mV, neither a function of switching frequency nor the ESR of the filter capacitor, as long as the ESR is reasonably low. This matches (6) pretty well and it is shown in Fig. 18.

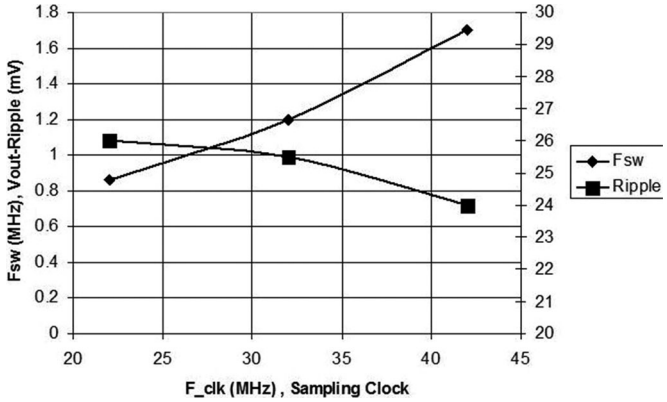

Fig. 18. Output voltage ripples and frequency as a function of the sampled clock (diamonds: switching frequency; squares: ripples).

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

Parameter	[6] , 2002	[7] , 2010	This Work
Technology	0.25um CMOS	0.35um CMOS	0.35um CMOS
Die Area	1.43mm2	1.3mm2	2.72mm2
Vin/Vout (V)	2.5/1.1~2.3	1.6~3.3/0.9~3.0	2.8~3.8/1~2.5
Vout Ripple	<15mV	<30mV	<23mV
Switch. Freq. (MHz)	0.460-0.860	0.250*	0.800-1.2
Efficiency	89%~95%	96.5% (max)	72%~83%**
Settling Time	5us (for 80mA)	0.6us (for 45mA)	5us (for 600mA)
Overshoot	65mV	122mV	60mV
Settling Time Line reg.	pre-regulated input	N/A	20us (for 20% line-jump)
Overshoot for line reg.	pre-regulated input	N/A	3%

*Not Reported, extracted from the plots.
**Due to process limitations, see text.

The performance summary along with comparison to two of the references is presented in Table I.

V. CONCLUSION

A DSMC for point of loadPOL applications employing frequency domain $\Sigma\Delta$ ADCs and a high-bandwidth digital hysteretic differentiator was introduced. The dc error associated with the SMC controllers is suppressed by utilizing an integrator, without impacting the first-order behavior expected from the SMC controllers. To avoid a wide variation in the switching frequency response, a frequency-limited operation was implemented. The ADSM regulator achieves 1% settling time in less than 5 μs for a load variation of 600 mA. The SMC uses a high-bandwidth hysteretic differentiator and an integrator to perform the sliding control law in digital domain. The DSMC proved robustness to disturbance and fast transient response to load and line variations.

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