# Quasi Two-Level Operation of Modular Multilevel Converter for Use in a High-Power DC Transformer With DC Fault Isolation Capability

I. A. Gowaid, G. P. Adam, *Member, IEEE*, Ahmed M. Massoud, *Senior Member, IEEE*, Shehab Ahmed, *Senior Member, IEEE*, Derrick Holliday, and B. W. Williams

***Abstract*—DC fault protection is one challenge impeding the development of multiterminal dc grids. The absence of manufacturing and operational standards has led to many point-to-point HVDC links built at different voltage levels, which creates another challenge. Therefore, the issues of voltage matching and dc fault isolation are undergoing extensive research and are addressed in this paper. A quasi two-level operating mode of the modular multilevel converter is proposed, where the converter generates a square wave with controllable *dv/dt* by employing the cell voltages to create transient intermediate voltage levels. Cell capacitance requirements diminish and the footprint of the converter is reduced. The common-mode dc component in the arm currents is not present in the proposed operating mode. The converter is proposed as the core of a dc to dc transformer, where two converters operating in the proposed mode are coupled by an ac transformer for voltage matching and galvanic isolation. The proposed dc transformer is shown to be suitable for high-voltage high-power applications due to the low-switching frequency, high efficiency, modularity, and reliability. The dc transformer facilitates dc voltage regulation and near instant isolation of dc faults within its protection zone. Analysis and simulations confirm these capabilities in a system-oriented approach.**

***Index Terms*—Dual active bridge (DAB), dc fault, dc/dc power conversion, dc transformer, modular multilevel converter (MMC).**

## I. Introduction

THE increasing penetration of renewable energy into power grids, along with ambitious carbon reduction targets, is the main driving force towards new energy trade and security regulations worldwide. In this regard, high-voltage dc grids are viewed as a key element in building anticipated high capacity transmission systems. However, realization of such dc systems is surrounded by challenges ranging from the need for a new business model to major technical obstacles and lack of operational experience. Nevertheless, the concept continues to gain momentum across the industry.

Voltage-source converter (VSC) based dc transmission systems offer an essential feature; power reversal is realized without reversing the dc voltage polarity. A feature conventional current-source converter based dc transmission systems lack. Therefore, the VSC multiterminal dc (MTDC) grid is the core of academia and industry interests when looking beyond point-to-point connections.

Analogous to an ac system, a reliable dc grid must feature defined protection zones with high selectivity where all types of faults are rapidly isolated without affecting the rest of the system. Isolating and clearing dc faults is a showstopper for dc networks. A dc circuit breaker (CB) is required to interrupt high-fault currents in the absence of zero-current crossings [1]. The low impedance of a dc circuit leads to a steep rise in fault current where protection of power electronics necessitates interruption times in the order of a few milliseconds. Conventional mechanical CBs are slow and suited to ac type faults [1]–[3]. Solid-state dc CBs can achieve fast interruption times but at high capital cost and on-state operational losses [4]. A hybrid dc CB has been proposed where a mechanical path serves as a main conduction path with minimal losses during normal operation, and a parallel connected solid-state breaker is used for dc-fault isolation [4], [5]. However, capital cost remains high, and it has relatively large footprint. The mechanical opening time is a few milliseconds at 80 kV and is expected to increase because of the increased time needed to bridge the wider contact gap at higher voltage ratings. The semiconductors conduct and commutate high-fault currents arising during the mechanical CB opening time. Furthermore, for reliable grid-wide protection, proper and fast coordination between individual dc CBs in different sections of the grid must be administered to achieve fast interruption times [1]. The interruption time must be less than the dc line time constant, which is typically a few milliseconds.

Voltage regulation and optimized power flows through network lines are mandatory for proper and efficient operation of a dc grid. Dual to frequency in an ac network, a stable dc-voltage level is the indicator to power balance along the dc system. Several techniques have been devised for dc-line voltage control

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as reported in [6]–[11]. However, most of these techniques are not suitable for generic dc grids, with large numbers of converters and busses. Furthermore, additional power flow controllers, similar to phase shifters in an ac system, may be needed to support system voltage stability [12].

A real dc super-grid with multiple in-feed points, tapping points, and various terminals connected to different ac grids makes the voltage regulation issue more complex. Forming and solving an optimal dc load flow problem may be a practical solution to calculate terminal voltage set points. Information and commands throughout the network can be exchanged between individual dc busses and a control center, which determines optimal load flow scenarios similar to ac systems [13]. In general, any attempt to address voltage regulation in a real dc super-grid cannot disregard that it is not possible to build a vast grid without voltage stepping and matching. Unlike an ac transformer, the so-called 'dc transformer' will be based on active controlled power electronic components where dc voltage control and/or power flow control can be readily augmented. Having grid components dispersed through the dc network actively contributing to voltage regulation, power flow control, and rapid fault protection, in addition to terminal ports, will significantly boost network controllability and security.

While organizations such as the CIGRE, IEEE, and IEC are developing guidelines and standards for common HVDC manufacturing and operation practices, more point-to-point links are planned and commissioned in the absence of common standards [4]. The result is more point-to-point connections at different voltage levels (e.g., $\pm$80 kV, $\pm$150 kV, and $\pm$320 kV) and different topology concepts [4]. Therefore, apart from any efficiency considerations, high-power dc transformers appear the only way to interconnect and retrofit existing point-to-point links. If dc transformers built with active components are present at vital nodes throughout a potential dc grid, an augmented fault protection function will constitute a milestone toward a super-grid.

A multitude of dc–dc converter designs for low and medium voltage and power ranges are in operation across industry and power systems. High switching losses render traditional high-frequency hard-switched converters unsuitable for bulk power applications. Soft-switched converters offer low switching losses [14]; hence, may be more applicable for heavy power transfer. Such a low-loss characteristic is achieved using a resonant stage allowing zero-voltage switching or zero-current switching. The switching frequencies of both transformer and transformerless designs [15]–[25] are selected in the range of kilohertz or even tens of kilohertz in an attempt to reduce the size of the transformer and passive resonant components. However, these designs aim at medium voltage (a few kilovolts) and medium power (a few megawatts) applications such as, wind generation, dc distribution, and transportation. Apparently, a dc grid requires dc transformers capable of handling hundreds or even thousands of megawatts, at hundreds of kilovolts.

Scaled up versions of the designs discussed in [15]–[26] are not compatible as the basis of an ultrahigh voltage ultrahigh power dc transformer. The reasons range between unidirectional operation, extremely high-voltage stresses on passive components of resonant designs, destructive voltage derivatives acting upon the coupling transformer stage, and the high-frequency operation. A 25 MW HVDC tap was proposed in [27], [28], which is a unidirectional design to tap power to loads and not a solution for line interconnection with large power exchange.

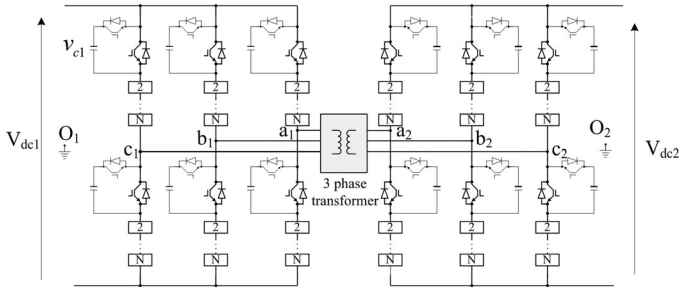


Fig. 1. MMC-based dc transformer for high-voltage high-power applications.

An interesting dc converter topology, claimed appropriate as a dc transformer for MTDC grids, is analyzed in [1], [29]–[33]. The topology is transformerless, thyristor-based featuring a "rotating" capacitor resonating with inductors to achieve high-voltage stepping ratios. However, the peak capacitor voltage in normal operation exceeds that of the high dc voltage side. Being exposed to such high-voltage stresses, switching device arrays in both the primary and secondary sides must be rated at higher than the high-side dc voltage. Furthermore, the proposed topology lacks isolation and defined ground separation between the low- and high-voltage circuits, which is not reliable considering the critical role of the dc transformer in bulk power transfer.

Conceptually, dual active bridge (DAB) dc–dc converter configurations may have potential as high-power dc transformers [34]–[40]. They employ an ac transformer to perform voltage stepping. Three-phase topologies enjoy low-ripple currents in addition to simple phase angle control and an inherent soft switching nature. The problem of transformer phase current unbalance, due to asymmetric leakage inductances, is addressed in [25], [34] through fast controllers. However, square-wave operation of the DAB converters is a fundamental drawback at high voltage. This impedes their scalability since the very steep rising and falling edges of square wave voltages apply destructive *dv/dt* stresses on transformer insulation. Moreover, the adopted ranges of switching frequency are not applicable in applications with gigawatt-level power transfer.

Taking into account the features of existing technology, and the trend towards modular designs, this paper proposes a dc transformer based on modular multilevel converters (MMC). Two three-phase MMCs are connected through an ac transformer as in Fig. 1; a high-voltage converter and a medium (lower)-voltage converter. Both MMCs employ half-bridge cells. The proposed operating mode is expected to offer a considerable reduction in converter footprint, cost and weight. Power flow control or dc-voltage regulation is administered by phase shift and voltage magnitude (modulation index) control. Both modular converters operate in a quasi-two-level (Q2L) mode in order to alleviate voltage derivative *dv/dt* stress on the ac transformer stage, thereby rendering the proposed dc transformer topology viable

at ultrahigh voltage levels. The trapezoidal voltage waveform, with controllable slopes, is created by sequential switching of the cells as in a conventional MMC operating with sinusoidal reference in a staircase mode.

In the proposed operating mode, each cell capacitor is utilized as an energy tank (switch-voltage clamp) to generate intermediate voltage levels for a few microseconds during transitions between $\frac{1}{2}V_{\rm dc}$ and $-\frac{1}{2}V_{\rm dc}$, allowing cell capacitances to be drastically reduced. This considerably reduces the footprint and cost of each Q2L converter. In Q2L mode, the arms currents of the converter do not contain a common-mode dc component, unlike conventional MMC operation; therefore, semiconductor losses are reduced. When a dc fault occurs, the proposed Q2L dc transformer (specifically the nonfault-side converter) rapidly isolates the faulted line such that the rest of the dc grid remains functional. Furthermore, galvanic isolation stops fault propagation between dc transformer sides, even when a fault occurs in one of the dc transformer converters. Modified design of conventional ac power transformer core reduces iron losses allowing switching frequency in the range of a few hundred Hz where a number of low-order harmonics engage in power transfer.

The paper investigates the role of the proposed dc transformer in addressing some of the technical challenges related to proper operation of generic dc grids with multiple dc-voltage levels, including dc fault ride-through. The study includes aspects related to losses, cost, and additional functionality.

## II. Brief Review of Conventional Operation of MMC

Conventionally, established modulation techniques operate the MMC such that the upper and lower arms of the same phase-leg conduct simultaneously, and this constitutes the sum of the cell capacitor voltages in conduction path of both arms must be equal to the total dc-link voltage minus the ac voltage drop in the arm inductances [41]–[44]. This necessitates the voltages developed across the cell capacitors of the upper and lower arms to be complementary, which can be approximated by

$$\begin{aligned} v_{x1} &= \frac{1}{2}V_{\rm dc}(1 - m\sin(\omega t + \varphi_x)) \\ v_{x2} &= \frac{1}{2}V_{\rm dc}(1 + m\sin(\omega t + \varphi_x)) \end{aligned} \tag{1}$$

where $V_{\rm dc}$ is the converter input dc-link voltage, $m$ is modulation index, and $\varphi_x = \left\{0,\ \frac{4}{3}\pi,\ \frac{2}{3}\pi\right\}$ for three phases $a, b$, and $c$, respectively. With such simultaneous operation of the upper and lower arms, the arm currents of each phase-leg contain ac and dc components. The ac component of the arm current comprises the fundamental current that is associated with active power exchange between the converter and the ac side, and a number of low-order harmonics (predominantly second harmonic) that are caused by cell capacitor voltage fluctuations in attempt to counter the ac voltage drop in the arm inductances. The dc component of the arm current is associated with the power exchange between the converter and the dc side. In steady-state, the converter power exchange with the ac side equals the power exchanged with the dc side. Under such a condition, the converter cell capacitors exchange zero net active power with the ac side over one or several fundamental periods; hence, the cell capacitor voltages are maintained around the desired set point $V_{\rm dc}/N$, where $N$ is the number of cells per arm. Normally, the modular converter cell capacitors are rotated based on arm currents polarities, to ensure capacitor voltage balancing. The presence of the common-mode dc component in the arm currents represents a major concern as it increases converter semiconductor losses [45]–[55].

Also, the ac fundamental current flow through the cell capacitors increases their energy storage requirements; thus, relatively large cell capacitances are needed [42]. The device issues influence modular converter viability from the perspective of efficiency and footprint. Additionally, the half-bridge modular converter does not inherent the ability to block current in-feed from the grid during a pole-to-pole dc fault, which necessitates increased sizing of arm inductances (together with interfacing transformer leakage inductance) to effectively limit the dc fault current. This further influences the cell capacitor size needed to limit the capacitor voltage ripple within the 10% range necessary to avoid a negative impact on the control system cross-modulation.

## III. Quasi Two-Level Operation of a MMC

In this paper, each modular converter in the dc transformer of Fig. 1 is operated in Q2L mode where the cell capacitors of the MMC are used for short periods, $T_d$, only to

$$V_{\rm arm} = \begin{cases} \displaystyle\sum_{i=0,1\ldots}^{N-1} \frac{V_{\rm dc} - V_l}{N}\left[u\left(t - iT_d - \frac{k}{f_s}\right)\right], & \frac{k}{f_s} \le t < \frac{k}{f_s} + (N-1)T_d \\ V_{\rm dc} - V_{lc}, & \frac{k}{f_s} + (N-1)T_d \le t < \frac{k}{f_s} + \frac{1}{2}T \\ V_{\rm dc} - V_{lc} - \displaystyle\sum_{i=0,1\ldots}^{N-1} \frac{V_{\rm dc} - V_l}{N}\left[u\left(t - \left[\frac{1}{2}T + iT_d + \frac{k}{f_s}\right]\right)\right], & \frac{k}{f_s} + \frac{1}{2}T \le t < \frac{k}{f_s} + \frac{1}{2}T + (N-1)T_d \\ 0, & \frac{k}{f_s} + \frac{1}{2}T + (N-1)T_d \le t < \frac{k}{f_s} + T \end{cases}$$

$$\text{where} \quad t_o = \frac{k}{f_s}, \quad k = 0,\ 1,\ 2, \ldots, \infty \tag{2}$$

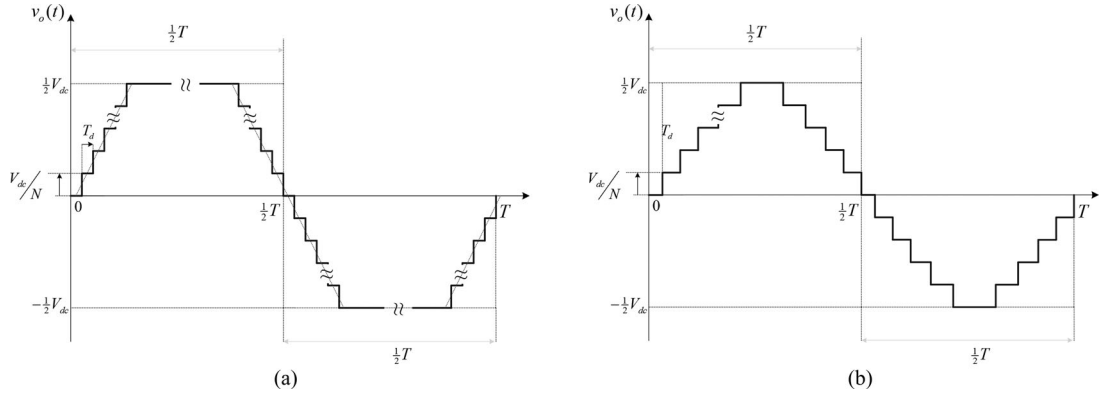


Fig. 2. Phase output voltage measured relative to virtual dc-link midpoint for (a) quasi two-level mode, and (b) conventional mode.

facilitate orderly stepped transitions between voltage levels $\pm\frac{1}{2}V_{\rm dc}$ through intermediate cell voltage levels (see Fig. 2). The dwell time $T_d$ spent at each intermediate cell voltage level is sufficiently small to reduce the energy storage requirement per cell capacitor for a given voltage ripple value, and must remain compatible with the switching ability of high-voltage insulated gate bipolar transistors. Also, the value of $T_d$ must be large enough to avoid unacceptable voltage derivative *dv/dt* levels and eliminate higher harmonics from the output voltage waveform. These harmonics, otherwise, bring about additional losses in the coupling transformer as they do not engage in power transfer.

In this manner, each phase in the Q2L modular converter of the dc transformer generates a step approximation of a trapezoidal ac voltage with predefined voltage steps equal to one cell capacitor voltage $(V_{\rm dc}/N)$, with a total transition time between $\frac{1}{2}V_{\rm dc}$ and $-\frac{1}{2}V_{\rm dc}$ of $2(N-1)T_d$ per fundamental cycle, where $N$ is the number of cells per arm. The dwell time at each cell voltage level is sufficiently small so that the time $2(N-1)T_d$ is much smaller than the fundamental period $T$. During the nontransitional times, the ac poles of the Q2L converter will be directly connected to the dc rails. This means the MMCs of the dc transformer effectively operate similar to two-level converters. That is, current flows separately in each arm per leg for a period $\frac{1}{2}T-(N-1)T_d$ of the fundamental half-cycle. Only during brief periods when the cell capacitors are successively switched, both upper and lower arms of the Q2L converter simultaneously conduct currents to the ac input as in true multilevel operation of an MMC. Therefore, the proposed Q2L mode eliminates the common-mode dc component normally present in the arm currents of a conventional MMC. Consequently, lower semiconductor losses are expected. Furthermore, small cell capacitances are required for the quasi two-level mode, since they are only loaded for a small fraction of the fundamental cycle, where smaller arm inductances are sufficient to limit inrush currents associated with cell switching.

As in the conventional MMC, the inserted cell voltages in each phase leg must sum to the dc voltage minus the arm inductances voltage drop. Over one fundamental cycle starting at $t = t_o$, the voltage of one converter arm in the Q2L mode can be expressed as in (2), at the bottom of the previous page.

The voltage of the other arm, in the same leg, is the complement. The arms of other legs in a three phase Q2L converter exhibit the same voltage waveform, phase-shifted accordingly. In (2), $V_l$ is the voltage drop in both arm inductances, whereas $V_{lc}$ is the inductance drop in the complementary arm. Proper Q2L mode operation can be achieved with minimal arm inductance, with circuit stray inductance being sufficient, as will be shown. Therefore, the inductance voltage drop in (2) can be neglected.

In the converter controllers, (2) can be realized by dividing the real-time value of a trapezoidal function of the fundamental frequency at slopes $\pm V_{\rm dc}/(N-1)\,T_d$ by the voltage step $V_{\rm dc}/N$. Rounding the result to the closest integer brings about the number of active cells per arm.

In the proposed operating mode, the fundamental voltage output is

$$V_{m1} = \frac{2V_{\rm dc}}{\pi}\frac{\sin\alpha}{\alpha} \tag{3}$$

where $\alpha = {}^1\!/_2\omega\,(N-1)\,T_d$, and $\omega$ is the fundamental frequency in rad/s. This corresponds to a modulation index of

$$m_1 = \frac{V_{m1}}{\frac{1}{2}V_{\rm dc}} = \frac{4}{\pi}\frac{\sin\alpha}{\alpha} \tag{4}$$

This expression shows that the trapezoidal voltage fundamental of the modular converter, present to interfacing ac transformer when operated in Q2L mode, tends to that of the square waveform, provided $\alpha\rightarrow 0$

$$m_1 = \frac{4}{\pi}\lim_{\alpha\to 0}\frac{\sin\alpha}{\alpha} \approx \frac{4}{\pi} \tag{5}$$

Additionally, most of the dominant low-order harmonics such as the third, fifth, and seventh can contribute to the power transfer, as will be presented.

Although the dwell time is assumed constant for each transition step between $\pm\frac{1}{2}V_{\rm dc}$, it can be varied so as to minimize the higher order harmonics (e.g., 17th, 19th, etc.) which contribute little to power transfer but are increasingly likely to be absorbed as losses in the bandwidth limited transformer iron core.

Different operational aspects and parameters of the proposed Q2L mode are illustrated using MATLAB/Simulink® to simulate a basic test case where an open-looped Q2L converter feeding a resistive load of 450 MW (0.99 lagging pf) is connected to an ac grid via an HVDC link of $\pm$320 kV.

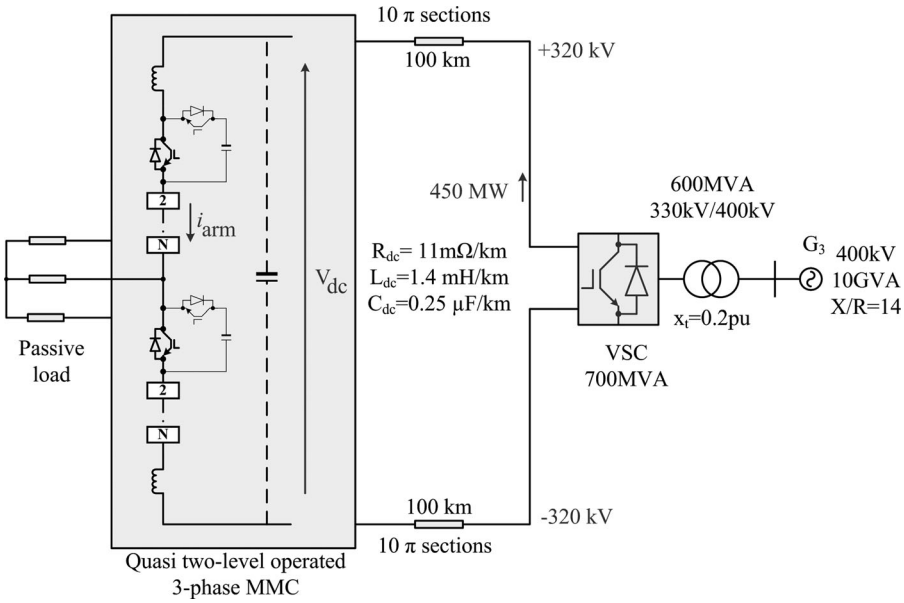


Fig. 3. Test system for the proposed quasi two-level modular converter.

Control of the ac grid-side converter is presented in Section VII. For expedience, the converter comprises ten cells per arm. A dwell time of $T_d = 5$ $\mu$s gives a 45 $\mu$s transition time between the two main voltage levels ($\frac{1}{2}V_{\rm dc}$ and $-\frac{1}{2}V_{\rm dc}$), which is 1/90 of the fundamental cycle at 250 Hz. The test system parameters are depicted in Fig. 3.

Various current and voltage waveforms are shown in Fig. 4. Subplot 4c depicts the load phase voltage peaking at $\frac{2}{3}$ the dc-link voltage while subplot 4d shows the phase voltage to the virtual dc-link midpoint, peaking at half the dc-link voltage. The gradual transition between the two voltage levels $\pm$320 kV is realized in ten steps, where cell capacitor voltages remain balanced with less than 0.3% peak-to-peak ripple around 64 kV [see Fig. 4(b)]. This low ripple is achieved with cell capacitors as small as 50 $\mu$F, which is significantly smaller than the corresponding cell capacitance for conventional MMC operation at comparable voltage and power levels. Such a low-voltage ripple indicates that the cell capacitance can be further reduced to give $\pm$10% ripple, which is a widely accepted figure for conventional MMCs. For the operating conditions in Fig. 3, cell capacitance of only 1 $\mu$F achieves $\pm$6% voltage ripple. However, with smaller cell capacitance, the dc current ripple increases.

Generally, cell capacitor sizing depends on voltage and power levels as well as the number of cells per arm; that is, it is application-specific. As a compromise, 50-$\mu$F cell capacitance is selected for the systems analyzed in this paper. A higher number of cells per arm and/or faster transition between intermediate voltage levels further reduces the cell capacitance requirement as each capacitor supports the voltage for a shorter period. However, this may be impeded by practical limitations.

For expedient comparison with the conventional MMC, the cell energy requirement in kJ/MVA is compared for the proposed Q2L converter with that of the 401-level MMC, $\pm$320 kV, 1059 MVA application in [52]. Therein, it was concluded that a 10 mF cell capacitor is needed to achieve 30 kJ/MVA, which is the energy level typically required for conventional MMC operation within $\pm$10% cell voltage ripple [53]. This figure is calculated from

$$E_{\rm cell} = \frac{3CV_{\rm dc}^2}{NS} \tag{6}$$

where $E_{\rm cell}$ is cell energy in kJ/MVA, $S$ is the total power in MVA, and $V_{\rm dc}$ is the pole-to-pole dc voltage in kV. If the same MMC converter is operated in the Q2L mode with a 50-$\mu$F capacitor per cell, the energy requirement, according to (6), drops to 0.145 kJ/MVA (with voltage ripple below 1%) which is less than 0.5% of the energy requirement for the conventional MMC. This confirms a drastic reduction in cell volume when operated in the Q2L mode.

The cell voltages are balanced with the same principles used in the conventional MMC [56]. During phase voltage transition, cell capacitors per arm are switched into or out of the circuit conduction path in an order dictated by their individual voltage magnitudes and arm current directions. This ensures the capacitors are rotated with their voltages remaining within an allowable voltage ripple band.

The voltage ripple is further reduced since, when switched in the circuit, cell capacitors have ideally no current flow, excluding the brief voltage transition periods between $+\frac{1}{2}V_{\rm dc}$ and $-\frac{1}{2}V_{\rm dc}$. This implies that the load current always flows in the arm which has its cells in the off state, as long as the respective ac pole is at one of its two main voltage levels (note the positive arm current direction in Fig. 3).

During an ac pole transition, output phase current is shared between the upper and lower arms as cell capacitors of both arms switch in complementary pattern. At the same time, the difference between the dc-side voltage and the sum of cell voltages in each leg, results in limited inrush current acting to establish voltage balance. The net result is a limited common-mode current whenever the load current commutates between the upper and lower arms of each phase leg, as observed in Fig. 4(e). This is why the aggregate voltage drop on both the upper and lower arm

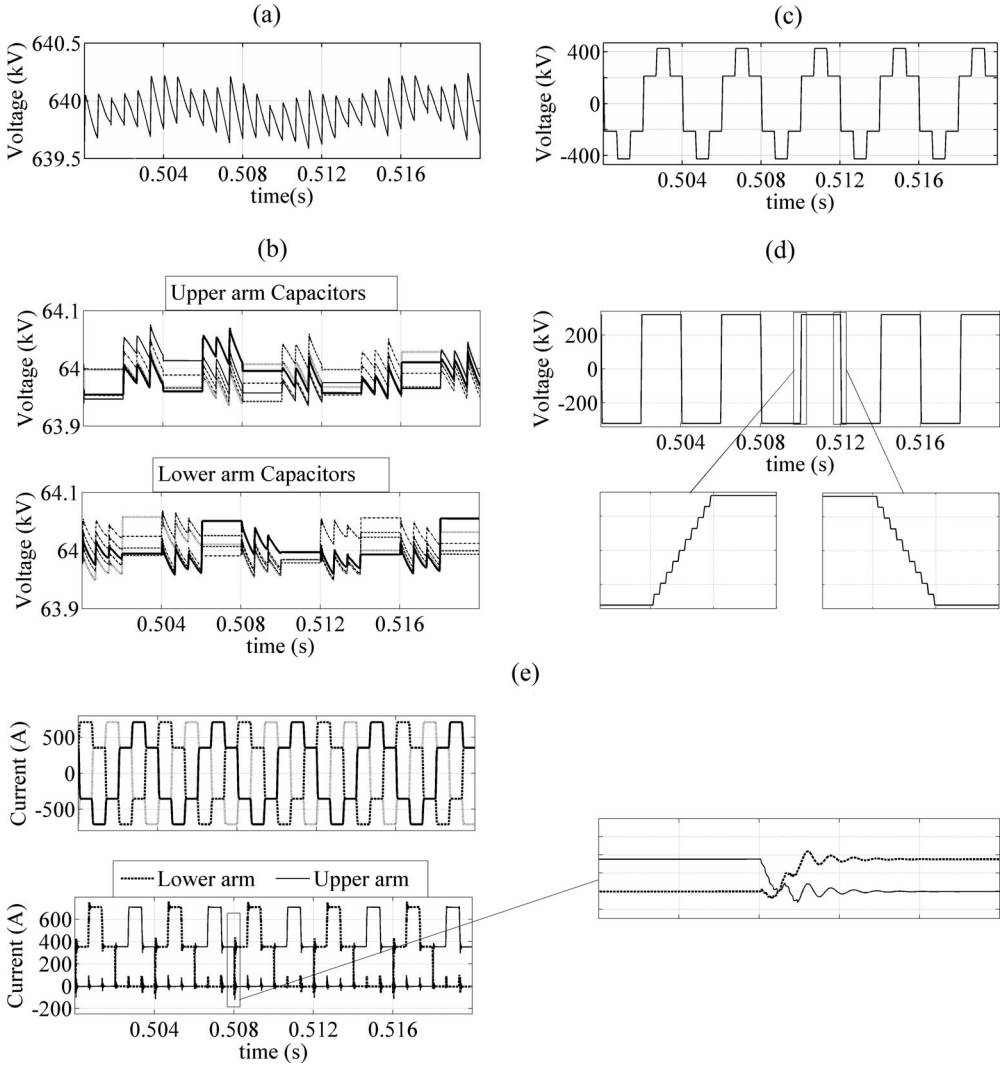


Fig. 4. Voltages and currents of the quasi two-level modular converter in Fig. 3. (a) DC-side voltage (kV). (b) Cell capacitor voltages of five cells in each arm of phase A leg. (c) Phase voltage (phase $A$). (d) Phase $A$ voltage relative to a virtual dc-link midpoint. (e) Three phase load currents (upper right), and upper and lower arm currents of phase $A$ (lower right).

inductances was considered during voltage transition periods in (2). As in conventional MMC operation, this common-mode circulating current neither diverts to output ac phase current nor reflects in the ac-voltage waveforms. This transient is mitigated by arm inductances.

For the considered case study, 5-$\mu$H inductance per arm was found to acceptably mitigate the common-mode current [see Fig. 4(e)]. In an actual system, this would be the stray inductance of the circuit. Higher arm inductance values produced longer current oscillations due to the small cell capacitances. In-depth study and mathematical quantification of this issue may need to be considered in a separate device-oriented context.

A dc-voltage ripple at the Q2L converter terminals, at triple the fundamental frequency, can be observed in Fig. 4(a). In each leg, all cell capacitors in the conduction path, having to sum up to dc-side voltage, experience similar ripple. This triggers additional common mode arm currents twice per half cycle, as seen in Fig. 4(e). This dc-side voltage ripple is the result of dc current ripple.

Unlike two level square wave operation where dc current is almost ripple-free in steady state, the introduced intermediary voltage levels in Q2L operation produce brief dc current dips of significant magnitude whenever current commutates between the arms of any phase leg (six times per fundamental cycle). In practice, the application of the Q2L modular converter in a dc transformer involves long dc cables. The distributed capacitance and inductance of a dc cable inherently bypasses and damps the dc current ripple along cable length. Fig. 5 indicates that only 2% current ripple (15 A peak-to-peak) is seen at the grid-side end of the 100-km HVDC line, with each dc cable modeled as ten consecutive $\pi$ sections. At the Q2L converter end, the first few kilometers of each dc cable are modeled as inductance in series with a resistor to account for their negligible equivalent capacitance as seen by the Q2L converter. When a dc filter (500-$\mu$F capacitor) is installed across the dc rails of the Q2L converter in the example of Fig. 3, the triple load frequency cell voltage ripple and arm inrush currents are mitigated. The larger the filter capacitor, the smaller the dc voltage and current ripples at the

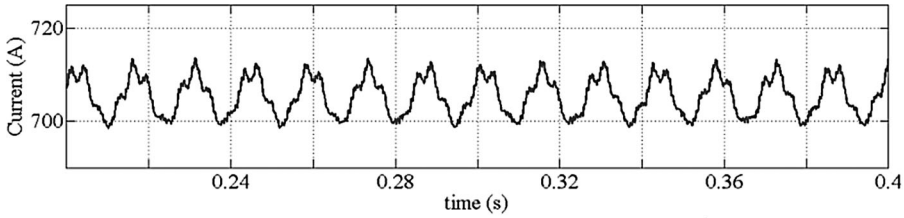


Fig. 5. DC current at the grid-side converter in the example of Fig. 3.

Q2L converter terminals. With a perfectly stiff dc source, these would be totally eliminated.

Despite being fairly a short line, the distributed parameters of the 100-km HVDC cables are clearly sufficient to assure satisfactory operating conditions for both load and grid, without any discrete dc filters. Longer HVDC cables will further alleviate dc voltage and current ripples. However, in applications where the Q2L converter is connected directly to a nonstiff dc source, or connected to low-capacitance dc line (e.g., overhead HVDC lines), discrete dc-link filter and/or increased size of cell capacitance may be needed.

The presence of a load current commutation transient in phase arms, in principle, may affect the soft-switching characteristics of some cells. However, the potential impact of common-mode arm currents on switching losses is expected to be outweighed by the alleviated conduction losses due to the higher fundamental output voltage, as described in (3)–(5), as well as the absence of the common-mode dc component and additional harmonics in arm currents.

The calculation method presented in [57] is used to quantify the conduction loss of the Q2L converter relative to a conventional MMC. It was presented in [57] that a three phase 17-level MMC with 20-kV dc voltage supplying an 11-kV load at 0.8 lagging power factor has around 0.85% (170.8 kW) conduction losses. For a three-phase 16 cell-per-arm Q2L converter with 20-kV dc supply, the power output of the 50 Hz fundamental voltages and currents being 20 MVA at 0.8 lagging power factor, the conduction losses are 0.51% (102.05 kW). The same 3.3-kV IGBT module was used for both cases, with parameters given in [57].

## IV. Operation and Control of the Proposed DC Transformer

### A. Operation and Topologies

The connection of two Q2L converters through a coupling ac transformer creates a type of DAB topology, which is recognized as a potential arrangement for high-power applications. The coupling transformer is responsible for voltage matching. Unlike other DAB proposals, a high-frequency coupling transformer is not considered. As pointed earlier, the switching speed of state-of-the-art power electronic devices, at ultrahigh voltage and power transfer levels, is not expected to exceed a few hundred Hz, mainly due to switching losses and gating characteristics (long delay times). An operating frequency in the range of 250 to 400 Hz is considered for the proposed transformer. Selection of a fundamental frequency which is higher than the power frequency (50/60 Hz) may facilitate ac transformer design that can operate at ultrahigh voltage/power levels where parasitic component-related phenomena are to some extent mitigated.

With an appropriate coupling transformer design, the proposed Q2L converter-based dc transformer may allow power transfer at fundamental frequency plus some of the higher harmonic frequencies. Today, such ac transformer design is technically feasible, and achievable with limited modifications to core design of the conventional 50/60 Hz ac power transformers. Power transfer at frequencies up to 2000 Hz implies that the third, fifth, and seventh harmonics of a 250 Hz fundamental voltage waveform engage in power transfer rather than inducing large iron losses in the core. This is a necessary step forward for a high-efficiency dc transformer that may be comparable to ac power counterparts. Additionally, the claimed smaller size of a high-frequency transformer cannot be fully exploited because at applicable ultrahigh voltages, the physical clearance needed for mounting large transformer bushings is limiting; hence, critical. Generally, because of these high voltage creepage and clearance requirements, a transformer operating at a few multiples of the utility frequency is only expected to be slightly smaller than a conventional 50/60 Hz ac power transformer. Thus, there is no footprint gain in significantly increasing the operating frequency.

Consequently, the proposed dc transformer may have restricted potential as an offshore installation. This is traded for the galvanic isolation and high efficiency offered by the ac transformer at such a frequency range. Further assessment of the transformer design and characteristics is not within the scope of this text.

In the proposed dc transformer, the two Q2L converters act as voltage sources coupled through interface impedance. Conceptually, bidirectional power flow is possible. The direction and amount of power flow in this case is theoretically administered by controlling the phase angle between the developed voltage space vectors, as well as vector magnitudes. Traditionally, DAB assemblies control both power flow direction and amount mainly by the polarity and magnitude of the phase shift angle, respectively [38], [39]. This is due to their limited capability of controlling voltage magnitudes, especially three-phase designs. Employing Q2L converters introduces the capability of controlling the fundamental voltage magnitudes due to the modular multilevel design. Moreover, selective harmonic elimination is a possibility. This brings about additional degrees of freedom for the proposed dc transformer to control power

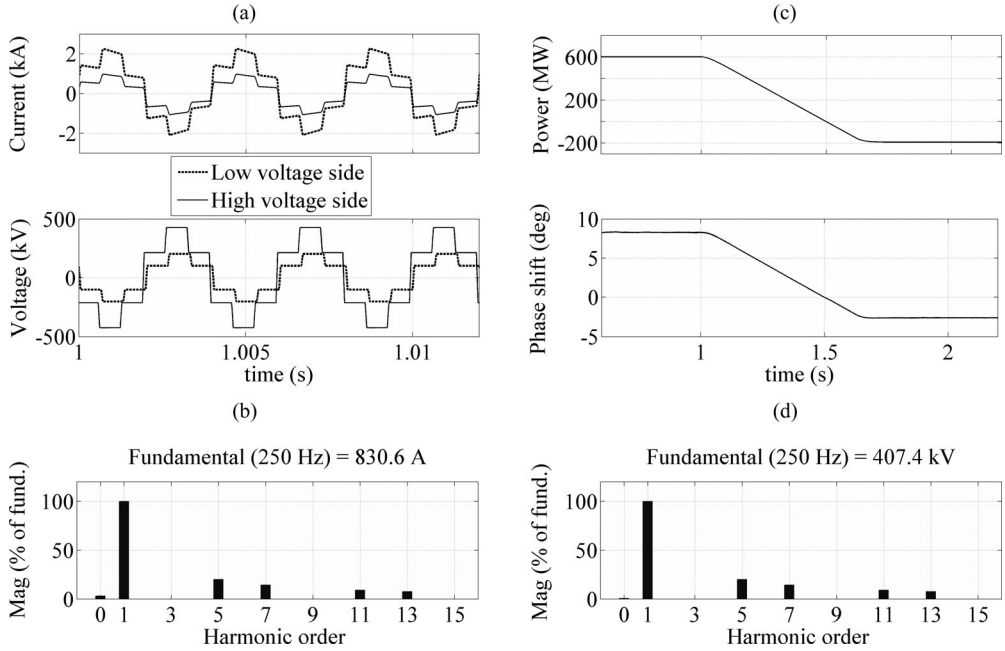


Fig. 6. Plots for normal operation of the monopolar dc transformer topology in Figs. 1 and 7(a). (a) Phase *A* transformer windings currents and voltages. (b) FFT analysis of phase current (HV side). (c) Power flow, and phase angle lead of the high voltage side converter. (d) FFT analysis of phase voltage (HV side).

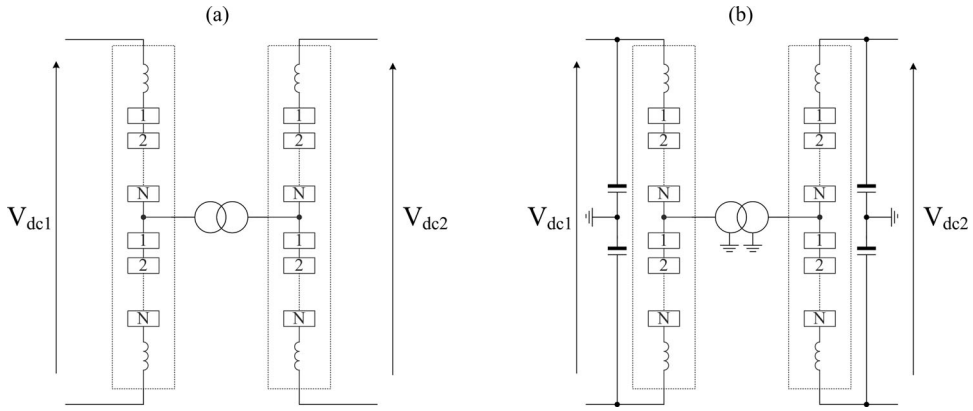


Fig. 7. Possible monopolar arrangements of the proposed bidirectional dc transformer. (a) Symmetrical monopolar arrangement. (b) Symmetrical configuration with both ac and dc sides grounded.

flow and provide voltage regulation. In this paper, only phase angle control is considered.

To investigate transformer operation, two three-phase Q2L converters are connected to form the monopolar arrangement in Fig. 1. The high-voltage converter operates at ±320-kV dc, whereas the low-voltage side operates at ±150 kV. The coupling ac transformer is modeled as an ideal transformer, with the required turns ratio, in series with 10% impedance (700 MVA base). At this stage, without any external control action, suitable phase angle values are commanded to alter power flow from 600 MW, injected into the ±150 kV side, to around 190 MW in the reverse direction. Fig. 6 presents a view of transformer winding voltages and currents, as well as phase angle and power flow. As observed, a limited phase angle change is needed. When power flows into the ±150 kV side, winding voltages of the ±320 kV side lead those of the ±150 kV windings. FFT analyses of the phase voltage, line voltage, and current [see Fig. 6(c) and (d)] show that triplen harmonics are absent. Thus, in practice, power transfer will not involve the third and ninth harmonic power even when transformer core design permits.

Low-order triplen harmonics can be made to contribute to power transfer when the topology is modified as in Fig. 7(b). For each transformer side, providing a closed path between the neutral point of the respective ac transformer windings and the dc-link midpoint lowers the phase voltage peak; hence, current peak. Effectively, the developed path permits the flow of zero-sequence currents associated with triplen harmonics.

The flow of triplen currents reshapes the resultant current waveform (see Fig. 8). Particularly, the third harmonic has one reverse-polarity peak exactly at the middle of the fundamental half cycle and two peaks of the same polarity as the fundamental half cycle, near its sides. Being of significant magnitude (around 1/3 the fundamental current magnitude), the third harmonic flattens the phase current waveform at three-fourth its former peak. Consequently, IGBTs of lower current rating could be utilized in the converter modules. However, the expense of current rating

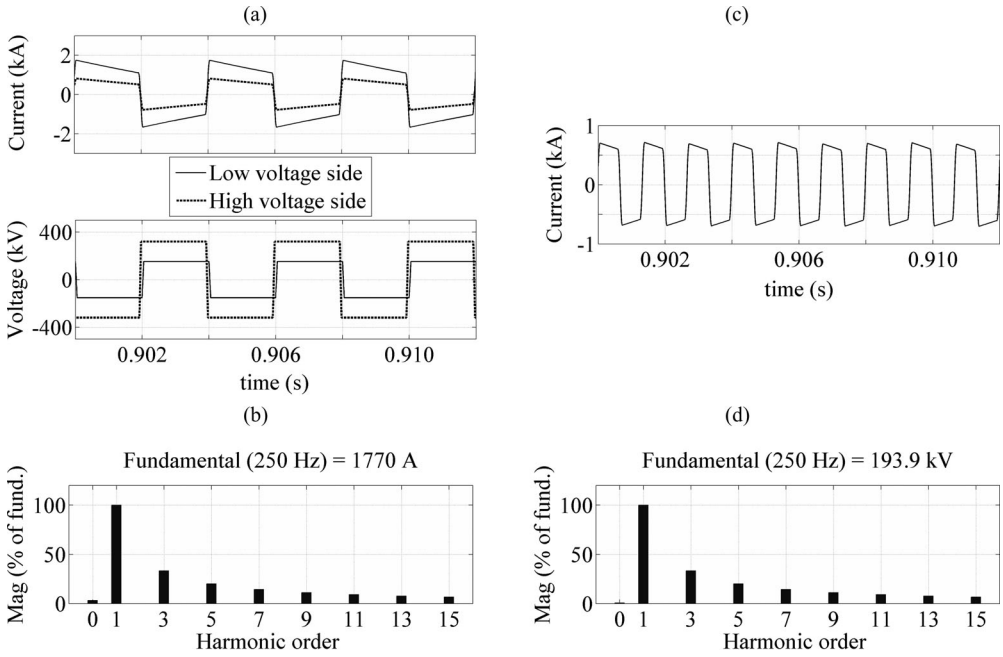


Fig. 8. Plots for steady-state operation of the monopolar dc transformer topology of Fig. 7(b) (with split capacitors) [same simulation scenario as in Fig. 6]. (a) Phase $A$ transformer windings currents and voltages. (b) FFT analysis of phase current (LV side). (c) Zero-sequence current of the high voltage side. (d) FFT analysis of phase voltage (LV side).

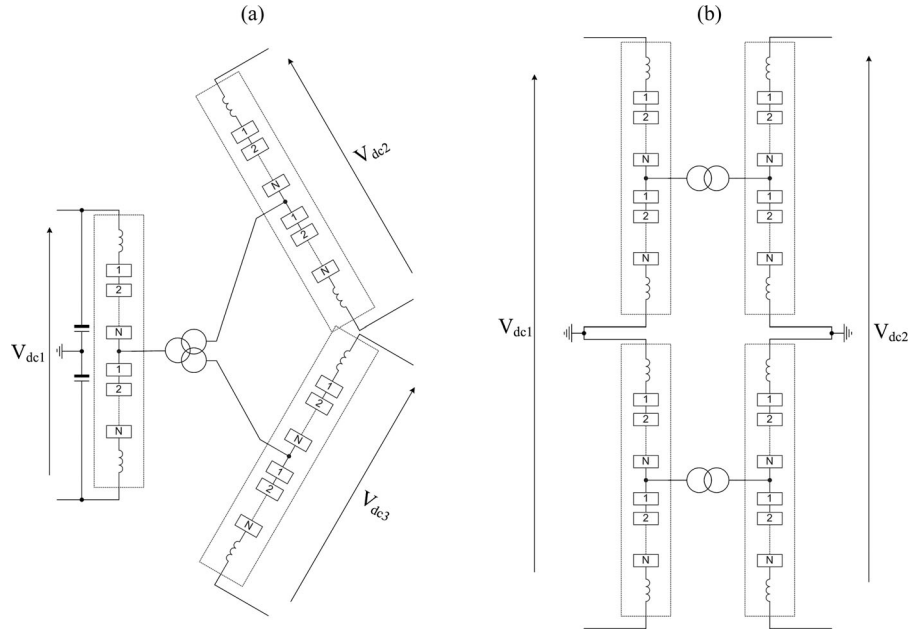


Fig. 9. More complex configurations of the proposed dc transformer. (a) Three terminal topology connecting three different dc levels. (b) True symmetrical bipolar arrangement.

curtailment is the installation of high-voltage split capacitors (a few microfarads each) between the dc rails of each Q2L converter, where it has been shown in Section III that discrete dc-link capacitors are not mandatory for dc-transformer operation. This implies the sufficiency of a small discrete dc-side capacitance, just to provide the grounding point. The midpoint of the each dc-link capacitor and respective transformer winding neutral point can be tied to ground or hard-wired.

The Q2L converter's inherent capabilities of voltage magnitude manipulation and selective harmonic elimination enable its utilization in more complex dc-transformer topologies, as for the three-terminal transformer topology shown in Fig. 9(a). It incorporates a three-winding ac transformer and three Q2L inverters for the connection of three dc lines at different voltage levels. Power flow control in this topology can be achieved only through combined control of both voltage magnitudes

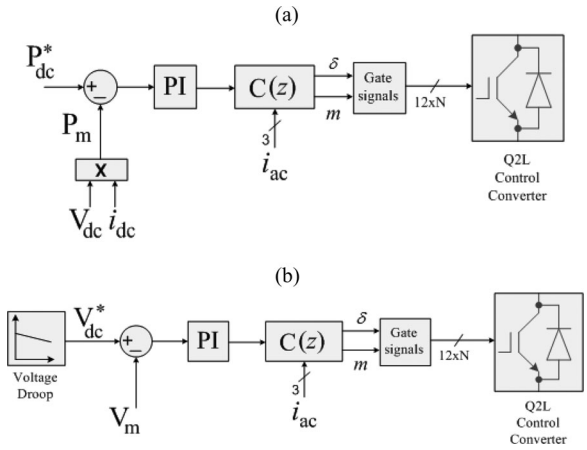


Fig. 10. Generic control algorithm for the control converter of the proposed dc Transformer. (a) Power flow control. (b) DC voltage control.

(modulation indices) and phase displacements. When a fault occurs at any of the three lines, the transformer (in conjunction with ac CBs) isolates it immediately with power flow through the other two lines unaffected. Fault protection capabilities of the proposed topologies are detailed in Section IV-C. A symmetrical bipolar arrangement is depicted in Fig. 9(b).

### *B. Steady-State Control*

In remaining within the main scope of the paper, the phase angle between the fundamental voltage space vectors of both converters is the only degree of freedom considered for transformer control (no voltage magnitude modulation has been incorporated at this stage).

Bidirectional power flow control can be achieved by setting the voltage phase angle of one Q2L converter as the reference (i.e., zero angle) and control acts upon the phase angle of the other Q2L converter to control the power flow through the transformer. The former converter is denoted as the *'reference converter*' and the latter the '*voltage/power control converter*', depending on what parameter it controls. In a power-control mode [see Fig. 10(a)], the power reference $P^*_{\rm dc}$ is compared to the measured power and the error signal is fed to a PI controller. The PI output is forwarded to a fast current controller which produces the required phase angle ($\delta$) and voltage modulation index ($m$). Fast current control is important for a fine-tuned transient operation and to compensate for any asymmetry in transformer parameters. In this paper, the discrete transfer function of the fast current control block is set to $\mathrm{C}(z) = 1$ and the modulation index is fixed to $m = 1$. AC transformer asymmetry is neglected, and detailed control design including fast current and transient control transfer function $\mathrm{C}(z)$ is beyond the scope of this basic demonstration.

In the dc-voltage control mode, the outer power control loop is replaced with a voltage control loop, as in Fig. 10(b), where the dc voltage reference $V^*_{\rm dc}$ is produced by a droop controller or commanded by the operator (the output of a load flow scenario). In both control modes (the dc voltage or active power), reactive power required by the ac transformer is shared between both converters, depending on $\delta$ and $m$.

### *C. Operation Under DC Line Fault*

When a two-level or modular multilevel VSC undergoes a dc fault, the fault absorbs large current from the ac side once the dc voltage drops below the ac line voltage peak. Such uncontrolled rectifier action is unavoidable in a Q2L converter with half-bridge cells during a dc line fault. The proposed fault protection scheme utilizes the dc transformer configuration to deprive the fault-side Q2L converter of energy input. That is, whenever one of the two Q2L converters senses current rise above a predefined threshold (e.g., 1.2 pu), all IGBTs of the other converter are immediately blocked (in the order of several microseconds for high-power IGBTs). This truncates energy in-feed to the ac transformer. As the ac transformer leakage inductance has negligible stored energy, the fault loses its energy in-feed from the dc transformer line terminal. Effectively, the fault and the fault-side Q2L converter become isolated from the healthy line on the other side of the transformer. The galvanic isolation provided by the ac transformer prohibits fault propagation from one side to another even if one converter fails. Additionally, ac CBs can be used at each side of the transformer, acting in a disconnector mode. If, at fault inception, the fault-side Q2L converter is not blocked, all cell capacitors will discharge into the fault. The small cell capacitors do not store a significant amount of energy, and their contribution to fault current will be insignificant. However, blocking the fault-side converter to retain its cell capacitor voltages serves for a smoother line restoration. With the topology of Fig. 7(b), the split capacitor fault contribution is also insignificant due to its small size.

Once the fault is cleared, or isolated, Q2L converters can contribute to system restoration due to their black-start capability. DC transformer action depends on the prefault operating mode of the fault-side converter:

1) *Voltage control converter*: The fault-side Q2L converter reenergizes the dc line where the dc voltage command ramps up from zero with an adequate slope to avoid transients and large inrush currents.
2) *Reference converter or power control converter*: The line is first energized by the other terminal converter station; the dc transformer power command is ramped up (e.g., at a rate imposed by the grid operator).

The converter control flexibility allows for additional maneuvering during postfault system restoration, if required. In the three-terminal dc-transformer topology [see Fig. 9(a)], upon a fault in the dc side of one Q2L converter, the IGBTs of the other two converters (or all three converters) are blocked; stopping current flow into the fault. Immediately, the ac CB poles of the fault-side converter are opened and the other two converters instantly resume operation. The operational restart procedure depends on the opening time of the ac CBs and the dc-link time constant.

## V. Three-Terminal DC Test System

Fig. 11 shows the test network used to assess the capabilities of the proposed high-power dc transformer under normal and transient conditions. In this three-terminal illustrative network, a main high-voltage dc line $\mathrm{B}_1-\mathrm{B}_2$ of $\pm$600 kV is connected

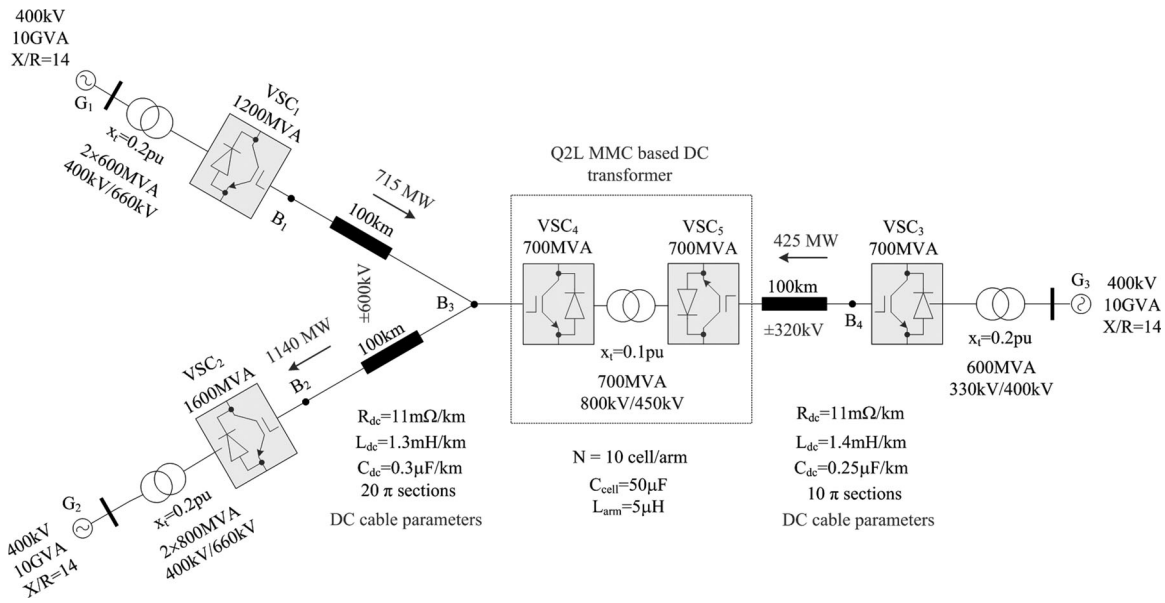


Fig. 11. Three terminal dc test system.

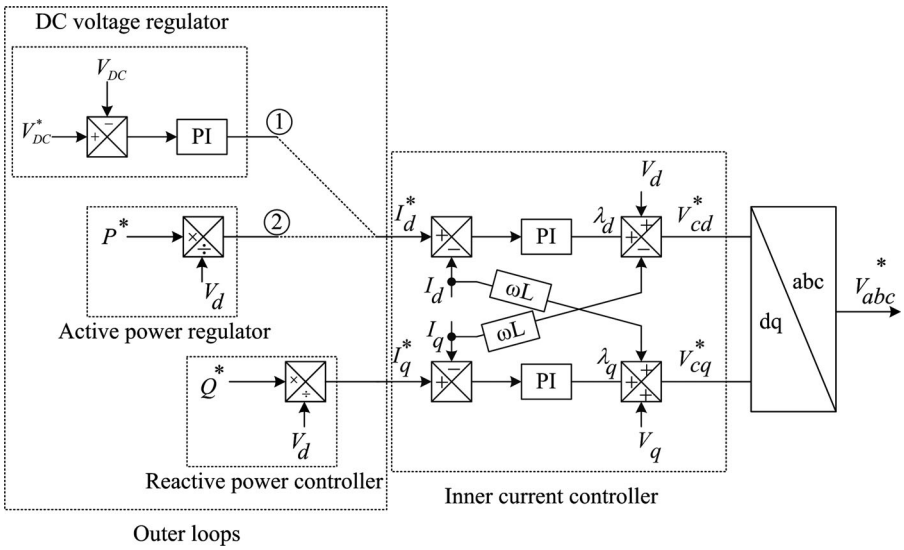


Fig. 12. Generic block diagram illustrating control systems of the grid-side converter terminals (refer to [58]–[60]).

at point $B_3$ to a $\pm$320 kV dc line through the proposed dc transformer. Terminal grid-side converter stations $VSC_1$, $VSC_2$, and $VSC_3$ are modeled as half-bridge MMCs, with all their basic controllers incorporated (see Fig. 12).

For the $\pm$600 kV dc line, $VSC_2$ is configured to regulate the voltage at $B_2$, while $VSC_1$ controls active power and ac voltage at busbar $B_1$; therefore, $VSC_2$ is rated at 1600 MVA, higher than $VSC_1$. For the $\pm$320 kV line, $VSC_3$ controls active power flow and ac voltage magnitude at $B_4$, whereas dc-voltage control is administered by the dc transformer control converter $VSC_5$. The other Q2L converter $VSC_4$ is the reference converter. To ensure that the harmonic requirements are met at $B_1$, $B_2$, and $B_4$, converter terminals $VSC_1$, $VSC_2$, and $VSC_3$ are operated in typical multilevel mode, with sinusoidal pulse-width modulation. Each Q2L converter in the dc transformer station has a 20-$\mu$F split capacitor connected across the dc rails, hardwired to the respective transformer winding neutral point, which is grounded. System parameters are shown in Fig. 11.

## VI. Performance Evaluation

### A. Steady-State Operation

In the system described in Section V, the simulation scenario is where power flows in the lines are 425 MW over line $B_3-B_4$, 715 MW over line $B_1-B_3$, and 1140 MW over line $B_3-B_2$, with directions shown in Fig. 11. In steady-state, the simulated grid has stable line voltages and steady power flows between all busbars. At $t = 1.7$ s, $VSC_3$ curtails the power injected to the grid at point $B_4$ down to 355 MW within 0.4 s. Fig. 13 shows the dc-grid response to the power reference change at $VSC_3$. The dc-voltage controllers quickly regulate the dc voltage at each line with brief 0.03% and 0.025% dips in the $\pm$320 kV and $\pm$600 kV

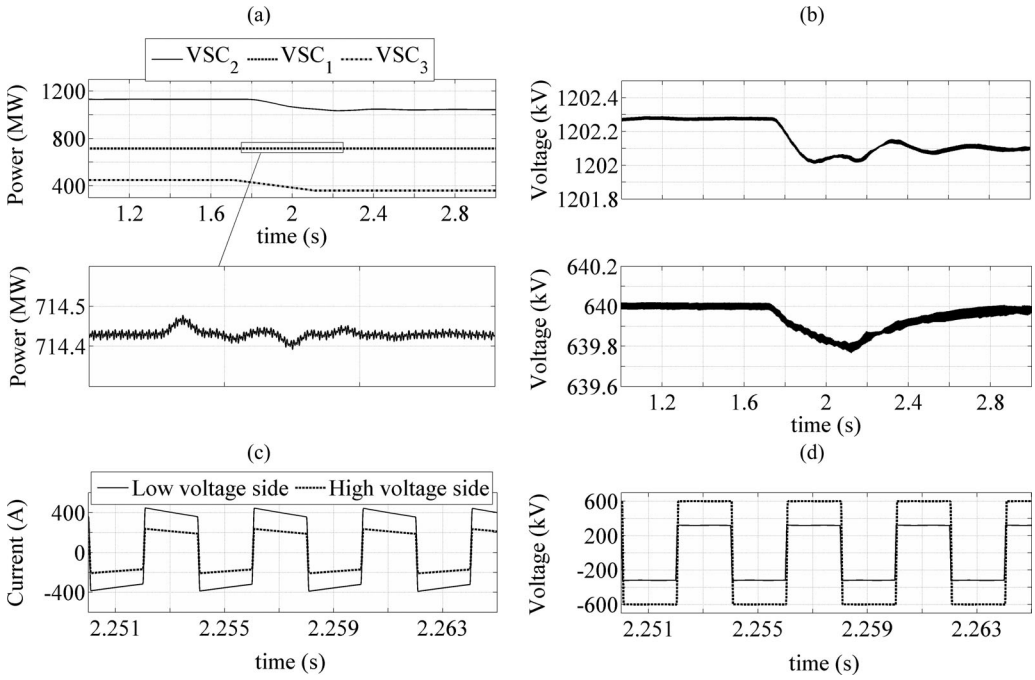


Fig. 13. Performance of the test system in Fig. 11 with a 16% drop in the power flow through the ±320 kV line. (a) Power flows in the grid. (b) DC line voltages at dc transformer sides (pole-to-pole). (c) Steady-state dc transformer winding currents (phase *A*). (d) Steady-state dc transformer winding voltages (phase *A*).

dc voltages lines, respectively. The created power imbalance is taken up smoothly and the grid returns quickly to steady state operation at a new operating point. In Fig. 13(b), both voltages are measured close to dc terminals of the dc transformer station.

### *B. DC Fault Ride-Through*

A simulated fault scenario is when the test three-terminal dc grid of Fig. 11 encounters a pole-to-pole fault, at $t = 1.5$ s, in line $B_3-B_4$ at a distance of 3 km from the dc transformer station. Each grid-side converter station is equipped with ac CBs which are modeled to open the circuit at the first ac current zero crossing after the dc side current exceeds 120% of the station's dc current rating. The slow mechanical time constant of an ac CB is considered, with a 40 ms delay in tripping action modeled for every AC CB. At 120% dc current, each grid-side converter blocks its switches. Similarly, the dc transformer is equipped with an ac CB at the low-voltage side of the ac coupling transformer, as well as an off-load isolation switch at each dc side, connected between the positive dc rail and the positive pole cable.

Data collected from two simulation runs are plotted in Fig. 14. In the first run, dc transformer Q2L converters continue operation under fault without blocking their IGBTs. In this case, the fault protection, as far as the dc transformer is concerned, is the sole responsibility of its 40 ms-delayed ac CB (triggered at 120% of current rating). In the second simulation case, both Q2L converters of the dc transformer block their IGBTs 20 $\mu$s after the 120% current barrier is reached. This 20-$\mu$s delay represents the time elapsed for fault sensing and gating of the IGBTs.

In Fig. 14(b), when the dc transformer converters are not blocked, the fault current leaps to 18 kA in 4 ms, as measured from the dc transformer end. Concurrently, line $B_3-B_4$ voltage drops to zero within the same time span, as seen from dc transformer end. Both dc voltage and fault current encounter oscillations due to the distributed impedance of the line.

All cell capacitors of the control converter (fault-side converter) discharge their energy into the fault, as does the low-voltage side dc-link split capacitor. At the other end of line $B_3-B_4$, grid-side converter station $VSC_3$ encounters high-fault currents both in the ac and dc sides. Although all IGBTs of $VSC_3$ were immediately blocked, dc-fault current of 16 kA freewheels in the cell diodes until its ac CB interrupts all ac phase currents in about 42 ms. During this time, the grid-side converters at both ends of line $B_1-B_2$ do not encounter any high currents. The dc-line voltage undergoes a shallow dip mainly due to the sudden interruption of power in-feed from line $B_3-B_4$. The dc voltage regulator at $VSC_2$ rapidly restores the dc voltage, resulting in power oscillations at $VSC_2$ [see Fig. 14(a)], whereas the power flow remains near steady at $VSC_1$.

The reason that line $B_1-B_2$ is affected most by the power imbalance triggered by the fault, is the presence of the dc transformer. The reference converter, which is energized by the voltage of line $B_1-B_2$, remains in operation despite the fault, applying Q2L voltage to the transformer windings. Being counteracted by zero-voltage output from the control converter, the reference converter drives high currents in the windings of the ac transformer [see Fig. 14(d)], which are rectified in the control converter to feed the fault. These currents are almost 90° phase shifted with respect to the reference converter output voltage, as observed in Fig. 14(d). This implies that the power fed to the fault by the dc transformer is purely reactive, which agrees with the fact that no active power can be fed to a line at zero-voltage (line $B_3-B_4$). Within 40 ms, the high currents in

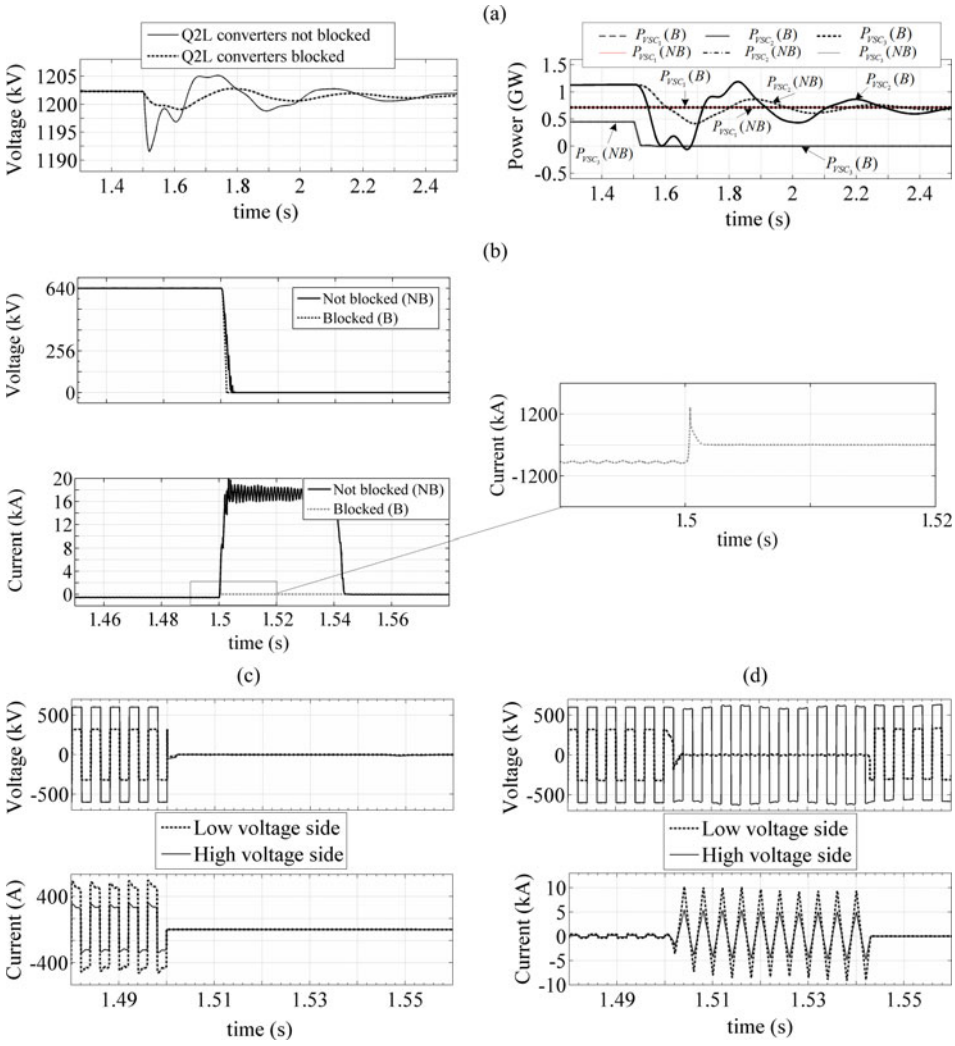


Fig. 14. System response to a fault in line $B_3-B_4$ at $t = 1.5$ s. [B: Q2L converters blocked, NB: Q2L converters not blocked]. (a) Line $B_1-B_2$ dc voltage (pole-to-pole) and power flows in the system [B: Q2L converters blocked, NB: Q2L converters not blocked]. (b) DC voltage and fault current in the faulted line (seen from the transformer end). (c) DC transformer voltages and currents when both Q2L converters are blocked. (d) DC transformer voltages and currents when both Q2L converters are not blocked.

the dc transformer are interrupted by its ac CB and the dc-fault current drops to zero.

In Fig. 14(d), low-side winding phase voltage does not actually return to its prefault level when the ac CB trips, it is rather the voltage induced by current flowing in the high-voltage windings. The net result is that the fault is confined within the downstream line ($B_3-B_4$) and the upstream line is only affected by the power imbalance and, to a lesser extent, by the circulating reactive power. However, without blocking Q2L converters, the dc transformer is exposed to destructive currents. A current controller acting on the reference converter must be included to limits these currents; otherwise the second protection scenario, where all IGBTs are blocked, becomes the only practical fault protection scheme.

When IGBTs of the Q2L converters are blocked once the dc current reaches the 120% limit, energy supply is cut from the dc transformer line end. Hence, the fault current contribution from the transformer end drops immediately to zero and currents in both transformer sides diminish [see Fig. 14(c)].

At the other end of the line, $VSC_3$ undergoes the same high currents like the previous case and is tripped out by its ac CB. The power oscillations triggered in the system by the contingency are of lower magnitude and the system migrates relatively faster to the new power balance point [see Fig. 14(a)].

It is clear that when Q2L converters of the dc transformer are blocked, a smoother fault-ride through is achieved by the protected line (line $B_1-B_2$ in this case). Note that the dc transformer effectively impedes fault propagation from one side to another, but it has no role in protecting $VSC_3$. Additional protecting devices are required for $VSC_3$ to ride-through the dc fault.

## VII. Conclusion

A quasi two-level (Q2L) operating mode has been proposed for modular multilevel converters, for utilization in a dual-active-bridge dc-transformer topology. In this mode, a modular multilevel converter offers the following merits:

1) two-level operation with controllable values of voltage derivative, *dv/dt*;
2) low cell capacitance requirement results in a considerable reduction in converter footprint;
3) lower losses due to higher fundamental output voltage and the absence of a dc common-mode component in converter arm currents, soft switching occurs owing to the dc-transformer topology;
4) beside flexibility of manufacturing and installation, the modular design results in additional output control capabilities; voltage magnitude (modulation index) control and selective harmonic elimination.

The Q2L is unable to filter out dc current ripple. Theoretically, a discrete dc-link capacitor may be needed to filter this ripple. Practically, the dc current ripple will be naturally filtered out when the Q2L converter is connected to dc cables. It was shown that the distributed impedance of a 100-km dc cable attenuates the dc-current ripple to acceptable limits. This may not be the case with dc overhead lines.

A dc-transformer topology comprising two Q2L converters connected through a coupling ac transformer (dual-active-bridge) was shown to be promising for high-power and high-voltage applications. The topology offers galvanic isolation and voltage level matching. With a low-operating frequency range (250–400 Hz), efficient ac transformers with thinner core laminations could be utilized, with low-order harmonics contributing to power transfer. Although the low-frequency range (250–400 Hz) reduces overall losses, the inevitable size of an ultrahigh voltage ac transformer may still limit the application of the proposed dc transformer to onshorelocations.

In addition to voltage matching, the proposed dc transformer is controlled normally to provide dc voltage regulation or power flow control. More importantly, it offers near instant fault isolation within a certain protection zone. At dc fault inception at one side (e.g., the secondary circuit), the proposed dc transformer instantly interrupts the fault current contribution of the healthy line, connected at the other side, by blocking all power electronic switches in both converters. Alternatively, fault currents can be limited by the current controller of the non-fault-side converter. In either case, the dc fault is seen by the healthy line as an ac fault. When the fault is cleared, the dc transformer actively participates in smoother restoration of the disconnected line.

In a generic dc grid with several power corridors and ac grid connection ports, multifunctional active components distributed around key points within the grid are necessary for protection, power flow control, dc-voltage regulation, and voltage matching. Despite cost downsides, the presented dc transformer shows promise as such a component. Further detailed studies at both system and device levels are necessary for precise evaluation of the concept presented in this paper.

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