# Optimal Low-Switching Frequency Pulsewidth Modulation of Medium Voltage Seven-Level Cascade-5/3H Inverter

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***Abstract*—Low-switching frequency modulation of multilevel inverters for medium-voltage high-power industrial ac drives is essential to reduce switching losses and, thus, improve the overall energy efficiency of the system. However, minimizing the switching frequency increases the total harmonic distortion (THD) of machine currents. Synchronous optimal pulsewidth modulation (SOP) is an emerging technique for controlling multilevel inverters at low-switching frequency without compromising on the THD of machine currents. The goal of our experiment was to implement SOP technique for controlling seven-level cascade inverter for an induction motor drive at an average device switching frequency limited to rated fundamental frequency. First, optimal seven-level waveforms were obtained by offline optimization assuming steady-state operating conditions. Then, the switching angles for each semiconductor device were obtained that ensure equal distribution of switching losses as well as minimal unbalance in dc-link capacitor voltages. The proposed SOP technique is validated by experimental results obtained from the seven-level cascade inverter feeding a 1.5-kW induction motor.**

***Index Terms*—Low-switching frequency modulation, medium voltage ac drives, multilevel inverters, seven-level inverter, synchronous optimal pulsewidth (SOP) modulation.**

## I. Introduction

MULTILEVEL converters have become popular for medium voltage high-power applications due to several advantages like reduced rating of power semiconductor devices and improved quality of output voltage waveforms [1]. The popular multilevel topologies are neutral-point or diode-clamped converters (NPC) [2], flying-capacitor converters, and cascaded H-Bridge converter. In addition, several other topologies have been proposed in the literature [3], [4]. For higher-level operation, cascaded inverters are preferred but major disadvantage is requirement of multiple numbers of dc-sources, which is not feasible in many applications. Therefore, mixed-level hybrid topology is suggested for seven-level (7L) cascade inverter that reduce the number of dc-sources to two for each phase [5].

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In high-power applications, the switching losses contribute to a major portion of total device losses and therefore, it is important to reduce the device switching frequency. It has been demonstrated by Holtz *et al.* that by reducing the switching frequency to 200 Hz (20% of conventional switching frequency), the current-carrying capability of semiconductor devices can be increased to the extent that the power rating of inverter approximately doubles [6]. On the other hand, minimizing switching frequency increases the harmonic distortion of machine currents. Therefore, the challenge is to minimize the harmonic distortion while reducing the switching frequency. A new modulation technique for operating modular multilevel converter at fundamental switching frequency while eliminating fifth harmonic was proposed [7]. A new control method for operating 7L cascaded inverter at fundamental switching frequency was proposed [8].

Offline optimization techniques are widely used for generating switching patterns for low-switching frequency operation. These techniques are used to determine finite number of switching angles per quarter fundamental period assuming steady-state operating conditions. In the beginning, selective harmonic elimination techniques are used for optimization in order to eliminate lower-order harmonics [9], [10]. However, it was found that elimination of lower-order harmonics never leads to optimal motor performance and it has been concluded that using degrees of freedom for minimization of overall harmonics is better than complete elimination of certain harmonics. In the literature, several criteria like minimizing total harmonic distortion (THD) [11] or minimizing overall motor losses [12] have been used for objective function. The goal of various objective functions is to minimize the unwanted effects of harmonics.

Synchronous optimal pulsewidth modulation (SOP) is an emerging control technique to reduce switching frequency without compromising on quality of machine currents. It consists of optimizing switching angles to minimize THD of machine currents under steady state operating conditions. SOP technique for five-level (5L) and dual three-level (3L) inverters have been demonstrated [13]–[17]. For high dynamic performance requirement applications which are subjected to frequent transient conditions, SOP along with stator flux or stator current trajectory tracking methods have been suggested [18]–[21]. The SOP technique for 7L inverter has been demonstrated by authors without experimental results [22]. Therefore, the goal of our study is to demonstrate SOP technique for controlling 7L cascade inverter for an induction motor drive at an average device switching

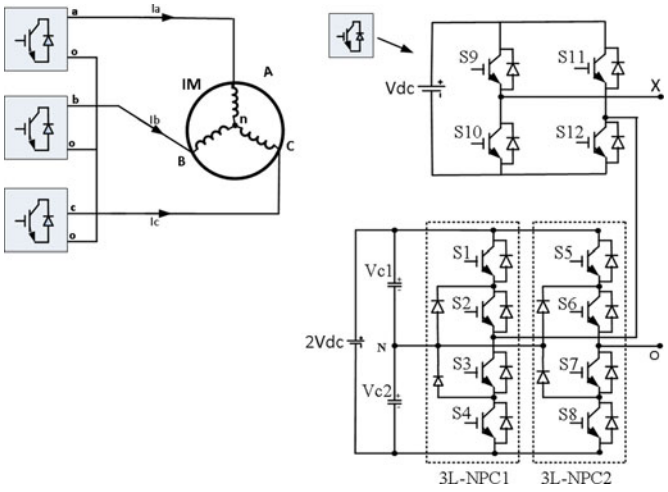



Fig. 1. Cascade-5/3H inverter fed induction motor drive.

frequency limited to rated fundamental frequency (50 Hz) in open-loop ($\frac{v}{f}$) control mode.

The topology and steady-state operation of 7L inverter is explained in Section II, analysis of SOP for 7L cascade inverter is reported in Section III, and distribution of optimal pulse patterns is discussed in Section IV. The experimental results for SOP technique controlling a 7L inverter feeding an induction motor are demonstrated in Section V to validate the proposed modulation technique.

## II. Seven-Level Cascade Inverter

### A. Topology

The 7L cascade inverter topology is shown in Fig. 1 [5]. It consists of an H-bridge connected in series with a 5L-NPC inverter and only two dc power sources are required for each phase. The dc power supply to 5L-NPC inverter is twice that of H-Bridge. The output of 3L-NPC1 ($V_{3L1}$), 3L-NPC2 ($V_{3L2}$) with respect to neutral point 'N'consists of three discrete voltage levels ($-V_{\rm dc}, 0, V_{\rm dc}$) and hence, five discrete voltage levels ($-2V_{\rm dc}, -V_{\rm dc}, 0, V_{\rm dc}, 2V_{\rm dc}$) are obtained at output terminals of 5L-NPC converter ($V_{5L}$). Similarly, the output of H-Bridge ($V_{\rm HB}$) consists of three discrete voltage levels ($-V_{\rm dc}, 0, V_{\rm dc}$). Thus, by combining output voltages of 3L-NPC1, 3L-NPC2, and H-Bridge, a 7L waveform with discrete voltage levels ($-3V_{\rm dc}, -2V_{\rm dc}, -V_{\rm dc}, 0, V_{\rm dc}, 2V_{\rm dc}, 3V_{\rm dc}$) will be obtained at the output of each phase. The switching states and synthesized output voltages for 7L cascade inverter are shown in Table I.

### B. 7L Structures

A multilevel inverter provides an additional degree of freedom in choosing the next voltage level that leads to multiple output voltage waveforms known as structures. A structure is unique in terms of sequence of output voltage levels. A 3L waveform has only one possible structure, whereas higher-level inverters have more possible structures. A structure is usually stored in the form of step transitions $s(i)$ at each switching instant, which is equal to 1 when switching to higher potential and $-1$ when switching to lower potential. Ensuring half-wave and quarter-wave symmetry in the switching pattern, it is possible to eliminate all even order harmonics. Then, it is sufficient to consider switching instants in a quarter period, known as pulse number $N$. The different possible structures for a 3L, 5L, and 7L waveforms with $N = 5$ are shown in Table II. The number of possible structures increases as number of levels and $N$ goes higher [22].

## III. Synchronous Optimal Pulsewidth Modulation

SOP is employed for generating optimal pulse patterns of a multilevel inverter by determining optimal switching angles [23]. In synchronous PWM, carrier signal at frequency ($f_s$) and sinusoidal control signal at frequency ($f$) are synchronized with each other, i.e., $\frac{f_s}{f}$ is an integer, and thus, subharmonic frequencies which are undesirable in many applications are eliminated. The goal of optimization method is to minimize the THD of inverter output currents.

### A. Optimization Problem

As THD calculations involve internal impedance of induction machine, distortion factor $d$ is used as an objective function for optimization. The expression of $d$ is given by [23]

$$d = \frac{i_h}{i_{h,\text{six-step}}} \tag{1}$$

where, $i_h, i_{h,\text{six-step}}$ represents the harmonic rms current during normal operation and six-step operation ($m = 1$ or rated fundamental frequency) of a multilevel inverter, respectively. By Fourier series analysis of output voltage waveforms, the final expression for $d$ is obtained as [22]

$$d = \frac{\sqrt{\sum_k \left(\frac{1}{k^4}\right)\left(\sum_{i=1}^{N} s(i)\cos(k\alpha_i)\right)^2}}{3\sqrt{\sum_k \left(\frac{1}{k^4}\right)}}. \tag{2}$$

where, $k$ corresponds to $k$th order harmonic ($k = 5, 7\ldots$) and $s(i)$ represents the step transition at switching angle $\alpha_i$.

Optimal switching patterns are obtained for all steady-state operating points of induction motor drive assuming constant ($\frac{v}{f}$) control. The modulation index $m$ is defined as $\frac{f_1}{f_{1R}}$, where $f_1$ and $f_{1R}$ are the variable fundamental frequency and rated fundamental frequency of input voltage to induction motor, respectively. Since the induction motor is operated at constant ($\frac{v}{f}$) control mode, the constraint on switching angles to obtain the fundamental frequency of the inverter output voltage as $f_1$ is given by

$$\frac{f_1}{f_{1R}} = \frac{u_1}{u_{1,\text{six-step}}}$$

$$3m = \sum_{i=1}^{N} s(i)\cos(\alpha_i). \tag{3}$$

In SOP, the maximum switching frequency of operation is limited to a fixed value $f_{s,\max}$ in order to reduce the switching losses of power semiconductor devices. For a 7L waveform, the

TABLE I
SWITCHING STATES AND SYNTHESIZED OUTPUT VOLTAGE LEVELS

| $V_{7L}$ | $V_{5L}$ | $V_{3L1}$ | $V_{3L2}$ | $V_{HB}$ | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 | S10 | S11 | S12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| -3$V_{dc}$ | -2$V_{dc}$ | -$V_{dc}$ | $V_{dc}$ | -$V_{dc}$ | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| -2$V_{dc}$ | -2$V_{dc}$ | -$V_{dc}$ | $V_{dc}$ | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| | -$V_{dc}$ | -$V_{dc}$ | 0 | -$V_{dc}$ | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| | -$V_{dc}$ | 0 | $V_{dc}$ | -$V_{dc}$ | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| -$V_{dc}$ | -$V_{dc}$ | -$V_{dc}$ | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| | -$V_{dc}$ | 0 | $V_{dc}$ | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| | 0 | 0 | 0 | -$V_{dc}$ | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| $V_{dc}$ | 0 | 0 | 0 | $V_{dc}$ | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| | $V_{dc}$ | $V_{dc}$ | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| | $V_{dc}$ | 0 | -$V_{dc}$ | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 2$V_{dc}$ | $V_{dc}$ | $V_{dc}$ | 0 | $V_{dc}$ | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| | $V_{dc}$ | 0 | -$V_{dc}$ | $V_{dc}$ | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| | 2$V_{dc}$ | $V_{dc}$ | -$V_{dc}$ | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 3$V_{dc}$ | 2$V_{dc}$ | $V_{dc}$ | -$V_{dc}$ | $V_{dc}$ | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |

TABLE II
STRUCTURES FOR 3L, 5L, AND 7L WAVEFORMS ($N = 5$)

| Waveform | Voltage levels | Step transitions |
|---|---|---|
| 3L | 0, 1, 0, 1, 0, 1 | 1,-1,1,-1,1 |
| 5L | 0, 1, 0, 1, 2, 1 | 1,-1,1,1,-1 |
| | 0, 1, 2, 1, 0, 1 | 1,1,-1,-1,1 |
| | 0, 1, 2, 1, 2, 1 | 1,1,-1,1,-1 |
| 7L | 0, 1, 0, 1, 2, 3 | 1,-1,1,1,1 |
| | 0, 1, 2, 1, 2, 3 | 1,1,-1,1,1 |
| | 0, 1, 2, 3, 2, 1 | 1,1,1,-1,-1 |
| | 0, 1, 2, 3, 2, 3 | 1,1,1,-1,1 |

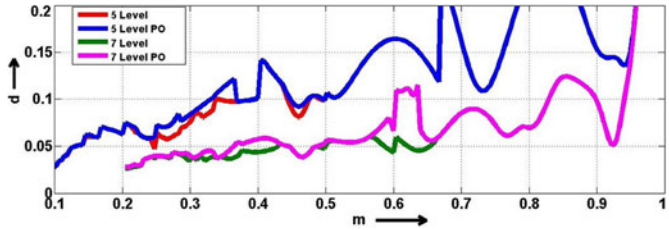



Fig. 2. Comparison of $d$ between 5L and 7L waveforms with $f_{s,\max} = 50$ Hz.

relationship between $N$, $m$, and $f_{s,\max}$ is obtained as [13]

$$N = \text{floor}\left(\frac{3f_{s,\max}}{f_1}\right) = \text{floor}\left(\frac{3f_{s,\max}}{mf_{1R}}\right). \quad (4)$$

The value of $m$ is discretized into 255 intervals and each interval corresponds to a particular value of *N*. For each steady-state operating point (*m*, *N*), optimal switching patterns are obtained that results into minimal $d$ given by (2). From (4), it can be observed that value of $N$ is high at lower $m$ values, which leads to high number of possible structures. Therefore, the computation time to optimize all structures increases at lower $m$ values. In addition, performance of optimization reduces at lower $m$ values ($0 \leq m < 0.3$). Therefore, space vector modulation is preferred for the lower $m$ values [15]. The complete details of optimization algorithm has been discussed in [22].

### B. Optimization Results

The SOP algorithm developed in the MATLAB programming is used for generating optimized angles for 5L and 7L waveforms with $f_{s,\max}$ limited to 50 Hz. The values of $d$ for 5L and 7L waveforms before and after post-optimization are shown in Fig. 2. The results show that for a 7L inverter, it is possible to reduce the device switching frequency to 50 Hz without compromising on THD of machine currents. Also, it is observed that there is a little compromise in $d$ with post-optimization that is done to avoid transients in machine currents. At lower $m$ values, the THD of machine currents increases even though the value of $d$ decreases. However, high-power drives are usually operated in higher modulation index range ($m > 0.5$), where SOP offers superior performance. As the value of $m$ becomes close to unity, operation of the inverter will be similar to six-step operation.

## IV. DISTRIBUTION OF OPTIMAL PULSE PATTERNS

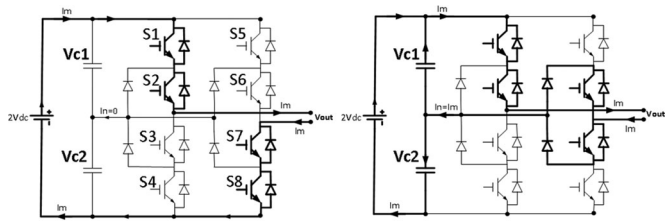
The phase output of cascade-5/3H inverter consists of 7L waveform, which is obtained by combining outputs of 3L-NPC1, 3L-NPC2, and H-Bridge inverters. A systematic procedure is developed to assign switching angles for each semiconductor device from corresponding optimal 7L waveforms. The main challenge is to ensure equal distribution of switching losses among all power semiconductor devices as well as minimal unbalance in dc-link voltages of 5L-NPC inverter.

### A. Distribution of Switching Transitions

The switching transition in a 7L waveform is due to transition in one of the 3L inverters, i.e, 3L-NPC1, 3L-NPC2, and H-Bridge. If $N_{3L}$ denotes switching transitions in a 3L inverter (3L-NPC or H-Bridge), the device switching frequency $f_s$ is equal to $N_{3L} f_1$. Therefore, the total switching transitions in a 7L waveform $N_{7L}$ should be equally divided among all 3L inverters for ensuring equal distribution of switching losses. However, equal distribution of switching transitions is possible only when $N_{7L}$ is a multiple of 3. Table III shows possible divisions of switching transitions $N_{7L}$ among all 3L inverters. It should be observed that switching transitions are equally divided among 3L inverters only when $N_{7L} = 3$, 6 or 9. Otherwise, each 3L inverter will have different switching transitions. In addition, due to constraint of minimizing the dc-link voltage unbalance, equal division of switching transitions may not be possible even if $N_{7L}$

TABLE III
DISTRIBUTION OF $N$ AND DEVICE SWITCHING FREQUENCIES FOR 7L CASCADE INVERTER

| $N_{7L}$ | $m$ | $f_1(Hz)$ | $N_{HB}$ | $N_{5L}$ | $N_{3L1}$ | $N_{3L2}$ | $f_{s,max}$(HB,3L1,3L2)(Hz) | $f_{s,avg}$ (Hz) |
|---|---|---|---|---|---|---|---|---|
| 3 | 0.751 - 1 | 37.55 - 50 | 1 | 2 | 1 | 1 | 50, 50, 50 | 37.55 - 50 |
| 4 | 0.601 - 0.75 | 30.05 - 37.5 | 1 | 3 | 1 | 2 | 37.5, 37.5, 75 | 40.06 - 50 |
| | | | 2 | 2 | 1 | 1 | 75, 37.5, 37.5 | |
| 5 | 0.501 - 0.600 | 25.05 - 30 | 1 | 4 | 2 | 2 | 30, 60, 60 | 41.75 - 50 |
| | | | 2 | 3 | 1 | 2 | 60, 30, 60 | |
| 6 | 0.429 - 0.5 | 21.45 - 25 | 2 | 4 | 2 | 2 | 50, 50, 50 | 42.9 - 50 |
| 7 | 0.376 - 0.428 | 18.8 - 21.4 | 2 | 5 | 2 | 3 | 42.85, 42.85, 64.28 | 43.87 - 50 |
| | | | 3 | 4 | 2 | 2 | 64.28, 42.85, 42.85 | |
| 8 | 0.334 - 0.375 | 16.7 - 18.75 | 2 | 6 | 3 | 3 | 37.5, 56.24, 56.24 | 44.53 - 50 |
| | | | 3 | 5 | 2 | 3 | 56.24, 37.5, 56.24 | |
| | | | 2 | 6 | 2 | 4 | 37.5, 37.5, 75 | |
| | | | 4 | 4 | 2 | 2 | 75, 37.5, 37.5 | |
| 9 | 0.301 - 0.333 | 15.05 - 16.65 | 3 | 6 | 3 | 3 | 50, 50, 50 | 45.15 - 50 |



(a) (b)

Fig. 3. Analysis of dc-link voltages for different switching patterns.

is a multiple of 3. This leads to different switching frequencies for 3L inverters and hence, unequal switching losses. However, by using swapping of gating signals, it is possible to operate all power semiconductor devices at same switching frequency [13]–[15]. The last column of Table III shows that average device switching frequency $f_{s,\mathrm{avg}}$ is always limited to $f_{1R}$ (50 Hz) for any given $N_{7L}$.

### B. Minimizing Unbalance in DC-Link Voltages

The dc-link voltages of inverter are assumed constant while deriving (2). However, there might be an unbalance in the dc-link voltages of the 5L-NPC inverter that depends on the load condition as well as switching patterns [24]. The difference between two dc-link capacitor voltages is termed as neutral point potential (NPP) error. In steady-state operating conditions, average value of NPP error tends to become zero and thus further distortion of machine currents is negligible [25]. On the other hand, NPP error might get accumulated during transient operation, and thus, NPP balancing algorithms should be used [17]. Moreover, the ripple in dc-link capacitor voltages should be minimized to reduce voltage stress on the power semiconductor devices and capacitors. For 5L-NPC inverter, charging and discharging of dc-link capacitor voltages happens when output is $\pm V_{\mathrm{dc}}$, otherwise dc-link voltages remain constant. The analysis of dc-link capacitor voltages for two different switching patterns is shown in Fig. 3.

### C. Analysis for Three Operating Points

Three operating points ($m = 0.9225$, $N = 3$), ($m = 0.4667$, $N = 6$), and ($m = 0.3412$, $N = 8$) were selected and then optimal switching angles for each semiconductor device were determined based on the previous analysis. Table IV shows two possible combinations for obtaining optimal 7L waveform corresponding to operating point ($m = 0.4667$, $N = 6$). In both cases, the switching frequency of power semiconductor devices is equal to $2f_1$. However, combination 1 is preferred over combination 2 as it leads to less NPP error in dc-link voltages of 5L-NPC inverter. This is because dc-link capacitors are charged and discharged for a shorter duration (30.66°) with combination 1 compared to combination 2 (66.17°) in a quarter period. Thus,

TABLE IV
DISTRIBUTION OF OPTIMAL PULSE PATTERNS FOR OPERATING POINT ($m = 0.4667$, $N = 6$)

| Angle (deg) | $V_{7L}$ | $V_{5L}$ | $V_{HB}$ | Duration (deg) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 2.98 |
| 2.98 | 1 | 0 | 1 | 16.81 |
| 19.8 | 2 | **1** | 1 | **7.56** |
| 27.36 | 3 | 2 | 1 | 6.94 |
| 34.30 | 2 | 2 | 0 | 26.26 |
| 60.57 | 1 | **1** | 0 | **23.1** |
| 83.67 | 0 | 0 | 0 | 6.33 |
| | $N$=6 | $N$=4 | $N$=2 | |

(a) combination 1

| $V_{7L}$ | $V_{5L}$ | $V_{HB}$ | Duration (deg) |
|---|---|---|---|
| 0 | 0 | 0 | 2.98 |
| 1 | **1** | 0 | **16.81** |
| 2 | 2 | 0 | 7.56 |
| 3 | 2 | 1 | 6.94 |
| 2 | **1** | 1 | **26.26** |
| 1 | **1** | 0 | **23.1** |
| 0 | 0 | 0 | 6.33 |
| $N$=6 | $N$=4 | $N$=2 | |

(b) combination 2

TABLE V
OPTIMAL SWITCHING ANGLES AND DIVISION OF $N$

| | Optimal Angles (deg) | | | | |
|---|---|---|---|---|---|
| Output | 0 | 5.4 | 16.48 | 34.71 | $N$ |
| $V_{7L}$ | 0 | 1 | 2 | 3 | 3 |
| $V_{5L}$ | 0 | 1 | 2 | 2 | 2 |
| $V_{HB}$ | 0 | 0 | 0 | 1 | 1 |
| $V_{3L1}$ | 0 | 0 | 1 | 1 | 1 |
| $V_{3L2}$ | 0 | -1 | -1 | -1 | 1 |

(a) ($m$=0.9225, $N$=3, $f_1$=46.125 Hz)

| | Optimal Angles (deg) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Output | 0 | 2.98 | 19.79 | 27.36 | 34.3 | 60.57 | 83.67 | $N$ |
| $V_{7L}$ | 0 | 1 | 2 | 3 | 2 | 1 | 0 | 6 |
| $V_{5L}$ | 0 | 0 | 1 | 2 | 2 | 1 | 0 | 4 |
| $V_{HB}$ | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 2 |
| $V_{3L1}$ | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 2 |
| $V_{3L2}$ | 0 | 0 | -1 | -1 | -1 | -1 | 0 | 2 |

(b) ($m$=0.4667, $N$=6, $f_1$=23.335 Hz)

| | Optimal Angles (deg) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Output | 0 | 4.3 | 12.15 | 18.07 | 20.99 | 44.15 | 46.0 | 55.61 | 66.9 | $N$ |
| $V_{7L}$ | 0 | 1 | 2 | 1 | 2 | 3 | 2 | 1 | 0 | 8 |
| $V_{5L}$ | 0 | 0 | 1 | 1 | 2 | 2 | 1 | 0 | 0 | 4 |
| $V_{HB}$ | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 4 |
| $V_{3L1}$ | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 2 |
| $V_{3L2}$ | 0 | 0 | -1 | -1 | -1 | -1 | -1 | 0 | 0 | 2 |

(c) ($m$=0.3412, $N$=8, $f_1$=17.06 Hz)

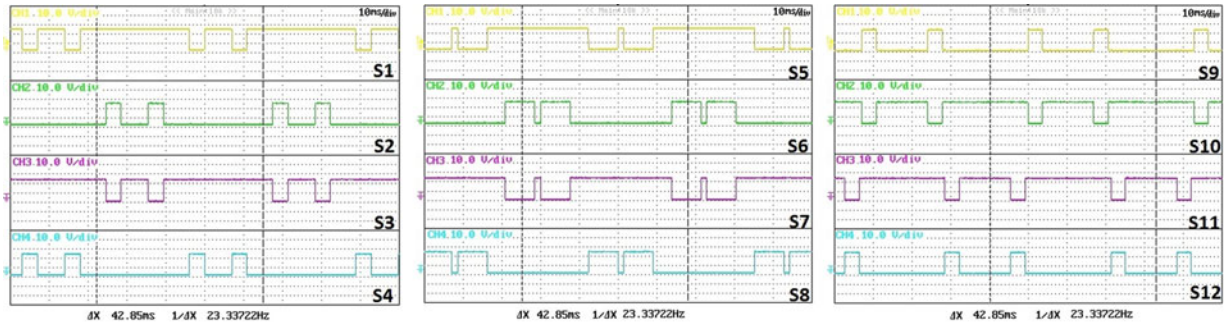



Fig. 4. Gating signals of power semiconductor devices for ($m = 0.4667$, $N = 6$). (a) 3L-NPC1, (b) 3L-NPC2, and (c) H-Bridge.

TABLE VI
VALUE OF $N$ AND DEVICE SWITCHING FREQUENCY $f_s$

| IGBT | $N$ | $f_s$ (Hz) |
|---|---|---|
| S1-S4 | 2 | 46.275 |
| S5-S8 | 2 | 46.275 |
| S9-S12 | 2 | 46.275 |

(a) ($m$=0.9225, $N$=3)

| IGBT | $N$ | $f_s$(Hz) |
|---|---|---|
| S1-S4 | 4 | 46.67 |
| S5-S8 | 4 | 46.67 |
| S9-S12 | 4 | 46.67 |

(b) ($m$=0.4667, $N$=6)

| IGBT | $N$ | $f_s$ (Hz) |
|---|---|---|
| S1-S4 | 4 | 34.12 |
| S5-S8 | 4 | 34.12 |
| S9-S12 | 8 | 68.24 |

(c) ($m$=0.3412, $N$=8)


Fig. 5. Gating signals of S1, S5, and S9 for ($m = 0.3412$, $N = 8$).

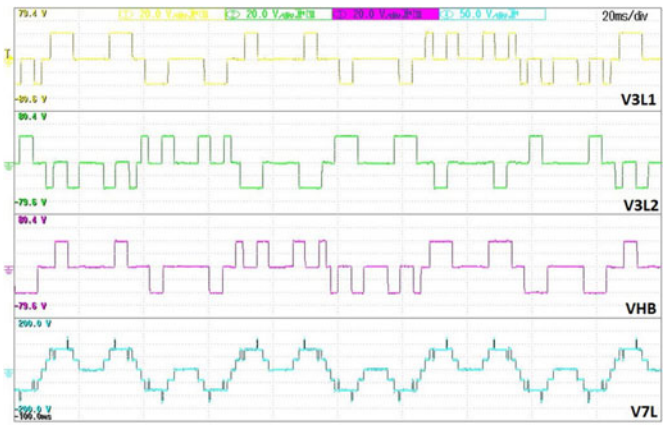



Fig. 6. $V_{3L1}$, $V_{3L2}$, $V_{HB}$, and $V_{7L}$ of phase A.

combination 1 is selected so that unbalance in dc-link capacitor voltages is less.

The optimal switching angles and corresponding division of $N_{7L}$ for three different operating points are shown in Table V. For operating point ($m = 0.4667, N = 6$), $N_{3L}$ for all 3L inverters

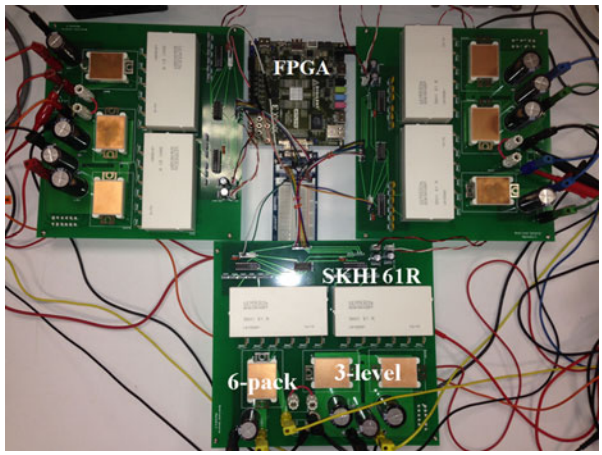



Fig. 7. Experimental setup for 7L cascade inverter.

TABLE VII
PARAMETERS OF MAJOR COMPONENTS IN 7L INVERTER EXPERIMENTAL SETUP

| Components | Parameters |
|---|---|
| Induction Motor | 1.5 kW, 400 V, 50 Hz |
| 3-level Module | F3L30R06W1E3_B11<br>$V_{CE}$ =600 V, $I_{Cnom}$ =30 A |
| Six-pack Module | FS30R06W1E3<br>$V_{CE}$ =600 V, $I_{Cnom}$ =30 A |
| Six-pack Driver | SKHI 61R<br>$V_{CE}$ =900 V, $f_{max}$ =50 kHz |
| Dc-link Capacitors | 1000 $\mu$F, 160 V electrolytic |

is obtained as 2 from Table V (b), so the switching frequency of all of them should be equal to $2f_1$. Fig. 4 shows the gating signals for all power semiconductor devices and it is clear from the waveforms that each semiconductor device is turned ON/OFF twice in one fundamental period, i.e., switching frequency is equal to $2f_1$. The value of $N$ and switching frequency of power semiconductor devices for all three operating points are shown in Table VI.

The optimal switching angles and division of $N$ for operating point ($m = 0.3412$, $N = 8$, $f_1 = 17.06$ Hz) are shown in Table V(c). It can be observed that value of $N$ is different for each 3L inverter, and thus, power semiconductor devices of 3L inverters will be operating at different switching frequencies ($2f_1$, $2f_1$, and $4f_1$) as shown in Table VI (c). By swapping the

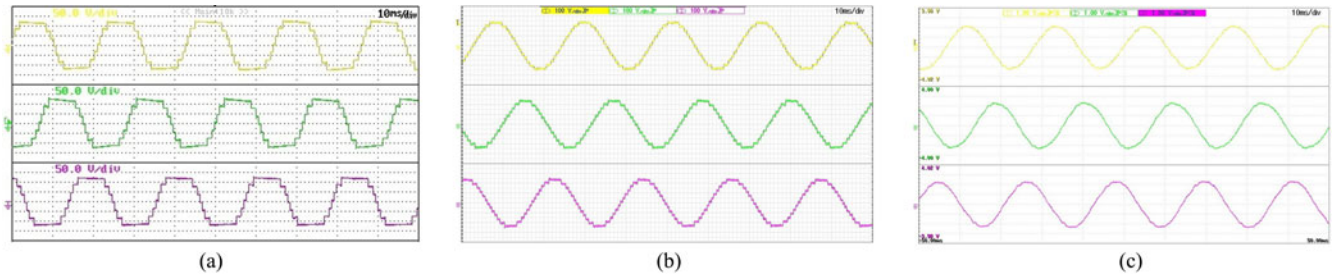



Fig. 8. Experimental results for ($m = 0.9225, N = 3$). *X*-axis: 10 ms/div (a) Phase voltages of 7L inverter (*Y*-axis: 50 V/div). (b) Input line voltages of induction motor (*Y*-axis: 100 V/div). (c) Stator currents of induction motor (*Y*-axis: 1 A/div).

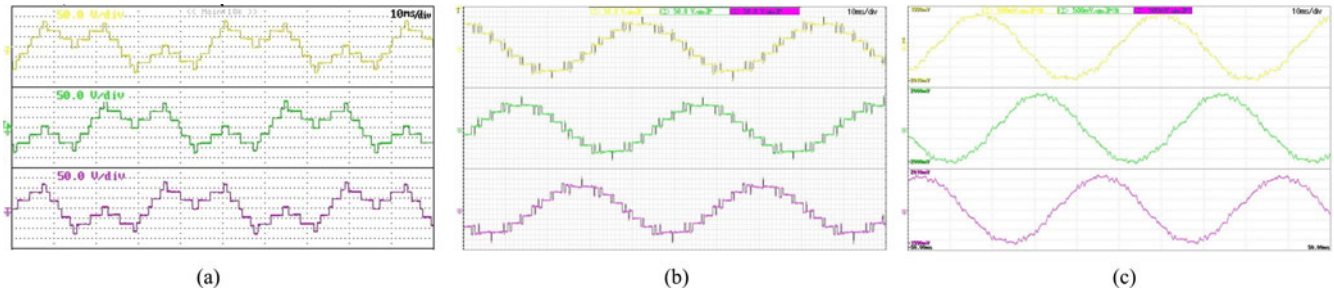



Fig. 9. Experimental results for ($m = 0.4667, N = 6$). *X*-axis:10 ms/div. (a) Phase voltages of 7L inverter (*Y*-axis: 50 V/div). (b) Input line voltages of induction motor (*Y*-axis: 50 V/div). (c) Stator currents of induction motor (*Y*-axis: 0.5 A/div).

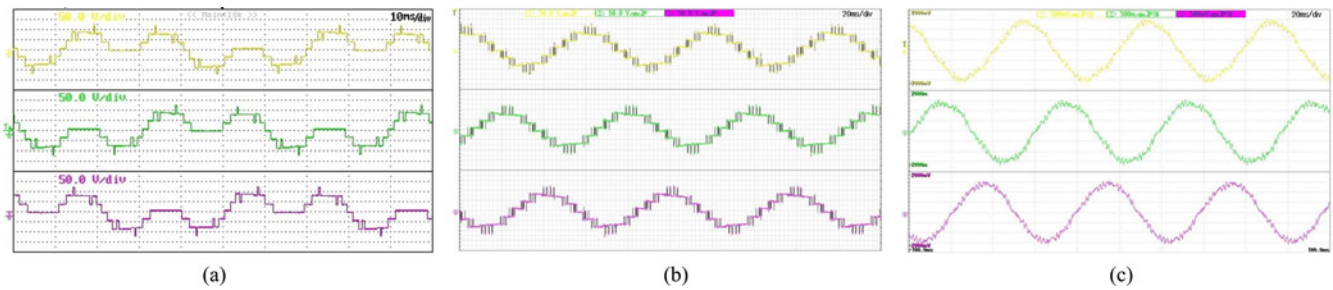



Fig. 10. Experimental results for ($m = 0.3412, N = 8$). (a) Phase voltages of 7L inverter (*X*-axis: 10 ms/div, *Y*-axis: 50 V/div). (b) Input line voltages of induction motor (*X*-axis: 20 ms/div, *Y*-axis: 50 V/div). (c) Stator currents of induction motor (*X*-axis: 20 ms/div, *Y*-axis: 0.5 A/div).

switching patterns among 3L inverters after every fundamental cycle, it is possible to operate all power semiconductor devices at same switching frequency. The swapping of gating signals can be observed in Fig. 5 for three consecutive fundamental cycles and it is clear from the waveforms that each semiconductor device has total switching transitions equal to 16 in three fundamental cycles and thus, each of them will be operating at switching frequency equal to $\frac{8f_1}{3}$. The output voltages of 3L-NPC1, 3L-NPC2, and H-Bridge inverters with swapping of gating signals are shown in Fig. 6. It should be noticed that the output phase voltage of 7L inverter remains same with swapping of gating signals among 3L inverters.

## V. Experimental Results

An experimental setup of 7L cascade inverter feeding a 1.5-kW induction motor shown in Fig. 7 has been developed for demonstrating the performance of SOP. The 7L cascade inverter was implemented by using 3L-NPC, six-pack modules from Infineon, and a six-pack IGBT driver SKHI 61R from Semikron. It should be noted that by using different configurations pins, it is possible to drive a three-level NPC module using SKHI 61R. The list of major components along with their rated parameters are shown in Table VII. The switching signals were programmed on a Xilinx Spartan-6 FPGA. The induction motor was supplied with phase voltage of 110 V at rated fundamental frequency (50 Hz). Then, the input dc voltages to H-Bridge and 5L-NPC inverter is obtained as 40.75 and 81.5 V, respectively.

The output phase voltages of 7L inverter for three operating points ($m = 0.9225, N = 3$), ($m = 0.4667, N = 6$), and ($m = 0.3412, N = 8$) are shown in Figs. 8 (a) to 10 (a), respectively. The line voltages of induction motor for three operating points are shown in Figs. 8(b) to 10(b), respectively. The stator currents of induction motor are nearly sinusoidal as shown in Figs. 8(c) to 10(c) with very low device switching frequencies below $f_{1R}$ equal to 46.275 Hz, 46.67 Hz, and 45.49 Hz, respectively. It can be observed that at lower $m$ values, the harmonic distortion of machine currents increases. The dc-link capacitor voltages ($Vc1, Vc2$) of the 5L-NPC inverter corresponding to three operating points are shown in Fig. 11(a)–(c) and they are almost

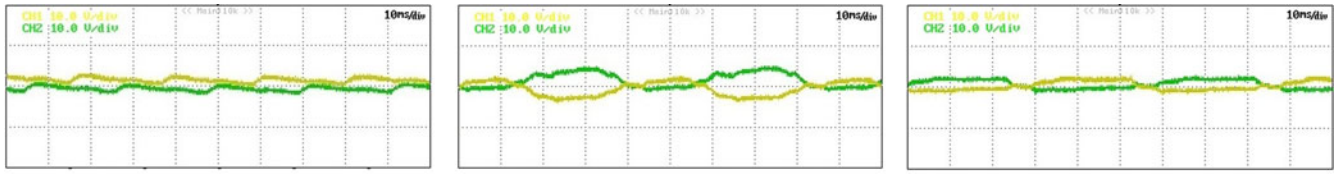



Fig. 11. Dc-link voltages of 5L-NPC inverter. *X*-axis:10 ms/div, *Y*-axis:10 V/div. (a) ($m = 0.9225$, $N = 3$), (b) ($m = 0.4667$, $N = 6$), and (c) ($m = 0.3412$, $N = 8$).

Fig. 12. Space vector trajectory of stator currents. (a) ($m = 0.9225$, $N = 3$), (b) ($m = 0.4667$, $N = 6$), and (c) ($m = 0.3412$, $N = 8$).

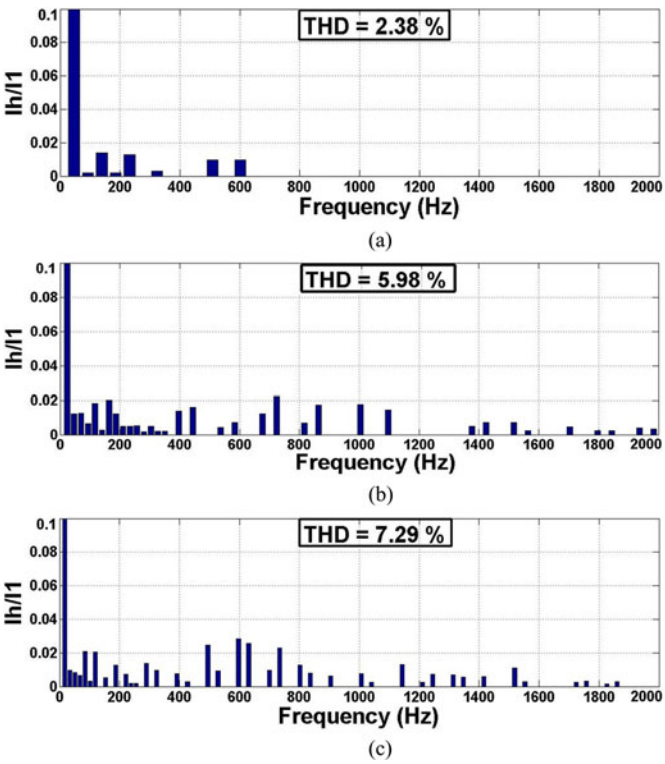



Fig. 13. Harmonic spectrum of stator current. (a) ($m = 0.9225$, $N = 3$), (b) ($m = 0.4667$, $N = 6$), and (c) ($m = 0.3412$, $N = 8$).

balanced. For operating point ($m = 0.4667$, $N = 6$), the dc-link capacitor voltages as shown in Fig. 11(b) have more NPP error due to higher duration for charging and discharging of dc-link capacitors (30.66°) compared to other operating points.

The space vector trajectory of induction motor stator currents for three operating points are shown in Fig. 12(a)–(c), respectively. The nearly circular space vector trajectories indicates minimal harmonic distortion. It should be observed that harmonic distortion increases at lower $m$ values. Also, data acquisition system has been used to record data of stator currents for determining harmonic spectrum. The harmonic spectrum of the stator currents for the three operating points are shown in Fig. 13(a)–(c), respectively. The THD of stator currents for three operating points is equal to 2.38%, 5.98%, and 7.29%, respectively, and it should be noted that all the dominant harmonic components are less than 3% of the fundamental component. Therefore, it can be concluded that there is no compromise on quality of stator currents with average device switching frequencies limited to $f_{1R}$ (50 Hz).

## VI. Summary and Conclusion

In medium voltage high-power drives, low device switching frequency and minimal harmonic distortion of stator currents are main requirements. However, low-switching frequency operation leads to more distortion of machine currents. The proposed SOP technique for the 7L inverter permits low-switching frequency operation while maintaining the quality of current waveforms. The cascade-5/3H topology is used to develop the 7L inverter. SOP generated optimal switching patterns of 7L waveforms for all steady-state operating points and then switching angles for each semiconductor device were determined to ensure equal distribution of switching losses as well as minimal unbalance in the dc-link capacitor voltages. The experimental results obtained from the 7L inverter controlling induction motor drive demonstrated effectiveness of the SOP technique for controlling the 7L multilevel inverter at average device switching frequencies limited to rated fundamental frequency without compromising on quality of stator currents.

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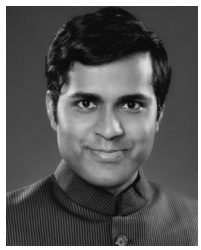

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