

Modular Multilevel Converter With an Adaptive Observer of Capacitor Voltages

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Abstract—A modular multilevel converter (MMC) is an attractive solution for power conversion without transformers. The MMC consists of cascade connections of floating dc capacitors. In this paper, an adaptive observer design has been proposed to estimate the capacitor voltages from the measurement of arm currents. This work introduces the capacitance value of the cell capacitors as a parameter uncertainty for making the system performance robust with unknown constant parameters. It may be used for predictive control, condition monitoring for capacitors, and diagnosis check for capacitor health. In addition, a pulsewidth modulation (PWM) technique for MMC has been explored. The PWM technique is performed using a carrier-based level-shifted PWM strategy. It does not necessitate the calculation of duty cycles, and can be easily implemented in a DSP. By using the PWM technique, harmonics in the phase voltage is shifted to twice the switching frequency. Theoretical analysis is included in this paper for showing stability and convergence of the proposed observer. Analytical expressions are verified by simulation and experimental results.

Index Terms—Adaptive observer, Lyapunov analysis, modular multilevel converter (MMC), pulsewidth modulation (PWM), switching frequency.

NOMENCLATURE

MMC	Modular multilevel converter.
HVDC	High voltage direct current.
V_{dc}	DC-link voltage of the converter.
v_j	Output voltage of the cell j .
L_1	Inductance of the arm inductor.
R	Load resistance.
L	Load inductance.
i_p	Upper arm current.
i_n	Lower arm current.
i_a	Phase A load current.
V_{AO}	Pole voltage of the converter phase A.
V_{cell}	Cell output voltage.
C	Cell capacitance.
N	Number of cells per arm.

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$J(x)$	Jacobian matrix.
$\lambda_j, \lambda_l, \lambda'_j,$ and λ'_l	Observer gains.
\hat{x}	Estimation error.
V_e	Lyapunov function.

I. INTRODUCTION

THE MMC has become an important aspect of research of both academia and industry environments among other multilevel topologies in recent times, mainly due to the outstanding merits of this converter over conventional ones including: simple implementation of redundancy, low device ratings, very low output harmonics, easy scalability and a possibility of common dc-bus configuration for multidrive applications [1]–[8]. As such, the converter has found a commercial application within few years of its first proposal [9]–[12]. The output voltage quality of the MMC is almost close to sinusoidal, thus putting less requirements on the design of the output ac filter. So far, several research studies have been conducted on employing of pulsewidth modulation (PWM) schemes in MMC [7], [13]–[18].

In recent papers [7], [13], [14], phase-shifted PWM (PS-PWM) and PWM using duty ratio calculations have been reported for a MMC. The algorithm based on the fixed pulse pattern has been studied in MMC to operate at the fundamental switching frequency [15]. The research work in [16] has addressed an improved submodule unified pulsewidth modulated method to achieve the output voltage level similar to the PS-PWM method. The advantage in this case is that it does not require a controller for voltage balancing. The study in [17] presented the modified PS-PWM approach to reduce the average device switching frequency by developing a voltage balancing algorithm. On the other hand, the sorting techniques proposed in [5] and [19] are very easy and elegant to implement. However, it still needs to calculate the duty cycles based on the reference waveforms. The duty cycle calculation can be avoided, as shown in [18], by using carrier-based level-shifted PWM (LS-PWM).

In this paper, an LS-PWM technique has been applied to the MMC. This aims in shifting the harmonics in the phase voltage to twice the switching frequency. This method provides the possibility to cancel the switching frequency harmonics from the upper and lower converters using properly adjusting the dc offsets in LS-PWM. Therefore, the phase voltage waveform contains harmonics at twice the switching frequency and its sidebands. In other words, to produce the same output voltage quality, the individual cells of the converter can be switched at half the switching frequency.

The second part of this paper focuses on designing an adaptive observer for MMC in order to estimate the unmeasurable voltages of the capacitors using the arm currents and the dc-voltage

source. By increasing the number of cascaded modules, it will be necessary to add the number of voltage sensors. As a consequence, it causes an increased hardware complexity, which will influence negatively the system reliability. Hence, the estimation of such voltages by means of an observer becomes an attractive and economical option particularly in real-time performance in the presence of time delay in measurements as well as the communication process.

There is no much research currently regarding the development of such kind of schemes for MMC. Observer-based and estimation methods are well suited for control reconfiguration purposes in such a way that estimated quantities are utilized for reconfiguration algorithms. For instance, by estimating the capacitors voltages, knowledge of the switches state, make it possible to find the output voltage which can be incorporated in fault detection and diagnosis strategy [20]–[22]. In [22], though presented interesting benefits of the sliding-mode observer for MMC in the simulation environment, but the chattering problem due to the discontinuous controls in this method is the crucial factor resulting in high oscillations [23].

Furthermore, as a matter of issues such as electrolytic reaction, humidity, effect of temperature, and some variable factors of the system, the capacitor variations can occur. So, it is necessary to know how much the capacitance has changed. It is also hard to measure directly the capacitance since capacitor banks are usually placed inside the converter system. To overcome this difficulty, some methods to estimate the capacitance have been proposed based on the increase of the internal equivalent series resistance of the capacitor with the aging [24], [25]. But main disadvantage is that those approaches are not suitable for online application. Moreover, online capacitance estimation methods for three-phase ac/dc/ac PWM converters have been reported in [26].

For making the system performance robust with unknown constant parameters, this paper introduces the capacitance value of the cell capacitors as a parameter uncertainty. The better understanding of observer behavior in MMC is based on the nonlinear dynamical system theory. Therefore, to create kind of a sensorless control, it is necessary to investigate the observability of the converter [27]. To compensate the uncertainty, a nonlinear adaptive control method is adopted to derive the control algorithm, and the uncertainty adaptation laws can also be derived systematically. The observer stability study based on the Lyapunov theory guarantees the stability and convergence of the estimated quantities. The first measurement considered is the arm currents which are the controlled variables and makes it possible to estimate the capacitor voltages. Afterward, it is necessary to know the dc-link voltage state V_{dc} because of the capacitors voltages references depend on it. By taking a measurement of this voltage, especially if the converter is supplied by a controlled rectifier, it will be available. However, in some applications, the converter output voltage is required, e.g., fault detection algorithms. From control theory point of view, an observer is considered as a software sensor used to estimate the unmeasurable variables of a system.

Finally, some illustrative simulation and experimental results of MMC are demonstrated to confirm the feasibility of the proposed PWM algorithm as well as the designed observer.

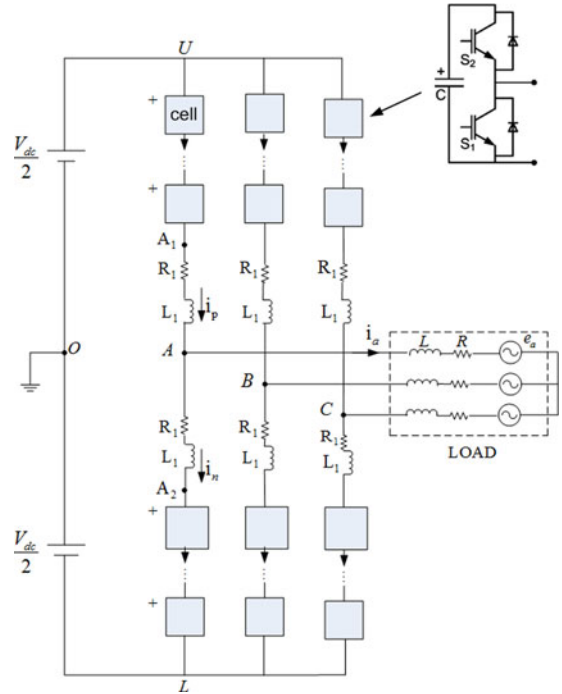


Fig. 1. Diagram of a three-phase MMC.

II. SYSTEM DESCRIPTION OF THE MMC

In this section, a short description of the operation principles of the MMC is given. This topology consists of a number of series-connected cells constituting of a capacitor and two complementary switches as shown in Fig. 1. When switch S_1 is turned ON, the capacitor is bypassed and there is no voltage at the cell output. When S_2 is turned ON, the capacitor voltage is appeared at the output. Depending on the direction of the current, the capacitor can either be charged or discharged. Employing many numbers of cells, a multilevel voltage waveform can be produced at the output through inserting or bypassing certain number of the cells.

There are two arms of the converter in each phase which are formed by the cells connected in series. These are called the upper and lower arms in this paper. The arms are fed from the dc link. The upper and lower converter currents make up the load current; their directions are denoted in Fig. 1. Assuming the convention of voltages shown in Fig. 1, the upper and lower converters produce sinusoidal voltages which are having 180° phase shift. For sinusoidal modulation, the ideal waveforms are depicted in Fig. 2 which are stated as v_{UA1} and v_{A2L} . The mathematical expression of arm voltages is given by

$$\begin{aligned} v_{UA1}(t) &= \left[\frac{1}{2} + m \cdot \sin(\omega t) \right] V_{dc} \\ v_{A2L}(t) &= \left[\frac{1}{2} - m \cdot \sin(\omega t) \right] V_{dc} \end{aligned} \quad (1)$$

where m is the modulation index lies between 0 and 0.5, ω is the angular frequency, and V_{dc} is the dc-link voltage. Using common mode voltage injection [28], the modulation index value can be enhanced up to 0.577 for achieving maximum ac voltage from the dc bus. Note the presence of the dc offset in

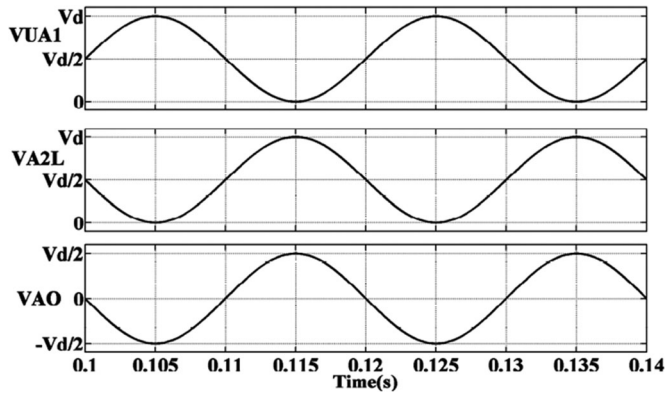


Fig. 2. Ideal output voltage waveforms for the upper and lower converters for phase A [18].

these waveforms. Because of the quite small voltage drop across the arm inductor, the output pole voltage v_{AO} is an ac voltage having equal positive and negative excursions

$$v_{AO}(t) \approx v_{A1U}(t) + v_{UO}(t) = m \cdot \sin(\omega t) V_{dc}. \quad (2)$$

In real circuit of MMC, the voltages v_{UA1} and v_{A2L} are not perfectly sinusoidal because of the waveforms are produced using finite number of dc sources through the PWM strategy. More specifically, the capacitors constantly charge or discharge due to the flow of the load current through them. Therefore, the voltages at points A_1 and A_2 are not exactly equal all the time. The arm inductor is inserted in the circuit to limit the flow of circulating current due to this voltage difference. The ideal waveforms of this converter are used to generate the reference modulating waveforms for control purpose, which is discussed next.

III. LS-PWM TECHNIQUE

The LS-PWM scheme for the MMC is explained in this section. In the first step, three sinusoidal balanced reference waveforms are generated for three phases. In order to increase the dc-bus utilization in the linear modulation range, a common mode signal is added to all the three reference waveforms. In actual implementation hardware with DSP, the reference waveforms are not continuous but are sampled at regular intervals. This makes the modulating waveforms stepped in nature as shown in Fig. 3. The reference waveforms for the lower converter are multiplied by -1 .

Here, only one triangular carrier is used for switching all the cells in three phases. This is done to avoid the high accuracy needed with synchronization of multiple carriers. Failure to achieve synchronization leads to delay between gating signals to the devices that are supposed to turn ON at the same time. The loss of synchronization can also happen if multiple DSPs and field-programmable gate arrays (FPGAs) are used to generate the carriers. In that case, synchronization of their clocks is to be maintained. The magnitude of the carrier is $1/N$, where N is the number of cells in each arm. In this paper, $N = 4$.

In LS-PWM, the modulating waveform is scaled and shifted in such a way so as to bring it inside one carrier (see Fig. 4). Here, the carrier magnitude is $1/4 = 0.25$ and spans from 0 to 0.25.

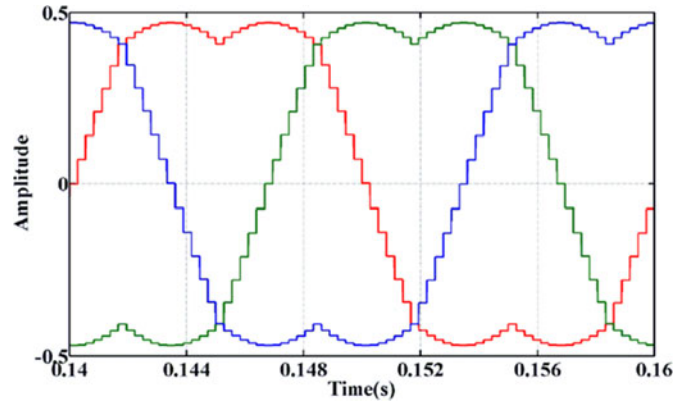


Fig. 3. Reference waveforms after the addition of the common mode signal [18].

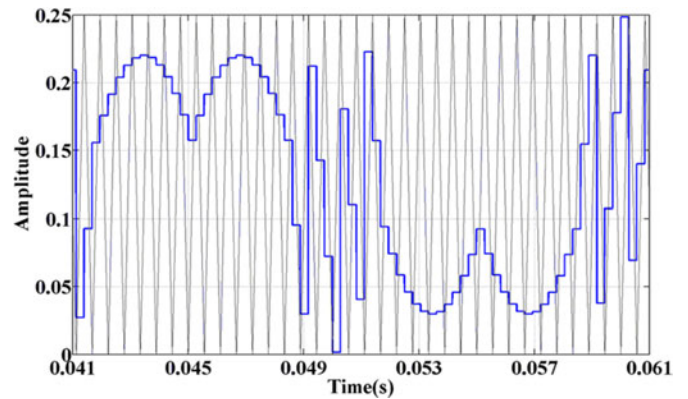


Fig. 4. Reference waveform after it is brought inside one carrier [18].

The modulating waveform should always lie within the carrier. So, it needs one or two level shifts to bring it inside this carrier. For example, if the modulating waveform is between 0.25 and 0.5, then a negative shift of -0.25 is required to bring it inside the carrier (between 0 and 0.25). Accordingly, the number of cells that will be turned ON, OFF, or used for PWM will be decided. This is tabulated in Table I. The duty cycle for the PWM is automatically generated as the level-shifted modulating waveform is compared with the carrier. There is no need to calculate the duty cycle of individual cells.

An example is presented here. It is assumed that a positive magnitude of upper arm current i_p will charge the cells further, while a negative magnitude will discharge them. At the current sampling, it is found that the voltage magnitudes of the upper cells are in the following order: Cells 3, 1, 2, and 4 where Cell 3 has the highest voltage. Suppose the modulating waveform is between -0.25 and 0. So, from Table I, it is found that Cells 1 and 3 are bypassed. Cell 4 is charging (by turning OFF S_1). Cell 2 is in PWM mode where the triangle is compared with the modulating waveform. Switch S_1 in cell 2 is turned ON once the modulating waveform is greater than the triangle; otherwise, it is turned OFF.

The next step is to make the duration of start and end crossings of the modulating waveform equal [see Fig. 5(a)]. Here, the reference waveforms for the three phases of the upper converter are shown. Note that, the start and end timing durations

TABLE I
SHIFT OF MODULATING WAVEFORM AND ITS EFFECT ON CELLS

Modulating waveform amplitude	Shift required	No. of cells turned on	No. of cells turned off	No. of cells used for PWM	Switching combinations for upper 4 cells			
					Cell 1	Cell 2	Cell 3	Cell 4
-0.5 to -0.25	0.5	0	3	1	S1=1	S1=1	S1=1	S1, S2 used for PWM
-0.25 to 0	0.25	1	2	1	S1=1	S1, S2 used for PWM	S1=1	S1=0
0 to 0.25	0	2	1	1	S1, S2 used for PWM	S1=0	S1=1	S1=0
0.25 to 0.5	-0.25	3	0	1	S1=0	S1=0	S1, S2 used for PWM	S1=0

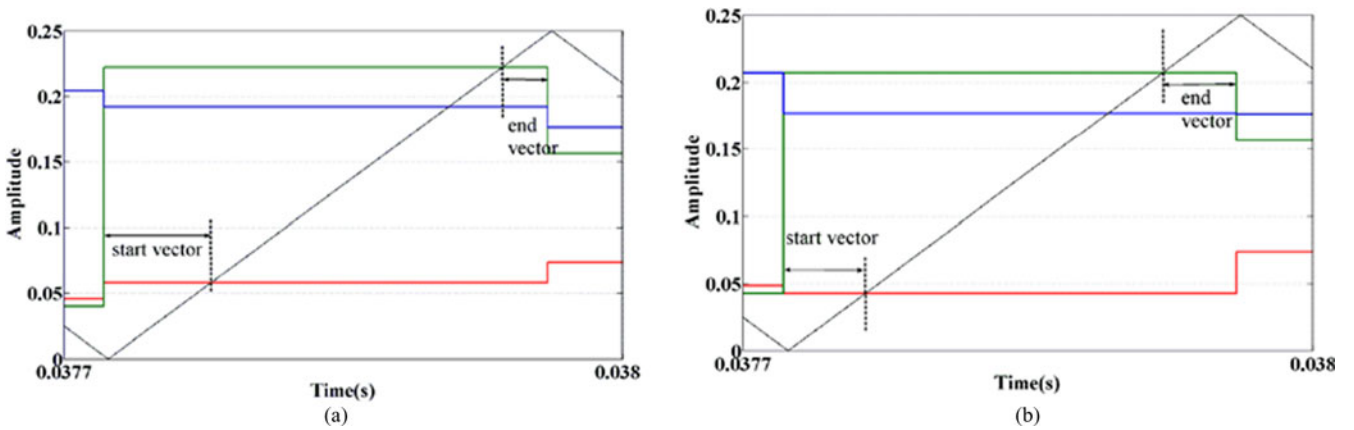


Fig. 5. Start and end vectors in a switching cycle: (a) unequal and (b) equal [18].

(corresponding to the start and end vectors) in a switching cycle are not equal. To make them equal, another offset (or common mode signal) is added to all the phases. The magnitude of this offset is

$$v_{\text{offset}} = \frac{1}{2}(0.25 - v_{\text{max}} - v_{\text{min}}) \quad (3)$$

where v_{max} and v_{min} are the maximum and minimum values in that switching cycle. The waveforms after the addition of the offset are shown in Fig. 5(b). With this strategy, the switching frequency harmonics of the upper and lower converters cancel each other. The harmonics in the output voltage are then shifted to twice the switching frequency.

An important requirement of MMC is the balancing of capacitor voltages. An easy balancing technique described in [5] is followed here. In this technique, a sorting algorithm is used to control the capacitor voltages. Based on the sensed capacitor voltages, the sorting algorithm identifies which cells need to be turned ON or OFF, and which one is to be used for PWM.

IV. DESIGN STEPS OF AN ADAPTIVE OBSERVER

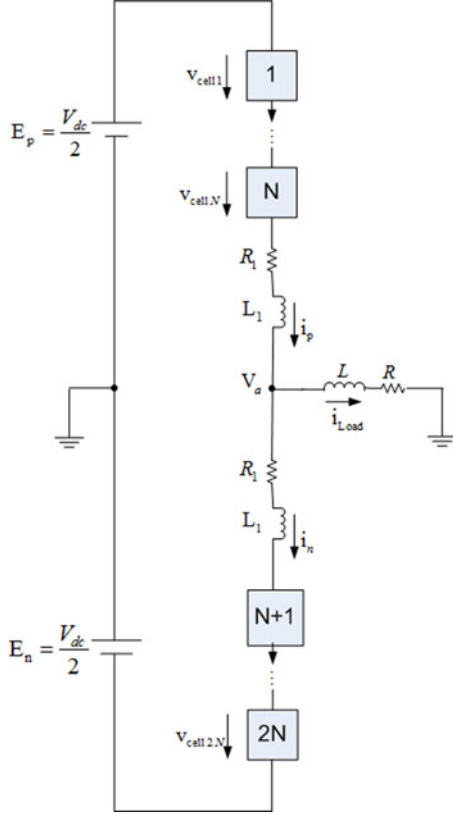
In this study, control strategy based on adaptive algorithm is investigated to design an observer for estimating the unmea-

surable states in the case that neither of the voltage sensors is available. It considers a systematic construction of both feedback control laws as well as related Lyapunov functions.

Without loss of generality, the analysis has been applied to one phase of the MMC including N cells for each arm (see Fig. 6).

From Fig. 6, the mathematical equations describing the dynamic behavior of a N -cells MMC converter are expressed as follows:

$$\begin{aligned} \frac{di_p}{dt} &= \frac{1}{L_1} \left[E_p - \sum_{i=1}^N (S_i \cdot V_{C_i}) - R_1 i_p - V_a \right] \\ \frac{di_n}{dt} &= \frac{1}{L_1} \left[E_n - \sum_{i=N+1}^{2N} (S_i \cdot V_{C_i}) - R_1 i_n + V_a \right] \\ \frac{dV_{C_i}}{dt} &= \frac{1}{C} (i_p \cdot S_i) \quad i = 1, \dots, N \\ \frac{dV_{C_i}}{dt} &= \frac{1}{C} (i_n \cdot S_i) \quad i = N + 1, \dots, 2N \\ y_1 &= i_p \\ y_2 &= i_n \end{aligned} \quad (4)$$

Fig. 6. MMC leg consisting of $2N$ cells.

where i_p, i_n, S_i, V_{C_i} , and V_a are upper/lower arm currents, gating signal of upper gate, capacitor voltage of i th cell, and phase a voltage, respectively. The gating signal of lower gate is the complementary of S_i . E_p and E_n are assumed as a half of the dc-link voltage.

We assume that arm currents, i_p and i_n , are measured (observer input) and are taken as the system outputs. So, the states of V_{C_i} $i = 1, \dots, 2N$ are not available for feedback. The control objective is to make capacitor voltages estimation track the desired reference voltage command (V_{dc}/N). Moreover, a developed observer should involve an estimation of the unknown constant parameters which are simplified by following notations:

$$a_i = \frac{1}{C_i} \quad i = 1, \dots, 2N. \quad (5)$$

Before explaining the design process, it is essential to analyze the observability property of MMC. According to the observability criterion [29], the observability analysis is performed via computing the following Jacobian matrix J of $O_1(x)$ with respect to the state x :

$$J(x) = \frac{\partial}{\partial(x)} O_1(x). \quad (6)$$

By denoting

$$h(x) = [h_1 \quad h_2]^T = [y_1 \quad y_2]^T$$

$$O_1 = [h_1 \quad h_2 \quad L_g h_1 \quad L_g h_2]^T$$

$$x = [x_1 \quad x_2 \quad x_3 \quad x_4]^T = [i_p \quad i_n \quad V_{C_{i-u}} \quad V_{C_{i-l}}]^T$$

$$g = \left[\frac{di_p}{dt} \quad \frac{di_n}{dt} \quad \frac{dV_{C_{i-u}}}{dt} \quad \frac{dV_{C_{i-l}}}{dt} \right]^T \quad (7)$$

where $L_g h$ is defined as Lie derivative of h with respect to g , ($= \frac{\partial h}{\partial x} g$) [30]. The computation of the corresponding observability matrix gives

$$J(x) = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ \frac{\partial}{\partial x_1} L_g h_1 & \frac{\partial}{\partial x_2} L_g h_1 & \frac{\partial}{\partial x_3} L_g h_1 & \frac{\partial}{\partial x_4} L_g h_1 \\ \frac{\partial}{\partial x_1} L_g h_2 & \frac{\partial}{\partial x_2} L_g h_2 & \frac{\partial}{\partial x_3} L_g h_2 & \frac{\partial}{\partial x_4} L_g h_2 \end{bmatrix}. \quad (8)$$

The Jacobian expresses the observability of the converter in terms of rank sense through determinant Δ of $J(x)$ as

$$\Delta = \frac{\partial L_g h_1}{\partial x_3} \cdot \frac{\partial L_g h_2}{\partial x_4} - \frac{\partial L_g h_2}{\partial x_3} \cdot \frac{\partial L_g h_1}{\partial x_4}$$

$$= \left(\frac{R_1^2}{L_1^2} \cdot V_{C_i} \right) \sum_{i=1}^{2N} S_i. \quad (9)$$

Remark 1: Note that if $V_{C_i} \neq 0$, the converter is observable. In other words, by assuming the arm inductance is nonzero and constant thus, the converter is observable if and only if the capacitor voltage is not null. Moreover, with the same analysis, the observation of the cell capacitance value is proven.

The prediction model for the adaptive observer is chosen to be

$$\frac{d\hat{i}_p}{dt} = \frac{1}{L_1} \left[E_p - \sum_{i=1}^N (S_i \cdot \hat{V}_{C_i}) - R_1 i_p - V_a \right]$$

$$+ \lambda_j \cdot f(\tilde{i}_p) + \lambda_l \cdot \tilde{i}_p$$

$$\frac{d\hat{i}_n}{dt} = \frac{1}{L_1} \left[E_n - \sum_{i=N+1}^{2N} (S_i \cdot \hat{V}_{C_i}) - R_1 i_n + V_a \right]$$

$$+ \lambda'_j \cdot f(\tilde{i}_n) + \lambda'_l \cdot \tilde{i}_n$$

$$\frac{d\hat{V}_{C_i}}{dt} = \hat{a}_i(i_p \cdot S_i) + \lambda_i \cdot f(\tilde{i}_p) \quad i = 1, \dots, N$$

$$\frac{d\hat{V}_{C_i}}{dt} = \hat{a}_i(i_n \cdot S_i) + \lambda_i \cdot f(\tilde{i}_n) \quad i = N + 1, \dots, 2N$$

$$\hat{y}_1 = \hat{i}_p$$

$$\hat{y}_2 = \hat{i}_n \quad (10)$$

where $\lambda_j, \lambda_l, \lambda'_j$, and λ'_l are the observer gains, and $f(\tilde{i}_p, \tilde{i}_n)$ used to eliminate the errors in the arm current estimations.

The weighting factors that are vital for arm currents and capacitor voltages equations $\lambda_j f(\tilde{i}_p), \lambda_l \tilde{i}_p, \lambda'_j f(\tilde{i}_n), \lambda'_l \tilde{i}_n$ and $\lambda_i f(\tilde{i}_p), \lambda_i f(\tilde{i}_n)$ will be designed later.

It should be noted that the estimated quantities are denoted as \hat{x} and the estimation error which is the difference between real states or parameters and the estimated ones are shown with the \tilde{x} sign ($\tilde{x} = \hat{x} - x$).

Considering previous definition and after subtracting (4) from the estimated model (10), respectively, the observation error dynamics for the developed observer could be easily obtained and are written as follows:

$$\begin{aligned}\frac{d\tilde{i}_p}{dt} &= \frac{1}{L_1} \left[-\sum_{i=1}^N (S_i \cdot \tilde{V}_{C_i}) \right] + \lambda_j \cdot f(\tilde{i}_p) + \lambda_l \cdot \tilde{i}_p \\ \frac{d\tilde{i}_n}{dt} &= \frac{1}{L_1} \left[-\sum_{i=N+1}^{2N} (S_i \cdot \tilde{V}_{C_i}) \right] + \lambda'_j \cdot f(\tilde{i}_n) + \lambda'_l \cdot \tilde{i}_n \\ \frac{d\tilde{V}_{C_i}}{dt} &= \tilde{a}_i(i_p \cdot S_i) + \lambda_i \cdot f(\tilde{i}_p) \quad i = 1, \dots, N \\ \frac{d\tilde{V}_{C_i}}{dt} &= \tilde{a}_i(i_n \cdot S_i) + \lambda_i \cdot f(\tilde{i}_n) \quad i = N + 1, \dots, 2N \\ \tilde{y}_1 &= \tilde{i}_p \\ \tilde{y}_2 &= \tilde{i}_n\end{aligned}\quad (11)$$

where

$$\begin{aligned}\tilde{i}_p &= \hat{i}_p - i_p, \tilde{i}_n = \hat{i}_n - i_n, \tilde{V}_{C_i} = \hat{V}_{C_i} - V_{C_i} \\ \tilde{a}_i &= \hat{a}_i - a_i, \quad \tilde{y}_1 = \hat{y}_1 - y_1, \quad \tilde{y}_2 = \hat{y}_2 - y_2.\end{aligned}\quad (12)$$

Here, an attempt is performed to find proper Lyapunov function which plays a crucial role for deriving the observer gains and finally to determine the adaptation rules for unknown parameters (capacitance values). In doing so, and considering the convergence of the adaptive observer, the following Lyapunov function is proposed:

$$V_e = \frac{1}{2} \left(\tilde{i}_p^2 + \tilde{i}_n^2 + \sum_{i=1}^{2N} (S_i \cdot \tilde{V}_{C_i}^2) + \sum_{i=1}^{2N} \frac{1}{\rho_i} \tilde{a}_i^2 \right) \quad (13)$$

where ρ_i is any real constant, called parameter adaptation gain.

In view of (11), the time differentiation of V_e is

$$\begin{aligned}\dot{V}_e &= \tilde{i}_p \left\{ \frac{1}{L_1} \left[-\sum_{i=1}^N (S_i \cdot \tilde{V}_{C_i}) \right] + \lambda_j \cdot f(\tilde{i}_p) + \lambda_l \cdot \tilde{i}_p \right\} \\ &+ \tilde{i}_n \left\{ \frac{1}{L_1} \left[-\sum_{i=N+1}^{2N} (S_i \cdot \tilde{V}_{C_i}) \right] + \lambda'_j \cdot f(\tilde{i}_n) + \lambda'_l \cdot \tilde{i}_n \right\} \\ &+ \sum_{i=1}^N \left(\tilde{V}_{C_i} \cdot [\tilde{a}_i(i_p \cdot S_i) + \lambda_i \cdot f(\tilde{i}_p)] \right) \\ &+ \sum_{i=N+1}^{2N} \left(\tilde{V}_{C_i} \cdot [\tilde{a}_i(i_n \cdot S_i) + \lambda_i \cdot f(\tilde{i}_n)] \right) + \sum_{i=1}^{2N} \tilde{a}_i \frac{1}{\rho_i} \frac{d}{dt} \tilde{a}_i.\end{aligned}\quad (14)$$

As in (14), if all the terms including the \tilde{a}_i grouped together, then we have

$$\begin{aligned}\dot{V}_e &= \tilde{i}_p^2 (\lambda_l) + \tilde{i}_p (\lambda_j \cdot f(\tilde{i}_p)) + \tilde{i}_n^2 (\lambda'_l) + \tilde{i}_n (\lambda'_j \cdot f(\tilde{i}_n)) \\ &+ \sum_{i=1}^N (\tilde{V}_{C_i} \cdot \lambda_i \cdot f(\tilde{i}_p)) + \sum_{i=N+1}^{2N} (\tilde{V}_{C_i} \cdot \lambda_i \cdot f(\tilde{i}_n))\end{aligned}$$

$$\begin{aligned}&+ \sum_{i=1}^N \tilde{a}_i \left[\frac{1}{\rho_i} \frac{d}{dt} \tilde{a}_i + \tilde{V}_{C_i} (i_p \cdot S_i) \right] \\ &+ \sum_{i=N+1}^{2N} \tilde{a}_i \left[\frac{1}{\rho_i} \frac{d}{dt} \tilde{a}_i + \tilde{V}_{C_i} (i_n \cdot S_i) \right].\end{aligned}\quad (15)$$

To eliminate them, the two brackets are selected to be 0. Then, update laws are defined as

$$\begin{aligned}\sum_{i=1}^N \frac{d}{dt} \tilde{a}_i &= -\sum_{i=1}^N \rho_i \left[\tilde{V}_{C_i} (i_p \cdot S_i) \right] \\ \sum_{i=N+1}^{2N} \frac{d}{dt} \tilde{a}_i &= -\sum_{i=N+1}^{2N} \rho_i \left[\tilde{V}_{C_i} (i_n \cdot S_i) \right].\end{aligned}\quad (16)$$

Because the change rate of the capacitance values in the observer time scope are negligible, thus, we obtain

$$\frac{d\tilde{a}_i}{dt} = \frac{d\hat{a}_i}{dt} - \frac{da_i}{dt} \approx \frac{d\hat{a}_i}{dt}.\quad (17)$$

Having chosen $f(\tilde{i}_p) = \text{sign}(\tilde{i}_p)$ and $f(\tilde{i}_n) = \text{sign}(\tilde{i}_n)$, to verify

$$\begin{aligned}\dot{V}_e &= \tilde{i}_p^2 (\lambda_l) + \tilde{i}_n^2 (\lambda'_l) + \text{sign}(\tilde{i}_p) \left[\sum_{i=1}^N (\tilde{V}_{C_i} \cdot \lambda_i) + \lambda_j \cdot \tilde{i}_p \right] \\ &+ \text{sign}(\tilde{i}_n) \left[\sum_{i=N+1}^{2N} (\tilde{V}_{C_i} \cdot \lambda_i) + \lambda'_j \cdot \tilde{i}_n \right].\end{aligned}\quad (18)$$

With some known negative scalars λ_l and λ'_l , which are large enough, can ensure

$$\begin{aligned}\lambda_j \cdot \tilde{i}_p &> \sum_{i=1}^N (\tilde{V}_{C_i} \cdot \lambda_i) \\ \lambda'_j \cdot \tilde{i}_n &> \sum_{i=N+1}^{2N} (\tilde{V}_{C_i} \cdot \lambda_i).\end{aligned}\quad (19)$$

According to the previous design principles, the observer and adaptation gains are defined as $\lambda_j = \lambda'_j = 750$, $\lambda_l = \lambda'_l = -520$, $\lambda_i = 100$, and $\rho_i = -0.124$ to satisfy the fast dynamic response and acceptable convergence characteristics.

Thus, $\dot{V}_e < 0$, which implies that the proposed observer is stable and the capacitor voltages estimation errors converge to 0.

From (16), it can be seen that the estimated capacitor voltages appear in the equation of adaptation rules. It means that the observer equations and adaptation rules are considered and solved together. In other words, the convergence rate for the parameters estimation and capacitor voltages are dependent on the observer and adaptation gains.

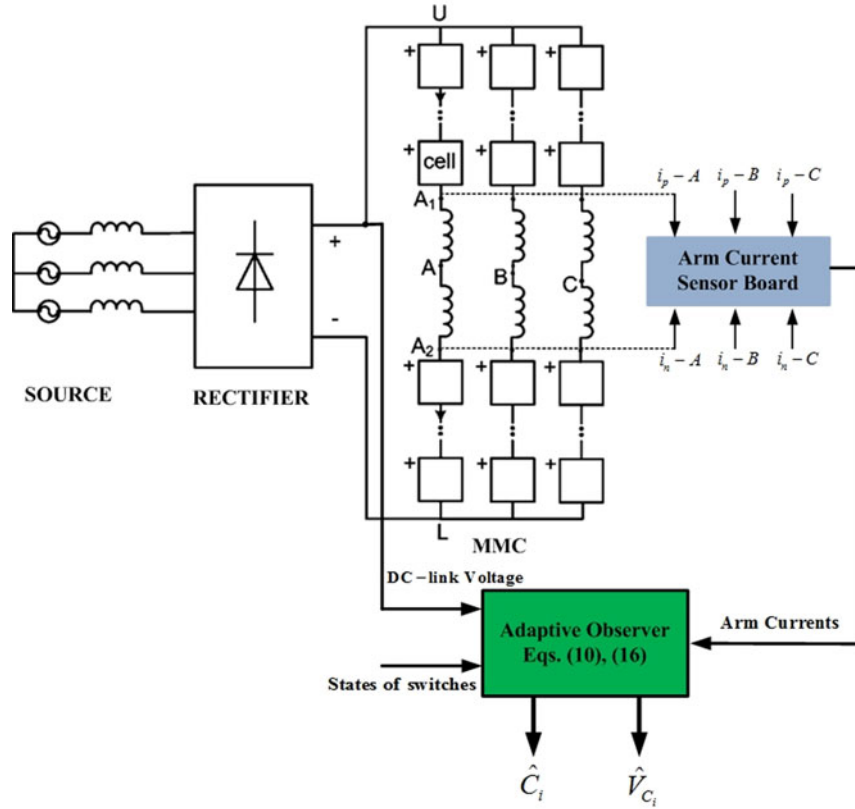


Fig. 7. Overall structure of the MMC with the proposed adaptive observer.

Assuming zero estimation errors for arm currents, the error equations can be stated as

$$0 = \frac{1}{L_1} \left[- \sum_{i=1}^N (S_i \cdot \tilde{V}_{C_i}) \right] + \lambda_j \cdot f_0(\tilde{i}_p) \quad u = a, b, \text{ or } c$$

$$0 = \frac{1}{L_1} \left[- \sum_{i=N+1}^{2N} (S_i \cdot \tilde{V}_{C_i}) \right] + \lambda'_j \cdot f_0(\tilde{i}_n)$$

$$\frac{d\tilde{V}_{C_i}}{dt} = \tilde{a}_i(i_p \cdot S_i) + \lambda_i \cdot f_0(\tilde{i}_p) \quad i = 1, \dots, N$$

$$\frac{d\tilde{V}_{C_i}}{dt} = \tilde{a}_i(i_n \cdot S_i) + \lambda_i \cdot f_0(\tilde{i}_n) \quad i = N + 1, \dots, 2N. \quad (20)$$

Functions $f_0(\tilde{i}_p)$ and $f_0(\tilde{i}_n)$ are obtained by first and second equations in (20) such that

$$0 = \frac{1}{L_1} \left[- \sum_{i=1}^N (S_i \cdot \tilde{V}_{C_i}) \right] + \lambda_j \cdot f_0(\tilde{i}_p)$$

$$0 = \frac{1}{L_1} \left[- \sum_{i=N+1}^{2N} (S_i \cdot \tilde{V}_{C_i}) \right] + \lambda'_j \cdot f_0(\tilde{i}_n)$$

$$\Rightarrow \begin{cases} f_0(\tilde{i}_p) = \frac{1}{L_1 \cdot \lambda_j} \left[\sum_{i=1}^N (S_i \cdot \tilde{V}_{C_i}) \right] \\ f_0(\tilde{i}_n) = \frac{1}{L_1 \cdot \lambda'_j} \left[\sum_{i=N+1}^{2N} (S_i \cdot \tilde{V}_{C_i}) \right] \end{cases} \quad (21)$$

TABLE II
PARAMETERS USED IN SIMULATION

Parameters	Value	Parameters	Value
Rated power	6MW	DC link voltage	10kV
Rated line-line voltage	6.6kV	Maximum modulation index	0.54
Rated current	583A	Number of cells per arm	4
Rated power factor	0.9	Arm inductance	1.2mH
Carrier frequency	1.8kHz	Arm resistance	0.04Ω
Rated frequency	50Hz	Cell capacitance	3.3mF

Substituting the expression (21) into (20) allows expressing the error dynamics of capacitor voltages:

$$\frac{d\tilde{V}_{C_i}}{dt} = \tilde{a}_i(i_p \cdot S_i) + \lambda_i \cdot \frac{1}{L_1 \cdot \lambda_j} \left[\sum_{i=1}^N (S_i \cdot \tilde{V}_{C_i}) \right] \quad i = 1, \dots, N$$

$$\frac{d\tilde{V}_{C_i}}{dt} = \tilde{a}_i(i_n \cdot S_i) + \lambda_i \cdot \frac{1}{L_1 \cdot \lambda'_j} \left[\sum_{i=N+1}^{2N} (S_i \cdot \tilde{V}_{C_i}) \right] \quad i = N + 1, \dots, 2N. \quad (22)$$

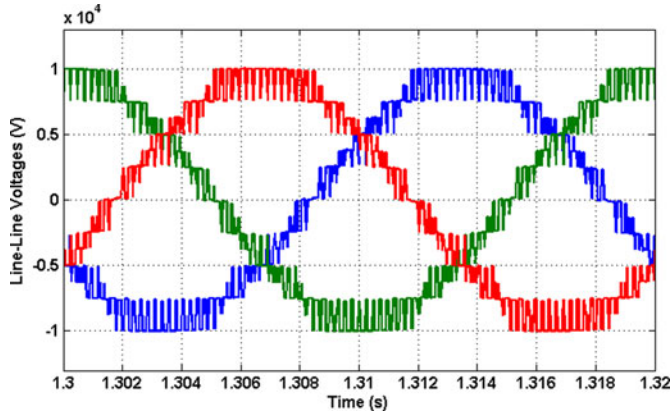


Fig. 8. Simulated three-phase line-line voltage waveforms.

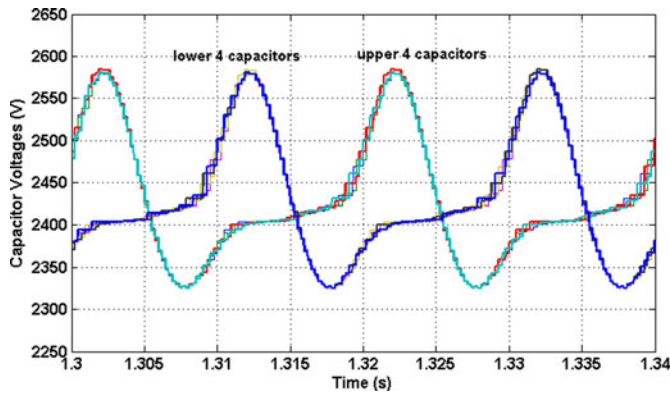


Fig. 9. Simulated eight capacitor voltages.

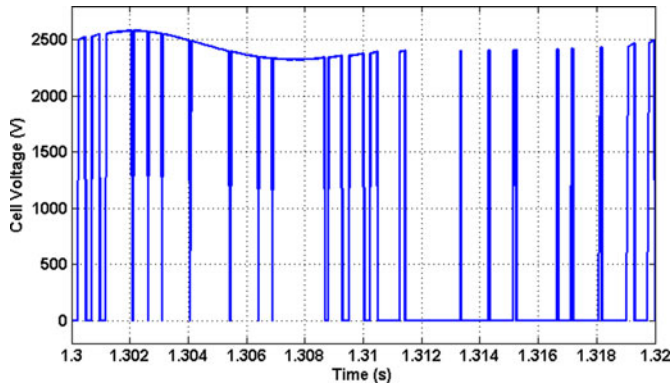


Fig. 10. Output voltage of top cell in phase A.

TABLE III
SPECIFICATIONS OF THE TEST BENCH

Parameters	Value	Parameters	Value
DC link voltage	600 V	Arm inductance	1.3mH
Number of cells in each arm	3	Arm resistance	1 ohm
Rated frequency	50Hz	Cell capacitance	3.3 mF
Carrier frequency	2 kHz	Load resistance	9 ohm
Sampling time	250μs	Load inductance	27mH

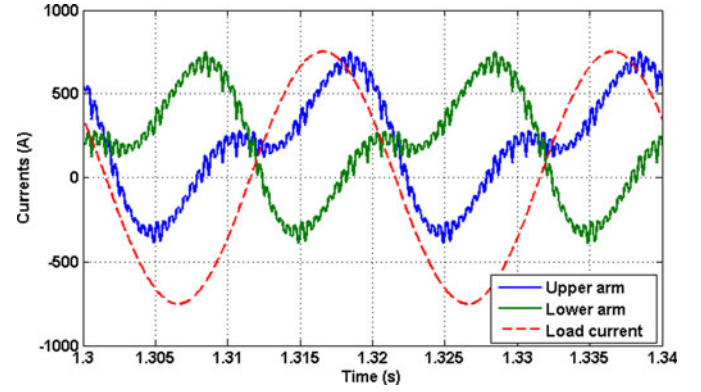


Fig. 11. Simulated upper/lower arm and load currents.

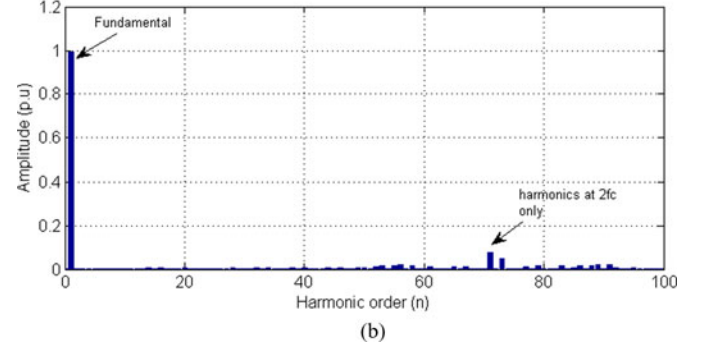
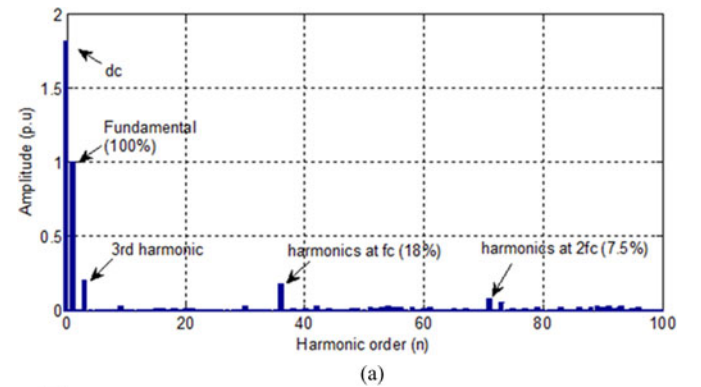


Fig. 12. Harmonic spectrums. (a) Upper arm voltage. (b) Phase voltage.

From (13) and (18), the LaSalle–Yoshizawa theorem [30] guarantees the boundedness of \tilde{a}_i , \tilde{V}_{C_i} and the convergence of the tracking errors to 0 as $t \rightarrow \infty$.

From Barbalat's Lemma [31], we can summarize that the system converges exponentially. In particular, this denotes that the observer errors converge to 0 if the Persistent Excitation condition is satisfied. Therefore, the adaptive observer is asymptotically stable despite the parametric uncertainty.

Theorem 1: $\lim_{t \rightarrow \infty} \tilde{V}_{C_i} = 0$, and $\lim_{t \rightarrow \infty} \frac{d}{dt} \tilde{a}_i = 0$.

A procedure same as the one proposed in the general proof in [31] is used. If there exist $V_e \geq 0$ and $\dot{V}_e \leq 0$, the capacitor voltage and parameter estimation errors are bounded, i.e., $\tilde{V}_{C_i}, \tilde{a}_i \in \ell_\infty$ in which ℓ_∞ depicts the time-domain set of bounded functions. Also, $\lim_{t \rightarrow \infty} (V_e(\tilde{V}_{C_i}(t), \tilde{a}_i(t))) = V_{e_\infty}$ and

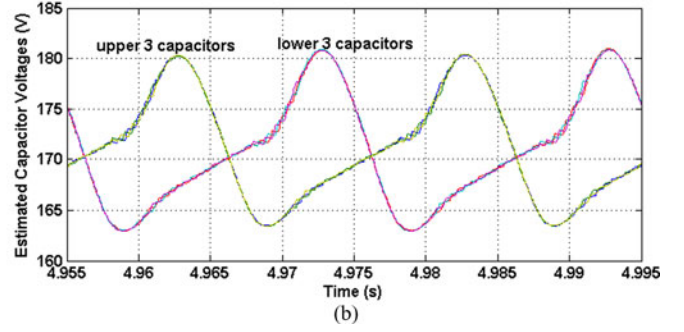
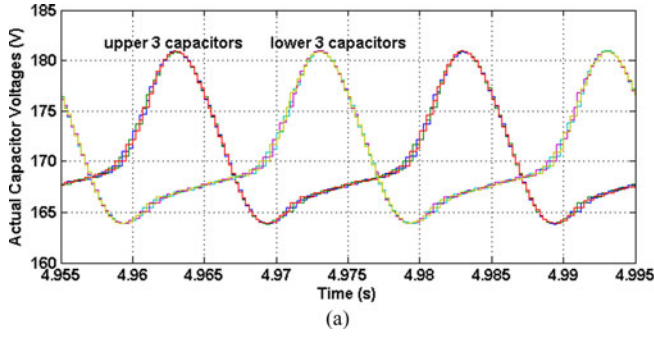


Fig. 13. Capacitor voltages in phase A. (a) Real. (b) Observed.

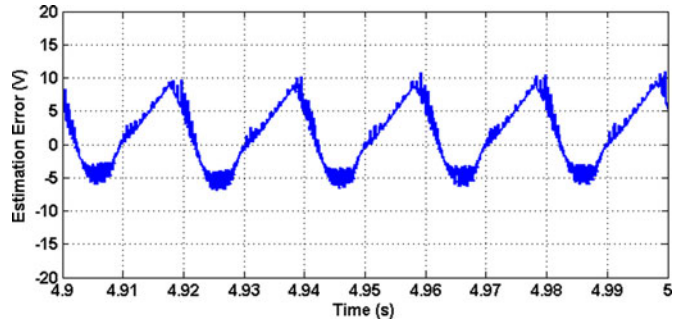


Fig. 14. Capacitor voltage estimation error for top cell in phase A.

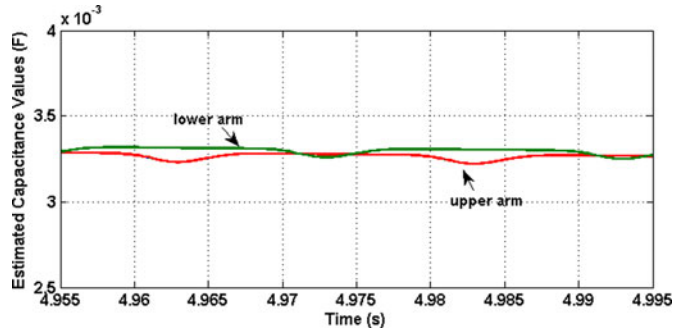


Fig. 15. Capacitance estimation in phase A.

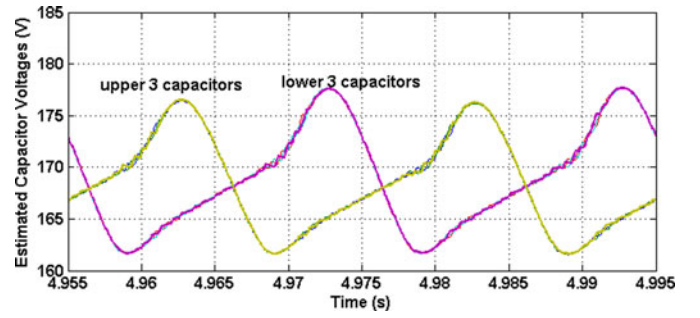
by integration of (11), it follows that:

$$\int_0^{\infty} \|\dot{V}_e\| d\tau = V_e(0) - V_e(\infty), V_e(0) = V_e(\tilde{V}_{C_i}(0), \tilde{a}_i(0)). \quad (23)$$

From (23), it is clear that the voltage estimation error is a square integrable function, i.e., $\tilde{V}_{C_i} \in l_2$, in which l_2 is the set of time domain square integrable functions. Furthermore, from (16), the following inequality holds:

$$\sum_{i=1}^{2N} \left\| \frac{d}{dt} \tilde{a}_i \right\| \leq \sum_{i=1}^{2N} \|\rho_i\| \cdot \|\tilde{V}_{C_i}\| \cdot \|(i_{p,n} \cdot S_i)\|. \quad (24)$$

In other words, $\tilde{i}_{p,n}$ must be bounded because \tilde{V}_{C_i} is bounded. As a result, since $\tilde{V}_{C_i} \in l_2 \cap l_{\infty}$, we have $\dot{\tilde{a}}_i \in l_2 \cap l_{\infty}$. From (11) and $\tilde{V}_{C_i}, \tilde{a}_i, \tilde{i}_{p,n} \in l_{\infty}$ it is easy to see that $\dot{\tilde{V}}_{C_i} \in l_{\infty}$ which, together with $\tilde{V}_{C_i} \in l_2$ denotes that $\lim_{t \rightarrow \infty} \tilde{V}_{C_i} = 0$, and $\lim_{t \rightarrow \infty} \frac{d}{dt} \tilde{a}_i = 0$.

Fig. 16. Estimated capacitor voltages under parameter changes ($L_1 = 1.1L_1, C = 1.2C$) for phase A.

This ends the proof.

A structural diagram of the adaptive observer implemented in MATLAB/Simulink/dSPACE environment is outlined in Fig. 7.

V. SIMULATION RESULTS

To evaluate the performance of the proposed PWM method as well as the validity of the constructed observer performance, simulation results are carried out on a 6.6 kV, 6 MW resistive-inductive load with the nominal parameters given in Table II.

The three-phase line-line voltages are shown in Fig. 8. It clearly reveals the presence of nine levels of voltage, as expected. The charge and discharge of the capacitors cause the voltage levels to vary within acceptable limits.

Fig. 9 displays the eight capacitor voltages of phase A. The sorting algorithm ensures that all the capacitors are fairly balanced at reference voltage (10 kV/4 =) 2.5 kV. They have a voltage fluctuation of around 10% of this value.

In order to examine the effectiveness of the PWM technique, we have shown the voltage across the top cell of phase A in Fig. 10. It shows that the cell switches 18 times in a cycle. This leads to a switching frequency of approximately 1 kHz for the insulated-gate bipolar transistors (IGBTs), which is an acceptable at this rating.

The arm currents and also load current for phase A are shown in Fig. 11. There is a circulating dc which flows through the arms and the dc bus. The dc current helps to maintain the power balance in the capacitors.

The corresponding spectra for aforementioned upper arm voltage and phase voltage waveforms are shown in Fig. 12(a)

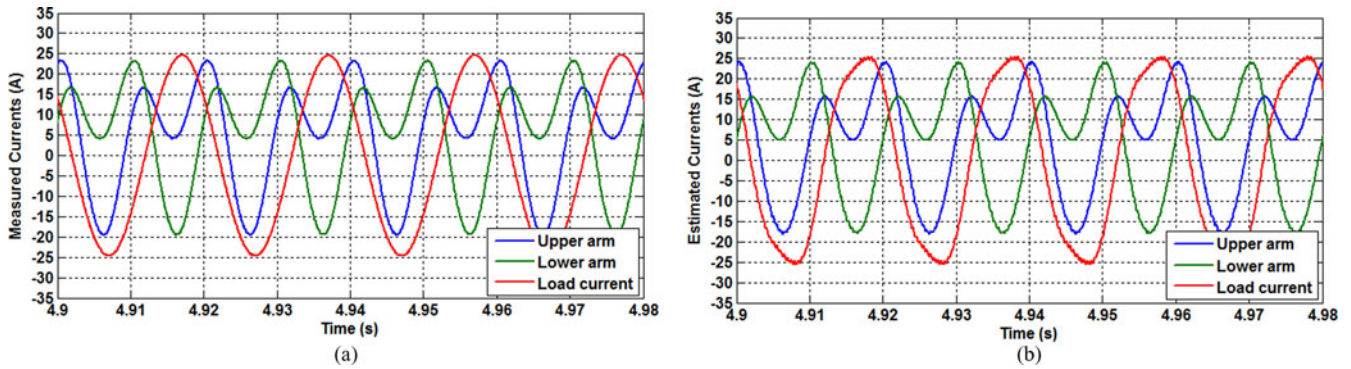


Fig. 17. Upper arm, lower arm, and load currents in phase A. (a) Real. (b) Observed.

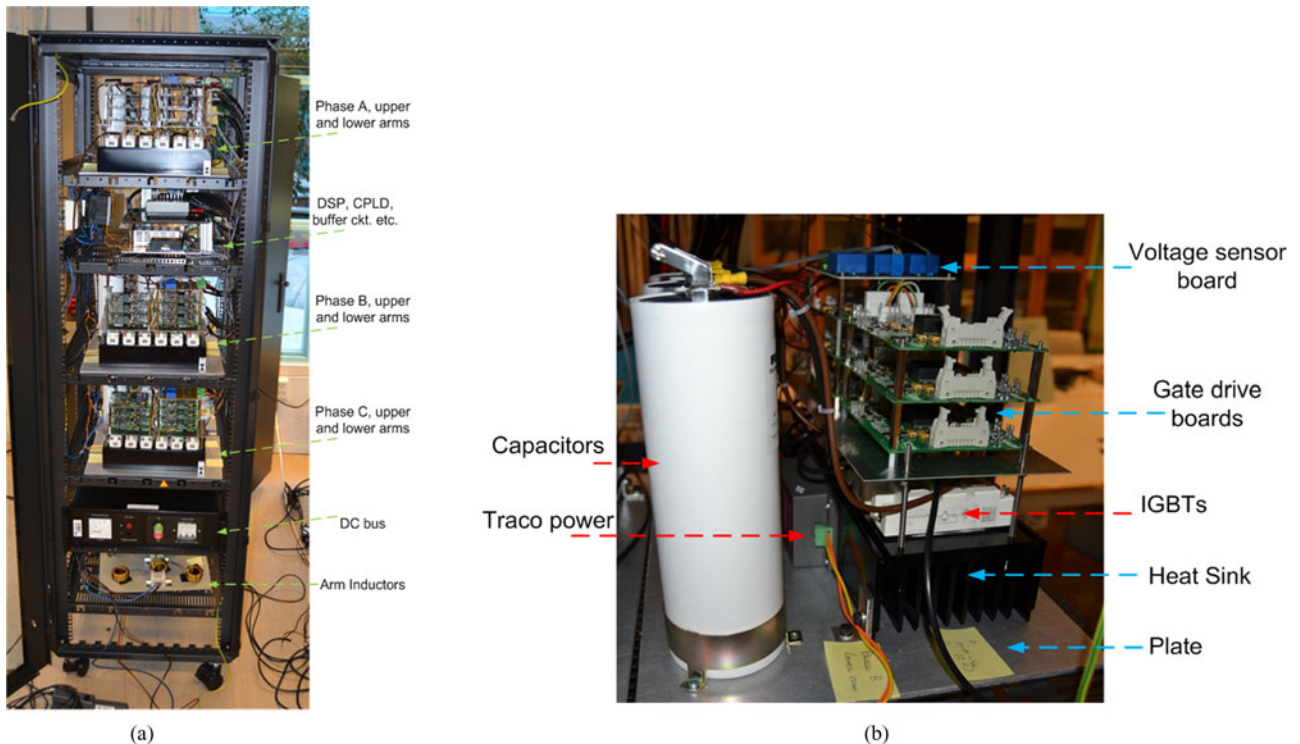


Fig. 18. Layout of the experimental test bench. (a) Overall view. (b) One cell of the MMC showing the different components.

and (b), respectively. The upper arm voltage waveform [see Fig. 12(a)] contains a considerable percentage of switching frequency harmonics. In addition to the dc component, the spectrum comprises a second harmonic component due mainly to the power balance between the upper and lower converters [32]. However, it contains a third (and other triplen) harmonic components, because of the addition of the common mode signal. As seen in Fig. 12(b), the switching frequency harmonics do not appear in the phase voltage spectrum.

Now, to examine the accuracy and robustness of the developed observer based on (10) and (16), some simulation results are presented. These results will be experimentally assessed in the next section. Therefore, the main parameters are the same as the parameters used in the experiments as provided in Table III.

Fig. 13 displays the actual capacitor voltages and estimated voltages in phase A, respectively. As illustrated in Fig. 14, it is clear that the observer has acceptable performance for ca-

pacitor voltage estimations while the voltage estimation error is acceptable.

Furthermore, Fig. 15 presents the estimated capacitance by developed observer which is satisfactory. In steady state, the estimation error compared with the nominal value (3.3 mF) is about 3%.

For evaluating the robustness of the proposed observer with respect to circuit parameters deviations, the arm inductance and dc-capacitance are increased by 10% and 20% of their nominal values, respectively. The efficiency of the observer behavior under impact of a mentioned mismatch is clearly evident from Fig. 16.

In Fig. 17, the estimator performance is shown in more detail. Here, it is possible to see how the estimated currents are similar to the measured ones.

From these figures, it can be verified that the proposed adaptive observer has achieved satisfying performance in spite of

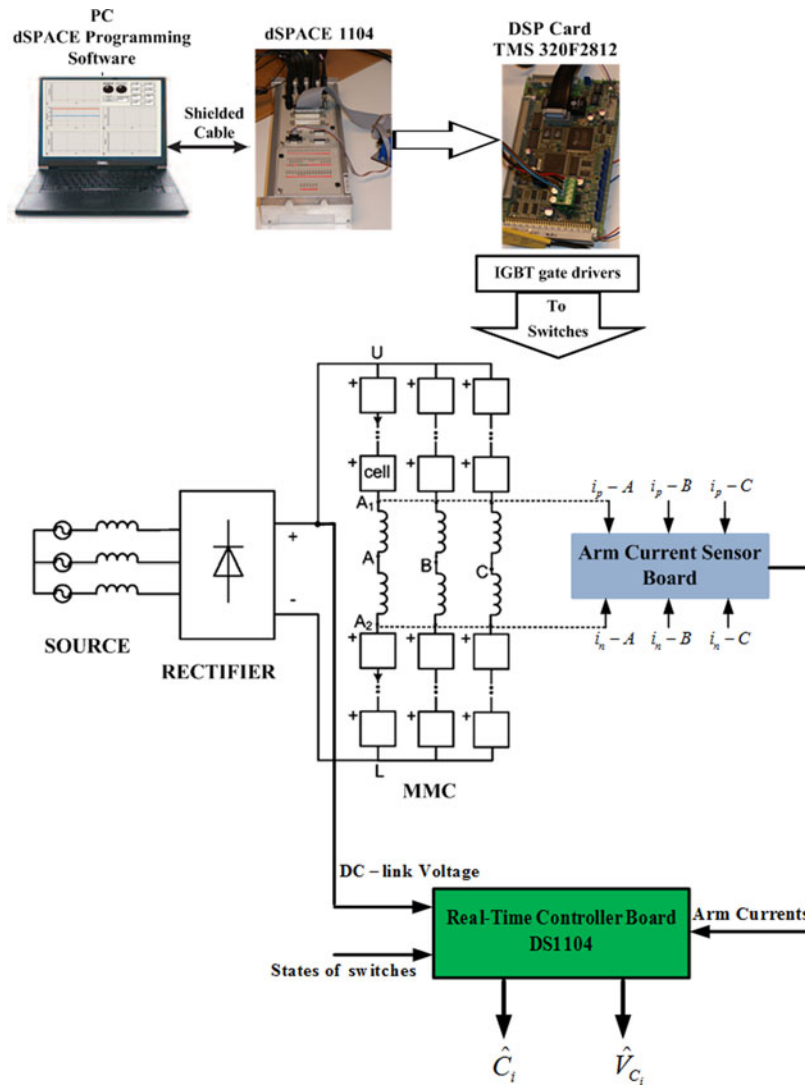


Fig. 19. Schematic diagram of the observer experimental setup with the components.

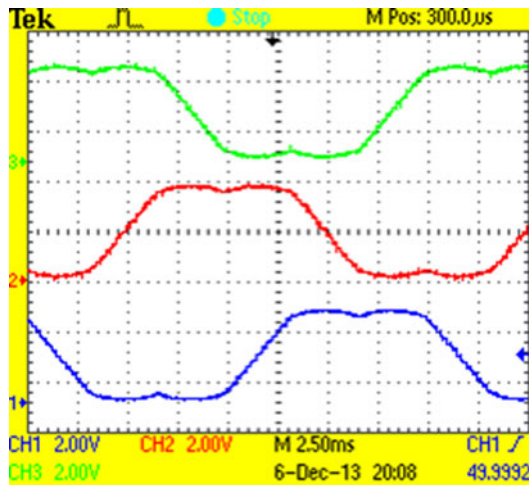


Fig. 20. Experimental reference modulation signals.

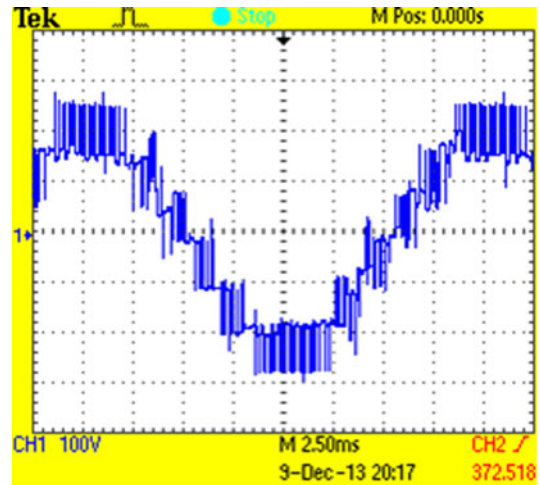


Fig. 21. Experimental waveform of pole voltage V_{A0} .

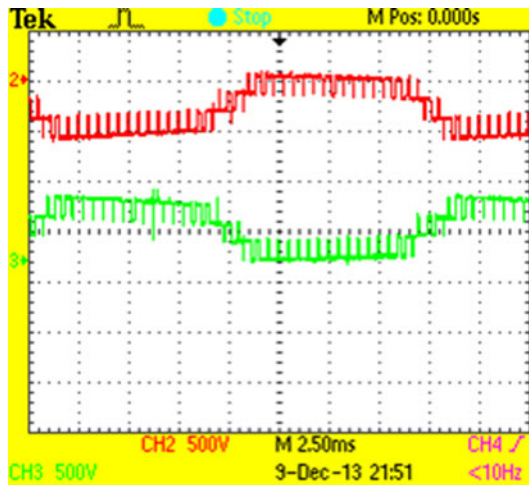


Fig. 22. Measured waveforms of upper (CH2) and lower (CH3) arm voltages for phase A.

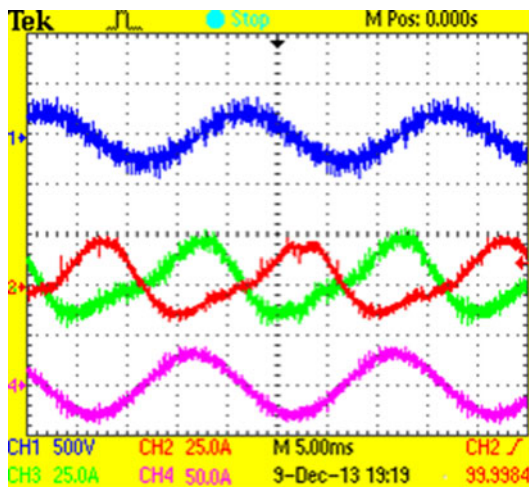


Fig. 23. Measured waveforms of output voltage (top), upper and lower arm currents (the middle plots), and load current (bottom) in phase A.

a mismatched uncertainties consisting of the circuit parameter variation.

VI. EXPERIMENTAL RESULTS

A laboratory setup of a 10 kVA/600 V three-phase MMC has been constructed to verify the operation principle of the proposed PWM strategy previously described. Fig. 18(a) shows the photograph of the laboratory prototype. There are three cells in each arm of the MMC. Each cell is fabricated on a supporting plate with the devices, the gate drivers together on the board and measurements as illustrated in Fig. 18(b). The switches are realized using IGBTs from Semikron (SKM100GB123D). A DSP (TMS320F2812) and an FPGA (XC6V300) have been used as control platform for generating the PWM pulse patterns for the cells, voltage and current sampling as well as coordination of data acquisition. Here, the voltage sensor used is LV-25P from LEM, fabricated on a PCB board to measure the capacitor voltage. The LS-PWM algorithm is performed with a 2 kHz carrier frequency. Power to the dc-link of the converter is provided by

a controllable rectifier. The parameters of the laboratory setup are given in Table III.

In addition, in order to validate the results of the analysis and simulation of an efficient capacitor voltage observer, a schematic diagram shown in Fig. 19 has been implemented. A dSPACE DS1104 controller board is used to carry out the estimator and the real-time algorithm. The observer will work as a software sensor working in parallel with the hardware measurement part. The current and voltage measurements as well as IGBTs gate commands are connected to the DS1104 interface board. Coding of a real-time scheme is conducted using C language through real-time interface library in MATLAB/Simulink Blockset allows compiling the code on processor. The dSPACE ControlDesk software makes it possible to experiment with the real-time application.

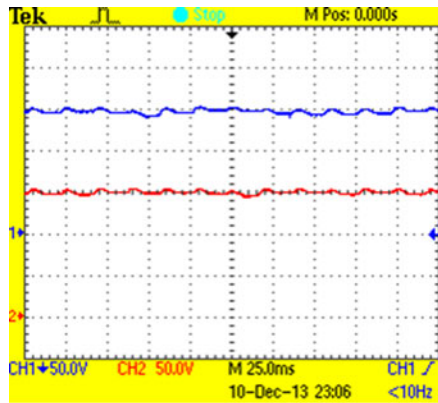
The dc-link voltage is fixed to 520 V. The experiment has been done that aims for an evaluation of the previously simulated PWM method. The actual three modulation waveforms with injection of common mode offset implemented with DSP are given in Fig. 20. The pole voltage waveform of phase A is depicted in Fig. 21 for one cycle. There are seven levels in the voltage waveforms confirming the simulation findings. The PWM voltage is built up of capacitor voltages which are not pure dc, but also have some additional harmonics, especially the second harmonic component, which could cause steep on voltage steps.

Fig. 22 shows the upper and lower arm voltages in converter phase A. It should be pointed out that there are four voltage steps in the waveforms indicating the presence of three cells per arm. The capacitor voltages are well balanced, as seen from the constant and equal steps in the waveform. These waveforms agree with the ideal waveforms presented in Fig. 2. Also, the upper/lower arm currents along with load current and output voltage are shown in Fig. 23. It is evident from the aforementioned results that the experiments provide closely match to those of the numerical simulations.

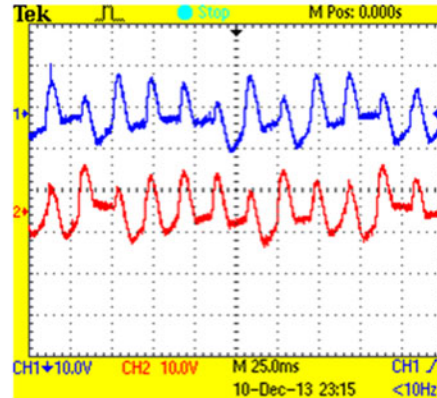
The measured and estimated waveforms of capacitor voltages in phase A top cell, with zoomed version of corresponding ripples, are compared in Fig. 24(a) and (b), respectively, when the dc-link voltage is 450 V. The sorting algorithm ensures that all the capacitors are balanced at $(450/3 =) 150$ V. This comparison exhibits that the capacitor voltages are properly estimated with estimation error converges to small value as shown in Fig. 25. This is also useful to see the observer behavior in case of capacitance estimation. Fig. 26 shows the observed capacitance profile for phase A top cell.

Finally, Fig. 27 shows the experimental waveform for the response of considering parameters mismatched in arm inductance and dc-capacitance values. The ripples around the rated reference voltage for the estimated capacitor voltage in top cell of phase A are detailed in Fig. 27. Therefore, it might be expected that parameter variation within acceptable limits does not have any detrimental impact on the estimation purpose.

It can be concluded that the proposed PWM strategy and estimation scheme are effective in reducing switching frequency as well as capacitor voltage monitoring.



(a)



(b)

Fig. 24. Voltage of capacitor in phase A upper arm. (a) Measured (CH2) and estimated waveform (CH1). (b) Measured (CH2) and estimated (CH1) voltage ripples across capacitor.

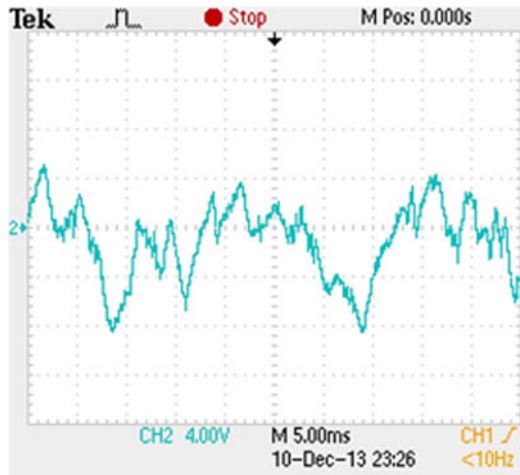


Fig. 25. Estimation error of capacitor voltage for top cell, phase A.

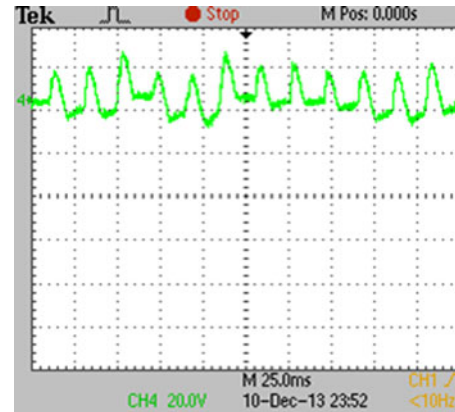


Fig. 27. Estimated ripples of the capacitor voltage in top cell, phase A when subject to parameter uncertainties as $L_1 = 1.1L_1$, $C = 0.8C$.

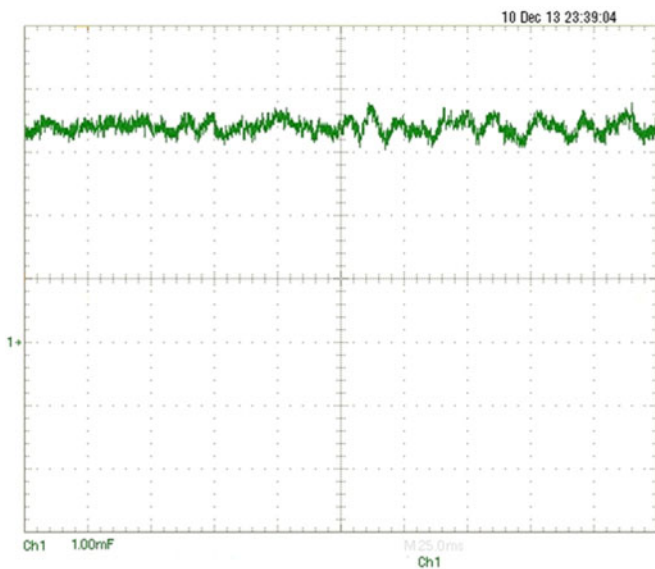


Fig. 26. Estimated waveform of cell capacitance value.

VII. CONCLUSION

This paper has provided an adaptive observer that is able to estimate the capacitor voltages of MMC. The structure of the observer is well adapted since it takes into account the capacitance value of the cell capacitor as a parameter uncertainty. The Lyapunov-based adaptation laws are derived using the stability theory. It is investigated that high observer gains are necessary to achieve observer stability.

The MMC is run using the LS-PWM technique, where the harmonics in the phase voltage are shifted to twice of the switching frequency. A detailed analysis of the PWM strategy used for this purpose has been described in this paper. It utilizes a single carrier and modulating waveforms to determine the duty cycles of individual cells. An interesting feature of this method is that there is no need to calculate the duty cycle of each cell.

Simulation results and experimental tests have confirmed that both strategies are feasible and effective. As a final remark, the findings of this study are applicable for other multilevel converters especially with a modular structure.

REFERENCES

- [1] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Power Tech Conf.*, 2003, pp. 1–6.
- [2] M. Glinka and R. Marquardt, "A new AC/AC multilevel converter family," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 662–669, Jun. 2005.
- [3] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.
- [4] M. A. Parker, L. Ran, and S. J. Finney, "Distributed control of a fault-tolerant modular multilevel inverter for direct-drive wind turbine grid interfacing," *IEEE Trans. Ind. Electron.*, vol. 60, no. 2, pp. 509–522, Feb. 2013.
- [5] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modulation, losses, and semiconductor requirements of modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2633–2642, Aug. 2010.
- [6] M. Hagiwara, I. Hasegawa, and H. Akagi, "Start-up and low-speed operation of an electric motor driven by a modular multilevel cascade inverter," *IEEE Trans. Ind. Appl.*, vol. 49, no. 4, pp. 1556–1565, Jul./Aug. 2013.
- [7] J. Mei, B. Xiao, K. Shen, L. M. Tolbert, and J. Y. Xheng, "Modular multilevel inverter with new modulation method and its application to photovoltaic grid-connected generator," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5063–5073, Nov. 2013.
- [8] D. Montesinos-Miracle, M. Massot-Campos, J. Bergas-Jane, S. Galceran-Arellano, and A. Rufer, "Design and control of a modular multilevel DC-DC converter for regenerative applications," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 3970–3979, Aug. 2013.
- [9] HVDC Plus, Siemens AG. (2010). [Online]. Available: <http://www.energy.siemens.com/hq/en/powertransmission/hvdc/hvdc-plus/>
- [10] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, "VSC-based HVDC power transmission systems: An overview," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 592–602, Mar. 2009.
- [11] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 2903–2912, Oct. 2010.
- [12] J. Peralta, H. Saad, S. Dennerrière, J. Mahseredjian, and S. Nguéfeu, "Detailed and averaged models for a 401-level MMC–HVDC system," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1501–1508, Jul. 2012.
- [13] M. Hagiwara and H. Akagi, "Control and experiment of pulse-width modulated modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1737–1746, Jul. 2009.
- [14] M. Hagiwara, K. Nishimura, and H. Akagi, "A medium-voltage motor drive with a modular multilevel PWM inverter," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1786–1799, Jul. 2010.
- [15] K. Ilves, A. Antonopoulos, S. Norrga, and H. P. Nee, "A new modulation method for the modular multilevel converter allowing fundamental switching frequency," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3482–3494, Aug. 2012.
- [16] Z. Li, P. Wang, H. Zhu, Z. Chu, and Y. Li, "An improved pulse width modulation method for chopper-cell based modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3472–3481, Aug. 2012.
- [17] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Trans. Power Del.*, vol. 26, no. 3, pp. 2009–2017, Jul. 2011.
- [18] A. Das, H. Nademi, and L. Norum, "A pulse width modulation technique for reducing switching frequency for modular multilevel converter," in *Proc. IEEE India Int. Conf. Power Electron.*, Jan. 2011, India, pp. 1–6.
- [19] F. Deng and Z. Chen, "A control method for voltage balancing in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 66–76, Jan. 2014.
- [20] P. Lezana, R. P. Aguilera, and J. Rodriguez, "Fault detection on multicell converter based on output voltage frequency analysis," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 2275–2283, Jun. 2009.
- [21] H. Sheng, F. Wang, and C. W. Tipton IV, "A fault detection and protection scheme for three-level DC–DC converters based on monitoring flying capacitor voltage," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 685–697, Feb. 2012.
- [22] S. Shao, P. W. Wheeler, J. C. Clare, and A. J. Watson, "Fault detection for modular multilevel converters based on sliding mode observer," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4867–4872, Nov. 2013.
- [23] A. Šabanović, "Variable structure systems with sliding modes in motion control—A survey," *IEEE Trans. Ind. Informat.*, vol. 7, no. 2, pp. 212–223, May 2011.
- [24] K. Harada, A. Katsuki, and M. Fujiwara, "Use of ESR for deterioration diagnosis of electrolytic capacitors," *IEEE Trans. Power Electron.*, vol. 8, no. 4, pp. 355–361, Oct. 1993.
- [25] D. Cao, S. Jiang, and F. Z. Peng, "Optimal design of a multilevel modular capacitor-clamped DC DC converter," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 3816–3826, Aug. 2013.
- [26] A. G. Abo-Khalil and D. C. Lee, "DC-link capacitance estimation in AC/DC/AC PWM converters using voltage injection," *IEEE Trans. Ind. Appl.*, vol. 44, no. 5, pp. 1631–1637, Oct. 2008.
- [27] D. Basic, F. Malrait, and P. Rouchon, "Euler-Lagrange models with complex currents of three-phase electrical machines and observability issues," *IEEE Trans. Autom. Control*, vol. 55, no. 1, pp. 212–217, Jan. 2010.
- [28] R. S. Kanchan, M. R. Baiju, K. K. Mohapatra, P. P. Ouseph, and K. Gopakumar, "Space vector PWM signal generation for multi-level inverters using only the sampled amplitudes of reference phase voltages," *IEEE Electr. Power Appl.*, vol. 152, no. 2, pp. 297–309, Mar. 2005.
- [29] A. Isidori, *Nonlinear Control Systems*, 3rd ed. Berlin, Germany: Springer-Verlag, 1995.
- [30] J. E. Slotine and W. Li, *Applied Nonlinear Control*. Englewood Cliffs, NJ, USA: Prentice-Hall, 1991.
- [31] M. Krstic, I. Kanellakopoulos, and P. V. Kokotovic, *Nonlinear and Adaptive Control Design*. New York, NY, USA: Wiley, 1995.
- [32] H. Peng, M. Hagiwara, and H. Akagi, "Modeling and analysis of switching-ripple voltage on the DC link between a diode rectifier and a modular multilevel cascade inverter (MMCI)," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 75–84, Jan. 2013.



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