Modular Multilevel Converter With Series and Parallel Module Connectivity: Topology and Control

Stefan M. Goetz, Angel V. Peterchev, and Thomas Weyh

***Abstract*—This paper introduces a novel modular multilevel series/parallel converter that allows switching modules dynamically not only in series, as in the traditional modular multilevel converter (M2C), but also in parallel. As in M2C, the semiconductor voltages do not exceed the module capacitor voltage for any module state. While the new topology is a generalization of M2C and could, therefore, be operated identically to it, the additional states provide degrees of freedom that the controller can dynamically employ to achieve several advantages. Whereas in M2C many modules are bypassed if the instantaneous converter voltage is lower than the system's peak voltage, the parallel connectivity enables these modules to contribute to the current load, thus reducing conduction losses. In addition, the parallel configuration of modules can be used for balancing the modules' state of charge (SOC). The parallelization losses are moderate or negligible, dependent on the switching rate. Since the parallel connection of capacitors can ensure balancing, it enables stable operation of a multilevel converter without the need for monitoring the module SOCs. While such economical control hardware may be appropriate for low-power systems, we also present more sophisticated control that uses the additional degrees of freedom to minimize losses. Finally, we point to further extensions of the circuit topology to multipole module connectivity that could enable additional functionality and applications.**

***Index Terms*—AC-AC power converters, ac-dc power converters, battery management systems, converters, dc power systems, topology.**

I. Introduction

A. Background and Applications of Multilevel Converters

MODERN multilevel converter technology is a product of the technical requirements for switching very high voltage levels. Semiconductor-based power electronics solutions need balanced portioning of the total voltage to a number of switches with lower voltage rating [1]. While early two-point voltage-source converters switched the entire voltage in one step [2], [3], multilevel approaches were developed to change the terminal voltage in fractions [4] so that they can approximate sinusoidal shapes, for instance, with a staircase.

The high power quality of multilevel converters is essential for many purposes [5], [6]. Presently, most common applications are high- and ultrahigh voltage facilities, such as for high-voltage direct-current (HVDC) transmission lines. Due to the limitations of conventional systems, multilevel HVDC currently acts as key application and technology driver. Traditional line-commutated thyristor-valve technology requires large and expensive filter facilities for power quality and correct commutation [7], [8]. Substantial progress has been made with self-commutated voltage-source converters with two-level [3], [9] and first three-level systems [10]–[13] in the last two decades, but the power quality and the electromagnetic emissions are still suboptimal and require filters. Multilevel approaches with a sufficiently fine resolution of the voltage, in contrast, can fully omit such filters [14]. A first commercial HVDC line with a fine voltage quantization provided by a multilevel converter has been in operation successfully for three years without major failures [15], [16]. Accurate control over the voltage may also be an important aspect for dc grids [17]. In addition to transmission-line converters, multilevel technology plays an important role in static synchronous compensators (STATCOM) [18], [19].

For drives in the large- and medium-power range, multilevel converters can provide a higher power quality, including a better power factor; lower dielectric stress on the insulation; less harmonic content with accordingly lower eddy current losses; and diminished common-mode problems [20], [21]. Most recent applications are solar inverters [22]–[25], wind turbine converters [26]–[30], as well as marine [31] and automotive propulsion [32]–[37].

In addition to these examples where it outperformed traditional electronics, multilevel converter technology can deal with so far unsolved problems, such as high-frequency, high-power pulses with freely controllable temporal shape as in noninvasive magnetic brain stimulation [38], [39]; similar requirements have to be met in plasma applications which demand high dynamics and short response times [40]–[47].

In low- and medium-voltage applications, multilevel converters enable the use of low-cost components with lower voltage ratings that are produced commercially at higher quantities than high-voltage components. First, field-effect transistors (FET) can replace IGBTs [36], [48]. The faster dynamics of FETs can reduce the switching losses, while the linear current–voltage relation around zero due to the almost ohmic behavior of FETs in contrast to the pn forward voltage of IGBTs allows, in principle, an almost unlimited reduction of conduction losses by parallelization. Second, electrolytic and ceramics capacitors can replace film capacitors and increase the capacitance while reducing the volume [38].

B. State-of-the-Art Modular Multilevel Converter (M2C)

Several multilevel converter topologies have been proposed. Most discussed among them are the neutral-point-clamped

Manuscript received September 30, 2013; revised January 13, 2014; accepted February 18, 2014. Date of publication March 11, 2014; date of current version August 26, 2014. Recommended for publication by Associate Editor Z. Xu.

S. M. Goetz is with Duke University, Durham, NC 27710 USA and also with TU Muenchen, 80333 Munich, Germany (e-mail: stefan.goetz@duke.edu).

A. V. Peterchev is with Duke University, Durham, NC 27710 USA (e-mail: angel.peterchev@duke.edu).

T. Weyh is with the Universitaet der Bundeswehr Muenchen, Neubiberg 85579, Germany and also with TU Muenchen, 80333 Munich, Germany (e-mail: thomas.weyh@unibw.de).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2014.2310225

topology [49] as well as its active counterpart [50], the flying-capacitor topology [1], the M2C [51], [52], and several designs for special applications, such as the multilevel modular capacitor-clamped dc–dc converter [53].

Among other designs, M2C stands out because of its structure, which consists of cascaded identical modules. The key principle of M2C is splitting the total voltage into small steps so that the high total voltage can be handled by N functionally independent low-voltage modules. Every module consists typically of an H-bridge connected to a capacitor, forming the microtopology. Through the H-bridge, the module capacitor is either connected in series to its neighbors, increasing the total voltage by one step, or bypassed in the inactive module state. The modules—each acting as an independent voltage source—are cascaded to form the arms of a larger H-bridge, the macrotopology [51]. This structure entails a number of unique advantages.

1) Every arm consisting of a number of cascaded H-bridges forms a dynamically balanced voltage divider. Within a module, the components (active semiconductor switches, diodes, and capacitors) can have a relatively low voltage rating. In addition, balancing the state of charge (SOC) of the capacitors in the single modules is easier and puts fewer constraints on the terminal voltages than in other multilevel topologies.
2) The modular design of practically independent sources enables scalability of the total voltage rating.
3) The scalability allows incorporating redundancy for higher reliability by adding additional modules so that a failure of one module can be seamlessly compensated by another one.
4) The modularity reduces complexity and allows a quick design of customized converters based on the same platform and modules.
5) For changing the total voltage of a converter arm by one step during operation, only a minimum number of modules and therefore of semiconductors has to be switched so that switching losses are relatively low.
6) With the H-bridge module design, multilevel converters can be made short-circuit proof, e.g., in power line converters, with respect to both ac and dc terminals [54].
7) If pulse-width modulation is applied, switching is usually performed on a single amplitude quantization step (single module voltage) and can be sequentially rotated through all available modules [55]. For a low individual module- and transistor-switching rate, the effective overall switching rate as the sum of the latter can overcome dynamical limitations of semiconductors and easily extend to the radio frequency range.

The fixed series connection of the M2C modules entails, however, some limitations. While the total voltage is split into small units and distributed among the modules, the current is not. Each module conducts the full current. Thus, in the inactive bypass mode, the module does not contribute to the output power but only increases the converter's parasitic inductance and resistance. At low voltage amplitudes, e.g., in the periods between the peaks of an alternating sine waveform, most modules are in the inactive bypass state and are, therefore, unused but contribute losses. The highest possible load factor of $f/(2\pi)\int_0^{2\pi/f}|\sin(2\pi tf)|\,dt = 2/\pi < 64\%$ for a sinusoidal voltage waveform with frequency f is rarely achieved in real systems, which are typically derated for robustness and availability. The negative impact of the series connection of the modules is further aggravated when additional modules are included for redundancy in high-availability systems, resulting in increased losses.

Recently, a module design was introduced that enables a dynamical change between a series and a parallel connection of distinct capacitors within a single module [56]. However, parallelization is not possible across modules. Furthermore, the design is limited to monopolar, two-quadrant modules so far.

C. Novel Modular Multilevel Series/Parallel Converter (M2SPC)

We introduce a novel M2SPC topology, which is a generalization of the traditional M2C topology as it allows not only series but also parallel connections among modules. Our motivation is to use productively inactive modules and particularly their integrated energy storages instead of bypassing them. While they cannot contribute to the voltage of an arm, they could take over some of the current load from active modules and consequently reduce the total parasitic inductance and resistance. Whereas a parallel option could be easily incorporated using a matrix structure of modules, we want to comply with the fundamental feature of M2C that the highest voltage level for all components within a module is limited. Thus, the resulting M2SPC topology is a generalization with the M2C as one subset.

We furthermore propose a novel control scheme that combines the switching modulator and the SOC balancing method. Existing approaches, in contrast, treat the switching modulation and balancing as separate functions. The novel combined approach can also be applied, as an extension, to the traditional M2C.

Finally, we point to further extensions of the circuit topology to multipole module connectivity that could enable dc-dc conversion and filtering functions between modules, potentially improving efficiency and inductive energy handling in some applications.

II. M2SPC Topology

A. Microtopology

The integration of a parallel option in M2SPC affects both the microtopology, i.e., the circuit of a single module, and the macrotopology, i.e., the circuit comprising all modules. The constraint that all voltages within a single module must be limited to the capacitor voltage level for any switching state implies that the structure has to be a serial one. This means that every module is still connected only to its immediate neighbors.

Fig. 1 shows the M2SPC microtopology. In contrast to M2C, the module is no longer a two-pole element, but provides four terminals, two for each neighbor. This doubling of terminals corresponds to a split of each connection between modules into two connections. Every terminal is connected to the module

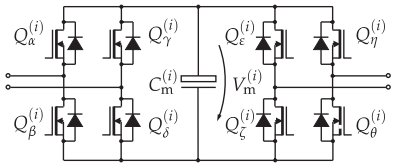


Fig. 1. Module topology (microtopology) of the M2SPC. The module comprises a capacitor that can be polarized and four half-bridges connected to it. Accordingly, each module has four connection terminals.

capacitor via a half-bridge formed by two semiconductor switches. In consequence, every neighbor of a given module has access to both sides of the capacitor at the same time for a parallel mode.

Of the $2^8 = 256$ states allowed by the eight switches, nine will be of particular interest here. These nine module states include all states of the traditional M2C microtopology. For the traditional four M2C module states (i.e., positive series, negative series, active 0 V, and passive [57]), the two terminals connecting a module to a neighbor are operated identically to behave like a single line. In the five new states, the two lines leading to a neighbor can be split. While one terminal is connected to the positive pole of the capacitor, the other terminal is connected to the negative capacitor pole, allowing a parallel connection with the capacitor in its neighbor.

Fig. 2 illustrates the nine module states of interest applied to three neighboring modules. The additional states entail a number of advantages for a strand of modules. In the traditional M2C, an individual charged module capacitor can only be added in series to the strand or bypassed without using it. The new states allow connecting such a bypassed capacitor in parallel to one or both of its neighbors. Consequently, the current rating of the strand increases, especially for low voltages, where most of the module capacitors are not required for achieving the voltage level, but are available for the parallel mode. In contrast, most of the module capacitors would be bypassed (unused) in the traditional M2C topology. In addition, the time-averaged internal resistance of the strand decreases. The reduction is most considerable in small- and medium-voltage multilevel converters in which electrolytic capacitors are the bottleneck for the internal resistance. Applications with high inductive load, where highest currents occur during low-voltage time intervals, such as STATCOMs, benefit particularly from the parallel mode.

Importantly, although Fig. 1 features twice as many distinct switches as a conventional M2C H-bridge, it requires exactly as many power semiconductors. The reason is that in every state, the current is distributed between two switches. For the same resistance, a switch can accordingly be implemented by only half of the discrete semiconductors, in case a semiconductor module is used, or by a smaller single device.

As indicated by the list of module states, the traditional M2C comprises a subclass of these states and is, therefore, a special case of the novel M2SPC topology. Thus, if the additional flexibility is temporarily not wanted, M2SPC converters can be operated identically to M2C systems. Section V-C further generalizes the module topology to n-poles.

B. Macrotopology

The macrotopology, i.e., the assembly of single modules to form an entire converter, can use traditional structures, dependent on the application. For simultaneous bidirectional power conversion among a number of terminals or phases, the Marquardt topology can be marginally modified [51].

In the Marquardt topology, modules are connected in strands, called converter arms (see Fig. 3). Two such strands with two ends and a center tap, in turn, form a so-called phase module or phase unit [51]. For a converter with p terminals or phases, $(p-1)$ phase modules are connected at their ends. Each of the center taps and the two end points, where all converter arms meet, form the terminals of the converter. For instance for a typical HVDC converter, which has to supply three ac terminals and a dc line with two connections, three phase modules with a total of six converter arms are sufficient. The three center taps of the phase modules connect to the ac terminals, while the two ends where the three phase modules meet feed the dc line.

Similar to the traditional M2C, the single modules of the M2SPC are strung together in converter arms and phase modules [see Fig. 3(a)]. In contrast to the M2C, the individual modules of the M2SPC have the described two interconnections reaching from one module to the next. At every terminal of the converter, where at least two converter arms meet, there are several connection options. While the converter arms—just like the modules—share two lines, which were introduced to enable parallel module connectivity, typical terminals have only a single connection. The determinant for the preferred solution is if modules should be able to establish parallel connections between separate converter arms.

If parallel connections of modules belonging to different converter arms are required, the dual-line connection can be kept. The terminal is connected to only one of the two lines [see right configuration in Fig. 3(b)]. The marginal modules terminating with one side at such a parallel terminal operate with respect to all their neighbors just like any module within a converter arm using the nine states shown in Fig. 2. For the traditional module states [states (a) to (d) in Fig. 2], the voltage of the terminal and therefore the voltage of a single converter arm is identical to the traditional M2C. In contrast, for the parallel states [states (e) to (i) in Fig. 2], the marginal module increases, reduces, or does not influence the arm voltage presented to the terminal, depending on which of the two intermodule connections forms the terminal.

If parallel connections of modules belonging to different converter arms are not necessary, the two lines connecting the two adjacent converter arms and the terminal can be shorted forming one terminal [see left configuration in Fig. 3(b)]. Accordingly, the marginal modules of a converter arm forfeit three states due to the missing parallel connections on one side, and the single converter arms can be treated separately to reduce complexity. Although we will concentrate on this case, several applications may reasonably benefit from parallel connectivity across converter arm limits.

As discussed in Section I, M2C topologies for medium-voltage high-current applications have particular importance for

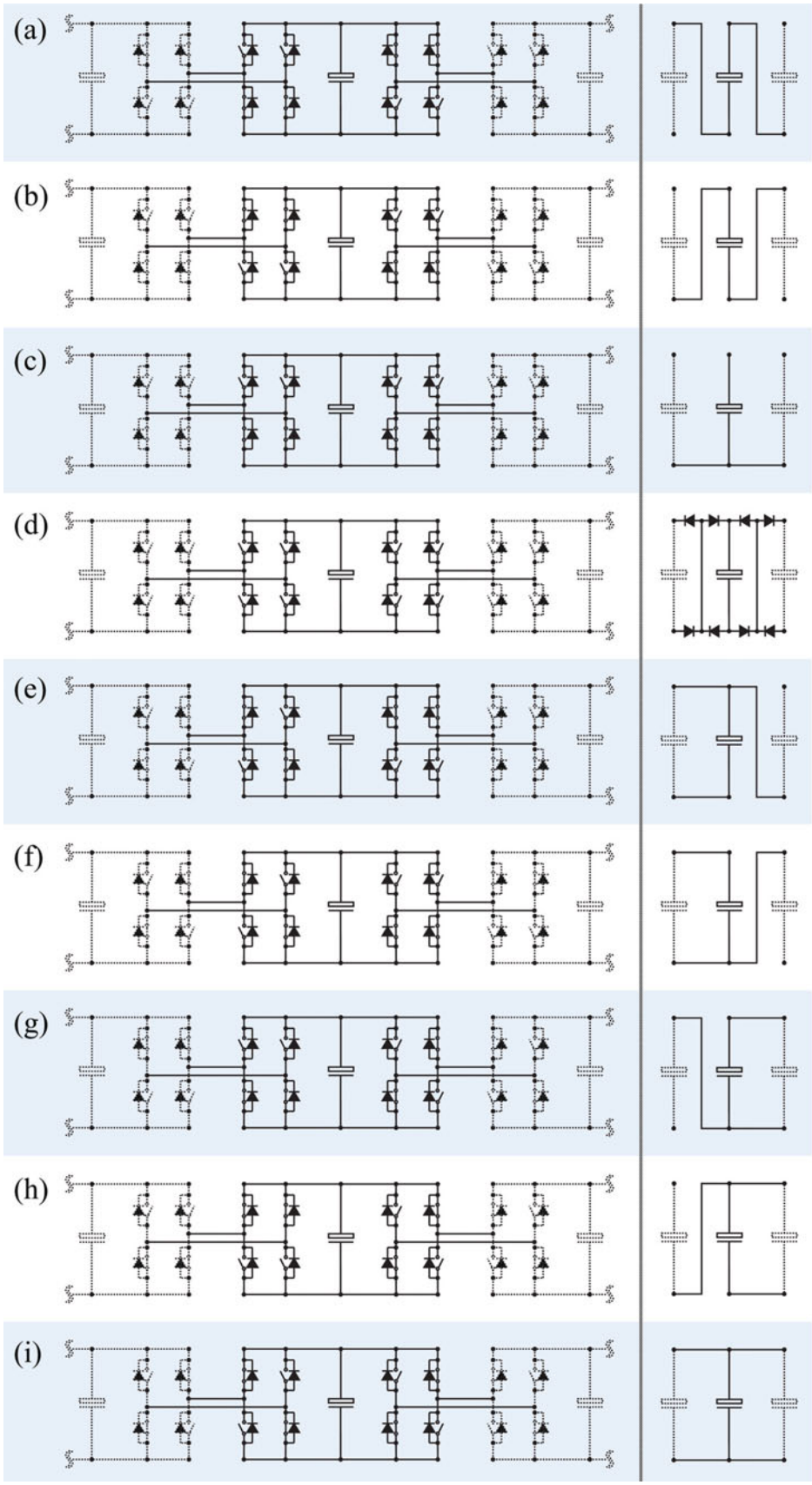


Fig. 2. Switching states of an M2SPC module. The module is shown between its two neighbors in the left column. The right column represents the corresponding idealized connection scheme. The states are (a) serial connection with positive polarity; (b) serial connection with negative polarity; (c) bypass state enforcing active zero voltage; (d) passive state, reverse diodes enforce rectification; (e) parallel on the left side, positive polarity; (f) parallel on the left side, negative polarity; (g) parallel on the right side, positive polarity; (h) parallel on the right side, negative polarity; and (i) parallel on both sides.

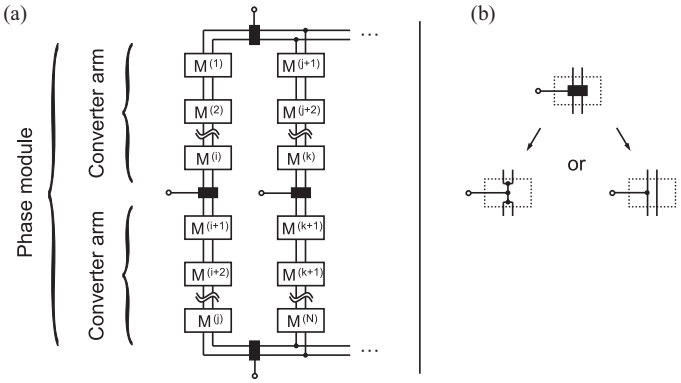


Fig. 3. M2SPC uses a Marquardt macrotopology modified to include parallel connectivity (a). Strands of cascaded modules form converter arms. Two converter arms form a phase module with a converter terminal in between. For p terminals, a converter requires $(p-1)$ phase modules. For the parallel module states, two lines are connecting neighboring modules. In case parallel connections are desirable across converter arms, the two-line scheme can be kept consistently throughout the macrotopology. In that case the converter terminal is connected to just one of the two lines; otherwise, the two lines can be shorted to form a terminal (b).

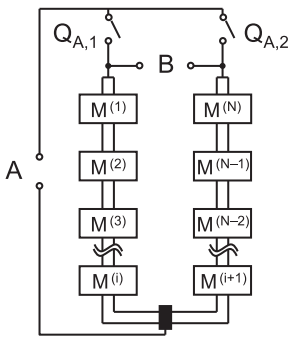


Fig. 4. Alternative M2SPC macrotopology. For some applications, such as pulse generation or dc systems, four-quadrant operation is not required simultaneously at all converter terminals, while the terminals have to handle significantly different voltage levels. The disconnectors $Q_{A,1}$ and $Q_{A,2}$ do not have to be fast nor do they need to have circuit-breaker capabilities. As in the modified Marquardt topology in Fig. 3, the parallel connectivity between converter arms can be maintained or terminated as shown in Fig. 3(b).

pulse generation, especially the synthesis of short nonsinusoidal current or voltage pulses [38], [58], [59]. These applications may require bidirectional four-quadrant operation for both the power line and the pulse terminals. However, these terminals are usually not operated simultaneously so that a simplified topology can be used (see Fig. 4). The two converter arms combined with two disconnectors can freely synthesize a wide variety of pulses for resistive or reactive loads. Recharging from and discharging of energy to the power line can be performed freely while no pulses are released. The disconnectors $Q_{A,1}$ and $Q_{A,2}$, which can be exclusively operated with zero-current switching, alternate between terminals A and B. For example, parallel connections between converter arms are highly favorable for high-power pulse generation due to the intense peak current load.

In addition to pulse synthesis, the topology in Fig. 4 qualifies well for applications that transfer energy between terminals of very different voltage levels. Specifically, the voltage level of Terminal B is higher than that of Terminal A by a factor of two.

III. Control and Balance

A. Preliminary Considerations

Although the novel multilevel converter M2SPC does not require more power semiconductor material compared to an equivalent traditional M2C, the additional module states add complexity. Each module has about twice as many states; for an entire converter with N modules, this leads to $(9/4)^N$-times as many states as those of an M2C.

A key requirement for the control method is to balance the SOCs of all modules so that none of them depletes and causes instabilities or a crash of the converter. In addition, it has to keep the losses low while providing the specified voltage for every terminal.

While the traditional M2C has to balance the module SOCs exclusively by controlling the energy flow into and out of every module, the M2SPC provides an additional means. It can clear SOC differences with the parallel mode—although the primary task of parallelizing is to increase the current rating. Every such clearing procedure is associated with electrical losses. However, these losses can be reduced to be notably below the level of resistive losses, as shown below.

Important for the losses is the imbalance of the SOCs, quantified by the module voltages $V_{\mathrm{m}}^{(i)}$, where $i = \{1,\ldots, N\}$. The worst case, i.e., the highest voltage difference ΔV between two modules, develops if one module is bypassed while the other one is either active positive or negative without any other module in parallel to it, which would slow the charge/discharge dynamics down. For a module capacitance $C_{\mathrm{m}}^{(i)}$ of the active module and an arm current I, the difference building up within a duration of *dt* is proportional to the duration and limited by

$$\Delta V = \int \frac{I(t)}{C_{\mathrm{m}}^{(i)}} dt \leq \max_{[t,t+dt]} I \cdot \frac{dt}{C_{\mathrm{m}}^{(i)}} \propto dt. \tag{1}$$

If N modules with individual capacitance $C^{(i)}$ and module voltage $V_{\mathrm{m}}^{(i)}$ are cleared by parallelizing them, their final voltage V_{eq} is

$$V_{\mathrm{eq}} = \frac{\Sigma_i C_{\mathrm{m}}^{(i)} V_{\mathrm{m}}^{(i)}}{\Sigma_i C_{\mathrm{m}}^{(i)}} \tag{2}$$

while the loss due to that procedure amounts to

$$\Delta E^{(N)} = \frac{1}{2}\left(\Sigma_i C_{\mathrm{m}}^{(i)} \left(V_{\mathrm{m}}^{(i)}\right)^2 - \frac{\left(\Sigma_i C_{\mathrm{m}}^{(i)} V_{\mathrm{m}}^{(i)}\right)^2}{\Sigma_i C_{\mathrm{m}}^{(i)}}\right). \tag{3}$$

For connecting two modules that do not have equal SOC, this can be simplified to

$$\Delta E^{(2)} = \frac{1}{2}\frac{C_{\mathrm{m}}^{(1)} C_{\mathrm{m}}^{(2)}}{C_{\mathrm{m}}^{(1)} + C_{\mathrm{m}}^{(2)}} \Delta V^2 \propto (Idt)^2. \tag{4}$$

The combination of (1) and (4) for the worst case shows that the maximum loss is independent from the absolute voltage

and is directly proportional to dt^2. In consequence, the interval between leveling by parallelization should be kept short. Particularly for pulse-width modulation with high switching frequencies, modules are constantly added, i.e., switched into the positive or negative series mode, and removed, i.e., switched to the bypass or parallel mode, so that every such state transition can be used to balance modules. With appropriate control methods, high overall switching frequencies can be achieved with low switching frequencies of each individual module [55].

For example, in an IGBT converter with a peak current of 1000 A, two modules with $C_m = 10$ mF can build up a maximum voltage difference of $\Delta V = 1$ V within 10 μs. For a moderate saturation forward voltage per IGBT of $V_{\mathrm{ce,sat}} = 1.5$ V, the conduction loss of at least 60 mJ dwarfs the balancing losses of 2.5 mJ by a factor of 24. For a longer interval of 100 μs, the conduction losses still exceed the losses of a potential parallelization by a factor of 2.4. However, this assumes that balancing is performed exclusively by parallelization, while real systems control the balance also by the load of the single modules. For systems with FET switches, the ratio of conduction to parallelization losses is further increased due to the higher switching speed, as demonstrated with simulations in Section IV.

The nonlinearity in losses (ΔV^2) shows that for balancing a converter arm exclusively by parallelization, the order in which the modules with different SOC are parallelized has fundamental influence on the losses—although their final balanced voltage is approximately the same for all sequences. For minimum losses, those modules with smallest voltage difference should be parallelized first.

B. Charge Balance

Our preferred control scheme is inspired by the typical balancing approach for M2C converters [51], [52]. The traditional M2C strategy controls the SOC of the single modules by accounting of their energy inflows and outflows. The additional parallel state of the M2SPC changes the strategy in two ways. First, parallelization can balance modules and does not require a load current flowing across the entire converter. As shown above, the losses fall quadratically (ΔV^2) for small voltage differences and can, therefore, be mastered. Second, units of parallel modules have a higher effective capacity and slow down the charge and discharge rate of the involved modules. Consequently, the charge/discharge rates can be different for each module dependent on the dynamic module configuration, but are slower on average than in M2C modules for the same module capacitance.

The key task of the control scheme is maintaining balanced SOCs and an appropriate module scheduling. The voltage regulation, in contrast, which determines how many modules are required in a converter arm, is performed separately by the modulator as in most M2C systems with known methods, e.g., as staircase in fundamental-frequency switching [51], [60], [61] or with high-frequency switching modulation [55], [62]–[64]. Further, the control strategy can implement methods to enhance robustness against typical fault or imbalance conditions in power systems, such as to suppress zero-sequence components without the need for a transformer [65], or to suppress circulating currents between different arms [66].

At the beginning of every switching period, the control scheme checks the following rules for setting the module states in a converter arm.

Case A: The absolute voltage has to be reduced by one module step.

1) If energy is flowing into the modules (i.e., the product of current and voltage from the source perspective is negative).
   a) Search among all modules that are active in series for the one with the highest SOC, i.e., module voltage; switch it in parallel to the neighbor that is closest in voltage.
   b) If no independent active modules are found, search for blocks of parallel modules that act as a series unit; the block with the highest voltage is merged into a bigger parallel unit with the neighboring block that is closest in voltage.
   c) If there are no appropriate active neighbors for a parallel block, the module is switched to bypass mode.
2) If energy is flowing out of the modules.
   a) Follow the same rules as for energy inflow, but pick the modules or parallel module blocks with the lowest module voltage for the parallelization process.

Case B: The absolute voltage has to be increased by one module step.

3) If all modules in the phase module are in bypass mode, i.e., the current voltage of the converter arm is zero, all modules are connected to one parallel unit that is switched in series at its ends.
4) If energy is flowing into the modules, the module with the lowest SOC is identified among all bypassed and passive modules.
   a) In case it is a bypassed module, it is set to the series state.
   b) In case it is a parallel unit, the unit is separated into two series units as close to its middle as possible.
5) If energy is flowing out of the modules, follow the same rules as for energy inflow, but with the module or module unit with the highest SOC.

Case C: The voltage does not change.

Since intervals with equal voltage are expected to be negligibly short for applications where at least one ac terminal is involved, the module states from the last switching cycle can be kept without the risk of a loss of balance.

This procedure is performed in software at the beginning of every switching period as often as required to reach the specified converter-arm voltage and the required module state list. The final state list is then submitted to the modules and subsequently commanded to the switches for this switching period.

Above outlined set of rules avoids the bypass state, and aims at keeping modules in parallel for as long as possible. In addition, single modules are usually given a higher priority for changing their state than units of parallel modules. For example, the method first looks for an appropriate single series module that can be parallelized with a neighbor and only applies the same to

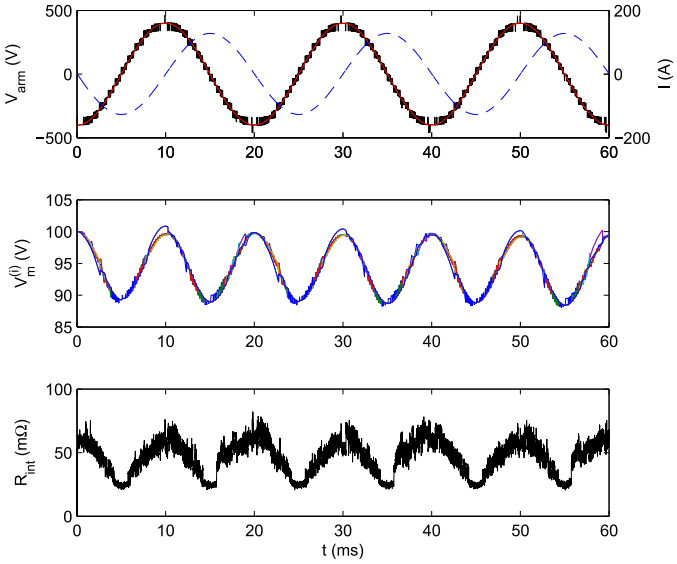


Fig. 5. Simulation results for an FET-based M2SPC converter arm as defined in Fig. 3(a) with eight modules, generating 25.7 kvar reactive power. The voltage was specified as a harmonic 400 V, 50 Hz phase (red line, top panel), which the delta–sigma modulator translated into the switching pattern $V_{\rm arm}$ and current I. The balancing scheme keeps the module voltages $V_{\rm m}^{(i)}$ within a narrow band. The bottom panel shows how the overall internal resistance $R_{\rm int}$ changes, with lowest values during low-voltage phases, when the majority of modules are in parallel. The simulated converter parameters are: MOSFET switches: $r_{\rm ds,on} = 3\ {\rm m}\Omega$, $t_{\rm on} = t_{\rm off} = 100$ ns, $C_{\rm gd} + C_{\rm ds} = 200$ pF; module capacitor: $C_m = 10$ mF, $R_{\rm esr} = 15\ {\rm m}\Omega$; delta–sigma switching rate: 25 kHz; and balancing with the method described in Section III.

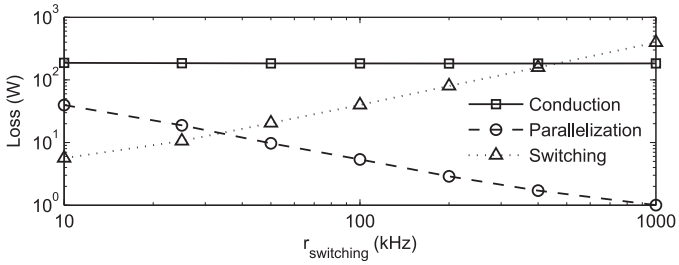


Fig. 6. Simulated losses of the converter arm of Fig. 5 in dependence of the switching rate. Within typical switching rate ranges the conduction losses are dominant, while switching losses take over when approaching the MHz range. Parallelization losses, however, never play a significant role. They fall with increasing switching rate, confirming the theoretical derivation in Section III-A.

parallel units if it does not find a single candidate. The motivation for this approach is that the slower charge/discharge rate of parallel units due to their higher effective capacitance assures that they get out of balance slower.

IV. Simulation Results and Performance Analysis

We simulated the scheduler for balancing the module SOCs as described in Section III together with a circuit model of an M2SPC converter arm with eight modules. The switches are in FET technology (channel resistance $r_{\rm ds,on} = 3\ {\rm m}\Omega$, switching time $t_{\rm on} = t_{\rm off} = 100$ ns, parasitic output capacitance $C_{\rm gd} + C_{\rm ds} = 200$ pF). Per module, we use a capacitance of 10 mF in electrolytic capacitors (equivalent series resistance $R_{\rm esr} = 15\ {\rm m}\Omega$). Pulse-width modulation is performed only on the order of one step size. Therefore, a delta–sigma modulator processes only the remainder of the reference voltage command divided by the module voltage. The scheduler distributes the switching operations among all modules.

Fig. 5 shows the results for the case of reactive power generation (400 V, 50 Hz, 25.7 kvar). The overall switching rate of the delta–sigma modulator is selected as 25 kHz. The module SOCs, as represented by their voltages $V_{\rm m}^{(i)}$, vary but stay close to each other in a balanced condition, although the modules release about a quarter of their energy. As a result of the parallel mode, which is particularly used during the lower and intermediate voltage intervals, the total internal resistance of the arm falls notably during these intervals. The same system run with a traditional scheduler [51], i.e., as an M2C, had on average an by 29% higher internal resistance.

The price for the low internal resistance is potentially higher losses associated with the parallelization of modules with unequal voltages. Fig. 6 shows an analysis of the conduction, switching, and parallelization loss contributions in the simulation model with respect to the switching rate. The parallelization losses are negligible throughout the simulated range down to relatively low overall switching rates around 10 kHz, which imply an average switching rate per module of less than 1.2 kHz. Such switching rates are suitable for IGBT multilevel systems as well [67]. The parallelization losses for the implemented balancing method decrease proportionally to $r_{\rm switching}^{-0.98}$, which is smaller than the theoretical optimum of an exponent of -2 and could indicate further potential for improvements.

In Fig. 6, the switching losses increase proportionally to the switching rate, as expected. When approaching the MHz range, switching becomes the dominant loss mechanism. Their magnitude is dominated by saturation losses during switching transitions due to the moderate turn-on and turn-off times in the simulations which deliberately avoided higher performance characteristics for this initial evaluation. Accordingly, there is the option for faster switching transitions, which will notably reduce their loss contribution.

V. Extensions

A. Simple Control

The SOC balancing method described in Section III-B is relatively complex and requires measurement data from the modules. The high complexity required for balancing is also an important issue for the traditional M2C. For many applications in the medium- and low-power range, this complexity may be too costly. In that context, it is noteworthy that the control of M2SPC allows simpler balancing approaches. Both the control algorithm and the hardware benefit from this simplification.

While the traditional M2C has to monitor the energy inflow and outflow of the modules to ensure the dynamical balance, the M2SPC has additional means based on parallelization that can clear voltage differences of modules. Therefore, M2SPC

module balancing can be performed by an open-loop control.[1] On the hardware side, this simplification obviates the elaborate module monitoring means, which have to be relatively fast and accurate in the traditional M2C. Especially for small multilevel converters, e.g., FET-based systems, the cost of the sensing elements in every module and the data traffic that has to be processed by the controller is substantial.

Balanced operation can be ensured if every module is parallelized to its neighbors on a regular basis, i.e., every interconnection between two modules is periodically in a parallel state. For highest efficiency, the duration between two parallelization procedures should be kept as small as possible; the maximum is given by the time τ in which the maximum expected current $I_{\max}$ could charge or discharge the module capacitors C_m to the limits of the specified tolerance range $V_m \pm V_{\mathrm{tol}}$ around the balanced module voltage V_m

$$\tau \leq \frac{C_{\mathrm{m}} V_{\mathrm{tol}}}{I_{\max}}. \tag{5}$$

Condition (5) can be met without difficulty, because every voltage level can be generated by a number of alternative module configurations, with different modules in parallel in each configuration, and pulse-width modulation provides frequent state transitions.

To achieve condition (5) practically, the controller can cycle through a list of predefined states that contains states with every intermodule connection being parallel at least once. More elegantly, the controller can maintain a list with the time of the last parallel state for every intermodule connection and pick for the next step the module configuration that switches those modules with the longest time into parallel operation. If the time-out τ [see (5)] for an intermodule connection is reached without having parallelized it automatically, a parallelization becomes compulsory, even if the reference voltage condition cannot be satisfied any more.

With this strategy, a converter can be balanced in an open-loop system without the risk that the converter becomes unstable or crashes. As with the closed-loop balancing strategy, the losses can be reduced to an insignificant level with appropriate switching rates. A simple and inexpensive control may be a pivotal aspect for the economic feasibility of small multilevel systems.

B. Advanced Control

The balancing and control schemes described earlier are practicable and may perform well, but leave space for improvements and cannot claim being optimal. There are two main starting points for improvements. First, the rules presented earlier could be called "ad hoc" since they do not systematically control the available degrees of freedom to improve the performance, as is also the case for the most common rules for the traditional M2C. For M2C, this led, for instance, to approaches that systematically optimize features such as circulating currents during operation [69], [70]. Second, the three key objectives of the converter control system—1) accurate voltage output; 2) efficient module balancing; and 3) low losses—are handled separately although in reality they are strongly interrelated. In the aforementioned approaches, the accurate generation of the specified voltage output is given the highest priority. The specified voltage over time, which is a product of the modulation scheme and includes also spectral properties and harmonic content of the voltage, is a fixed constraint for the balancer and does not allow modifications. While balancing has the second-highest priority, the losses are usually not controlled directly but are rather a consequence of parameters such as the pulse-width modulation timing.

While these considerations apply to the traditional M2C as well, the additional states of the M2SPC render it obvious that the decision how to arrange the modules in the next step actively controls all three objectives. For example, due to the parallel mode in M2SPC there are alternatives which lead to the same output voltage, but some alternatives using the parallel mode can either reduce the losses because of a lower internal resistance, or increase the losses because of high voltage differences between the modules. The three objectives can accordingly be controlled over a wide range, and all three can be in conflict which each other.

The following strategy, outlined briefly, addresses both by introducing more systematic rules and by uniting all parts of a control system to allow a coordination of the three objectives. First, it aims to improve all three objectives more systematically by predicting the different switching alternatives' impact on the objectives instead of using ad hoc rules. Second, it aims to enable more flexibility concerning the priorities of the three objectives.

The optimization for a switching period is performed at the beginning of that period. This approach is inspired by, but not limited to, delta–sigma modulation and reduces complexity since it has to predict only one step ahead.

The first control objective is that the actual voltage of a converter arm $V_{\mathrm{act}}(t)$ should follow the specified reference $V_{\mathrm{ref}}(t)$. The translation is traditionally the task of a separate modulator. For a concurrent optimization, however, the modulator can no longer make fixed decisions, but should assign quantitative ratings to all options given by all switching alternatives of the modules $\mathbf{s}_i$ for the next switching period i. For a simple staircase approximation, Objective 1 can be written as

$$\min_{s_i} \left| \frac{V_{\mathrm{act}}^{(s_i)}}{V_{\mathrm{ref}}} - 1 \right| \tag{6}$$

while we will prefer a delta–sigma-inspired modulation according to

$$\min_{s_i} \left| \int_{-\infty}^{t_i} V_{\mathrm{act}}(s_i, t) - \mathbf{V}_{\mathrm{ref}}(\boldsymbol{t})\, \mathrm{d}t \right|. \tag{7}$$

For the second objective, the total losses $E_{\mathrm{loss,total}}$ of the modules in the converter arm have to be split into their components, i.e., conduction losses $E_{\mathrm{loss,cond}}$, switching losses

[1] Open-loop strategies for traditional M2C modules, which use predefined switching patterns and switch roles between two power-line half-cycles [62] do not support quickly changing load and should still be monitored because small biases can lead to discharging or overcharging of some modules over time. Commercial M2C systems, therefore, implement a relatively fast sampling of the module voltage around 10 kHz [68].

$E_{\mathrm{loss,switch}}$, and parallelization losses $E_{\mathrm{loss,parall}}$

$$\min_{s_i} E_{\mathrm{loss,\,total}} = \min_{s_i} \left(E_{\mathrm{loss,\,cond}} + E_{\mathrm{loss,\,switch}} + E_{\mathrm{loss,\,parall}}\right). \quad (8)$$

These terms can be expanded [71]

$$E_{\mathrm{loss,\,cond}} = \underbrace{R_{\mathrm{int,\,tot}}(s_i) I^2 \Delta t}_{\text{internal resistance}} + \underbrace{\sum_j V_{\mathrm{ce}}\left(I^{(j)}\right) I^{(j)}}_{\text{forward-voltage drop}}$$

$$E_{\mathrm{loss,\,switch}} = \sum_{j \in \Delta s_i} \underbrace{\frac{1}{2} I^{(j)} V_{\mathrm{m}}^{(j)} \left(t_{\mathrm{on}} + t_{\mathrm{off}}\right)}_{\text{saturation losses}} + \underbrace{\frac{1}{2}\left(C_{\mathrm{gd}} + C_{\mathrm{ds}}\right)\left(V_{\mathrm{m}}^{(j)}\right)^2}_{\text{junction-capacitances}}$$

$$E_{\mathrm{loss,\,parall}} = \frac{1}{2} \sum_{\kappa \in P_{s_i}} \left(\sum C_{\mathrm{m}} \left(V_{\mathrm{m}}^{(k)}\right)^2 - \frac{\left(\sum C_{\mathrm{m}} \left(V_{\mathrm{m}}^{(k)}\right)^2\right)^2}{\sum C_k} \right) \quad (9)$$

where $R_{\mathrm{int,tot}}$ denotes the resistance in dependence of the module switching state $\mathbf{s}_i$, I is the total current, $V_{\mathrm{ce}}(I^{(j)})$ is the forward voltage of the jth semiconductor switch, which depends on the respective current $I^{(j)}$, $V_{\mathrm{m}}^{(k)}$ denotes the module voltage of module k, t_{on} and t_{off} are, respectively, the turn-on and turn-off times of the switches, C_{gd} and C_{ds} are the gate–drain and drain–source capacitances, and C_m is the module capacitance.

Balancing is the third objective and has the purpose to avoid modules from being overcharged until components are damaged or drained until the module power supply, which is usually fed by the module capacitor, collapses. In contrast to the traditional M2C, the M2SPC can be easily balanced at all times with the parallel state if it risks exceeding the voltage tolerance range. However, this process may be associated with losses. Since imbalance can be expressed in the form of costs, Objective 3 can be incorporated into Objective 2 by adding the expected losses for the case that all modules would be parallelized at the end of the next switching cycle i

$$\min_{s_i} E_{\mathrm{loss,\,total}} + \underbrace{\frac{1}{2} \sum_{q=1}^{n} \left(\sum C_{\mathrm{m}}^{(q)} \left(V_{\mathrm{m}}^{(q)}\right)^2 - \frac{\left(\sum_{r=1}^{n} C_{\mathrm{m}}^{(r)} \left(V_{\mathrm{m}}^{(r)}\right)^2\right)^2}{\sum_{r=1}^{n} C_{\mathrm{m}}^{(r)}} \right)}_{E_{\mathrm{forced\ balance}}}. \quad (10)$$

This penalty term impedes the modules' SOCs from drifting apart. In addition, a rule is required that enforces a short parallelization in case a module voltage leaves a predefined range.

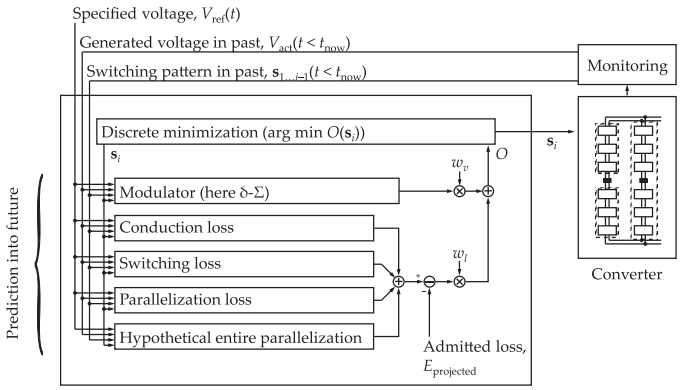


Fig. 7. Block diagram illustrating an advanced control scheme that optimizes the output voltage (performed by the modulator unit), losses, and balancing of the modules. The control output is a switching vector, s_i, that describes the module states. The depicted optimization is performed at the beginning of every time step, i, of the controller to determine the states the converter will use during that time step. A delta–sigma-type (δ-Σ) modulation scheme fits naturally into such an optimization framework because it assigns a numeric rating to any possible control alternative, allowing tradeoffs with other objectives in a numeric optimization. The modulation can, in principle, be performed by other schemes as well. The hypothetical forced parallelization of the entire arm at the end of the prediction period enforces balancing by accounting for the losses associated by an imbalanced state.

The integration of balancing into the losses reduces the number of objectives to two. While the two modified objectives from (7) and (10) could undergo a Pareto-front extraction first, we combine them as a traditional weighted sum in a single objective

$$\min_{s_i} \left(w_l \left(E_{\mathrm{loss,\,total}} + E_{\mathrm{forced\ balance}} - E_{\mathrm{projected}}\right) + w_v \left| \int_{-\infty}^{ti} V_{\mathrm{act}}^{s_i}(t) - V_{\mathrm{spec}} dt \right| \right). \quad (11)$$

The weights w_l and w_v match the different orders of losses and the integrated voltage deviation. They can be assigned based on expected development of both terms. For example, the maximum tolerable voltage error may be one module step so that the growth of the integral is $\leq V_m t$. The losses, on the other hand, were estimated as the conduction loss plus an additional margin for switching. $E_{\mathrm{projected}}$ specifies the tolerated losses. For our example, it was set to an average expected resistive loss with a predefined expected equivalent resistance R_{exp} according to $E_{\mathrm{projected}} \equiv R_{\mathrm{exp}}\, I^2 t$. Accordingly, at the beginning of every switching cycle, the combined objective in (11) is predicted for the end of that switching cycle for all possible configurations of the converter arm, represented by the module switching states $\mathbf{s}_i$. The configuration with the smallest value of the objective function is then assigned to the system. The block diagram in Fig. 7 gives an overview of the optimization, which is performed for every time step when the controller reconsiders the module states.

It should be noted that the actual switching rate of the modules is no longer a fixed predetermined parameter, but is dynamically adapted to coordinate switching losses exceeding the projected amount and voltage accuracy.

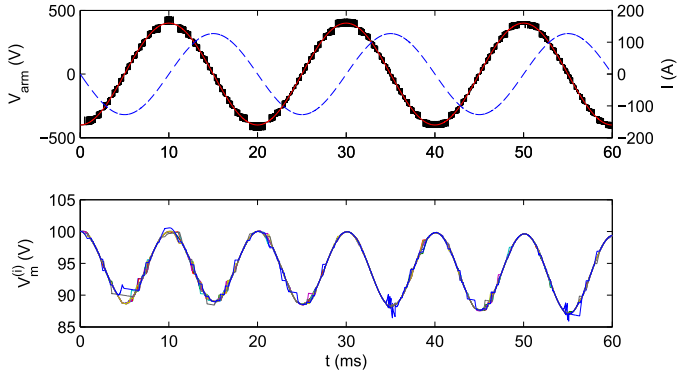


Fig. 8. Simulation of the advanced M2SPC control scheme based on loss minimization outlined in Section V-B and Fig. 7. Variable definitions and simulation conditions are the same as in Fig. 5.

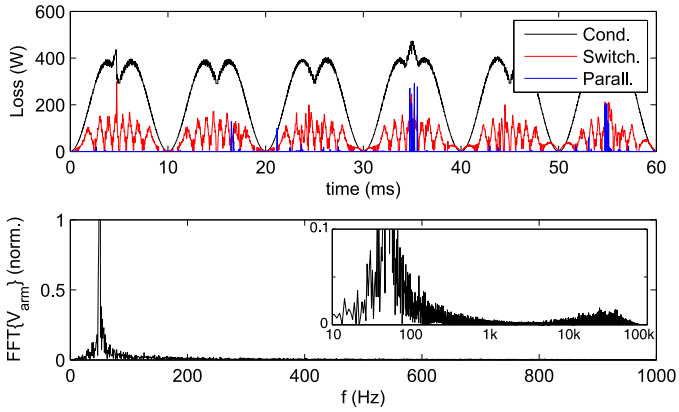


Fig. 9. Losses over time (conduction, switching, and parallelization losses) and spectrum of the arm voltage corresponding to the simulation in Fig. 8. The optimization aims at minimizing the loss and the voltage output locally, i.e., within the short minimum switching time step, balancing between the different cost-function contributions. The inset in the lower plot displays the spectrum with logarithmic frequency and magnified amplitude axis.

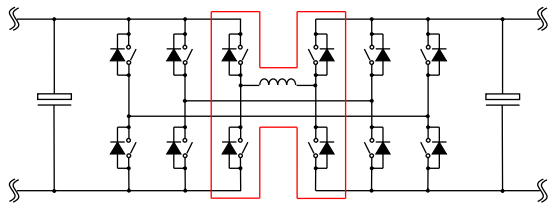


Fig. 10. Further module extension. When the strict two-pole limitation in the modular multilevel converter is given up, several new features can be incorporated into the modules. As shown an additional connection with an inductance, as a counterpart to the module capacitors, can form with the switches and diodes either a dc-dc converter, which can have a relatively low power rating for transferring energy between modules, or a controllable filter.

Finding the configuration of the converter arm given by the state of every module that minimizes the total objective in (11) and Fig. 7 is not a continuous but a finite discrete optimization problem. Particularly, because it cannot be extended or interpolated easily to an equivalent continuous problem that would show advantageous properties for optimization, many recent optimization methods that apply heuristic approaches to use trends of the objective function are not appropriate. We implemented an exhaustive search within all candidates that fulfilled the condition that the output would deviate from the previous one by no more than two module-voltage steps (2×100 V).

Fig. 8 shows an example simulation of a converter arm with eight modules controlled with the described energy-minimization method. The losses were controlled to 246 W, on average, which led to an average switching rate of 47.5 kHz. Worth noting is that this approach tolerates more fluctuations of the individual module SOCs than the example in Section IV. Apparently, in some cases, minor SOC imbalances may be favorable and either avoid additional, e.g., switching, losses or allow a higher voltage accuracy, at least on the time frame of one switching cycle. Stronger imbalances, however, are inhibited due to the squared influence of the voltage difference in the penalty term, which accounts for the expected losses of an unbalanced system. The instantaneous losses over time are plotted in Fig. 9. The conduction losses dominate most of the time due to the relatively low switching rates per semiconductor. Both the conduction losses and the trend of the switching losses reflect the current waveforms. However, the changing internal resistance leads to deviations from a squared sine in the former. The spectrum of the voltage (see Fig. 9, bottom) contains no distinct peaks besides the sharp fundamental mode at the output frequency of 50 Hz. Because a fixed switching rate does not exist and the resultant switching arises from a balance of losses and accuracy, the spectral power at the average switching rate of 47.5 kHz is close to the noise floor (see inset of Fig. 9, bottom).

Presently, this control approach is associated with significant computational effort. However, the optimization in every step could be sped up notably, since only a few module configurations may be reasonable for the next cycle based on the current system state. In addition, adaptive control may eliminate calibration parameters.

This presentation gives only a short outline and an informal proof that this integrated, energy-minimization control method can be operated stably. Further research could develop this method as an advantageous alternative to conventional approaches that treat the various converter control objectives separately.

An example for advancing such approaches may be a more wide-reaching optimization. While the presented procedure optimized only with respect to the momentary clock interval, a better approach may incorporate a number of steps ahead to find optima that require a sacrifice in the objective in the momentary step to increase the performance in a subsequent step. An example is preponing a switching action when the current increases despite the additional loss and the increasing modulator's objective to avoid higher losses for the same switching action a few steps later. Such a tree-based analysis of the upcoming switching steps may well remind of the strategy of chess computers [72], [73].

C. Topology Generalization

The essential step to achieving the parallel states in the M2SPC module is adding more half-bridge taps to the module capacitor. This approach can be extended beyond four-pole modules. Fig. 10 shows that a third terminal on each side of the

module can enable additional functionality. With an inductance in the third line between two modules, the modules obtain a step-up/step-down dc–dc converter, which is formed together with the active switches and the diodes. This dc–dc converter can transfer energy between the modules efficiently even for nonnegligible voltage differences. Since the energy transfer can be performed from a module with a lower voltage to one with a higher voltage, this approach allows very flexible charge transfer along a converter arm.

Depending on the application, the power rating of the components in this extended topology can be relatively low. If the dc–dc converter is given a leading role, novel macrotopologies become possible, especially for applications where energy has to be converted between terminals with significantly different voltages.

Furthermore, the inductance can be used as a controllable filter and replace dedicated fixed inductances in typical high-voltage multilevel converter arms to achieve higher stability. Such inductances can prohibit surge currents and oscillations between the phase modules of the converter due to switching and can filter the network connections. Especially for HVDC networks, permanent inductances can be a critical issue in case of a short circuit on the dc side. The distributed inductance in a third intermodule line, in contrast, can be controlled and successively removed from the line and discharged into the surrounding modules.

VI. Conclusion

While existing M2C topologies use only two-pole module structures, modules can more generally be n-pole, offering additional features. Essential for the low-voltage condition within the modules is that interconnections are only established with immediate neighbors, or potentially their neighbors. With every step the interconnection is reaching further away from the immediate neighbor, the maximum voltage to be expected for the semiconductors in at least some module states increases by one module voltage level.

We introduced the M2SPC topology that uses four-pole modules, extending the two-pole M2C module structure. Two additional half-bridge terminals in the M2SPC module enable a parallel mode in addition to the traditional M2C series and bypass states. Most importantly, the modules that are inactive in the bypass state in the traditional M2C when they are not required in series for a higher voltage can be used actively in parallel in M2SPC. Further, the introduction of parallel-mode capability is not accompanied by additional power semiconductor cost, since all traditional M2C series states are handled by two devices in parallel, resulting in the same overall amount of silicon.

The parallel mode serves two purposes. First, it increases the current rating by reducing the internal resistance. This improvement is particularly important for low- and medium-voltage converters based on FETs [36], [38], where the internal resistance of the capacitors often dominates the losses. Second, the parallel mode provides an additional method for balancing the SOCs of the individual modules. Because balancing in the parallel mode does not require accurate information of the energy inflow and outflow in every module, it can ensure a balanced state even with an open-loop approach, simplifying module SOC monitoring. The losses associated with parallelization can be made negligibly small, if the time intervals between parallelization are kept short.

While applications where highest currents occur during low voltage levels, such as in STATCOMs, would benefit obviously from parallelization, the low maximum module usage (less than 64% as given in Section I-B for ac conversion with the traditional M2C topology) shows that there is also a big potential for standard conversion applications. The exact gain associated with the parallel mode depends on both the specific implementation and the application.

M2Cs could provide an advantageous framework for handling battery packs, with applications, for example, in energy storage and electric vehicle drives. Specifically, the M2SPC topology can provide the structure for a dynamical reconfiguration of battery cells in series and in parallel. In this approach, a battery cell or combination of cells would replace the capacitors in the microtopologies in Figs. 1, 2, and 10. Due to the relatively high internal resistance of batteries—for Li-ion cells, for instance, on the order of 200 mΩ/Ah [74]—and their limited dynamics, the parallel mode is a central feature to distribute the load among the cells and to temporally even it out within each cell, essentially maximizing efficiency. Thus, the same system can perform battery cell balancing, charge control, and power conversion.

For controlling M2Cs, which allow multiple module configurations producing the same voltage output, the switching modulator and the balancing routine can be combined to coordinate the three important performance objectives, i.e., voltage accuracy, losses, and SOC balancing.

Finally, the strategy leading from a two-pole to a four-pole microtopology by adding another terminal, which enables the parallel mode, can be repeated to incorporate systematically novel features into M2Cs, such as intrinsic dc–dc converters or controllable filters. Such developments could further enhance the flexibility of M2Cs and enable new application.

Acknowledgment

The authors would like to thank Prof. R. Marquardt for his support and his devoted mentoring of this paper. Parts of the technology described in this paper are subject to patents and patent applications (Goetz/Weyh) held by Technische Universitaet Muenchen.

References

[1] T. A. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters," in *Proc. IEEE 23rd Ann. Power Electron. Spec. Conf. Record.*, 1992, vol. 1, pp. 397–403.

[2] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, "VSC-based HVDC power transmission systems: An overview," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 592–602, Mar. 2009.

[3] G. Asplund, K. Eriksson, and O. Tollerz, "HVDC light, a tool for electric power transmission to distant loads," in *Proc. VI SEPOPE Conf.*, Salvador, Brazil, 1998.

[4] J. Rodriguez, L. Jih-Sheng, and P. F. Zheng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[5] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. A. M. Prats, and M. A. Perez, "Multilevel converters: An enabling

technology for high-power applications," *Proc. IEEE*, vol. 97, no. 11, pp. 1786–1817, Nov. 2009.

[6] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, W. Bin, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[7] G. M. Kristmundsson and D. P. Carroll, "The effect of AC system frequency spectrum on commutation failure in HVDC inverters," *IEEE Trans. Power Delivery*, vol. 5, no. 2, pp. 1121–1128, Apr. 1990.

[8] D. Zhang, M. Haeusler, H. Rao, C. Shang, and T. Shang, "Converter station design of the ± 800 kV UHVDC project Yunnan-Guangdong," in *Proc. 17th Conf. Electric Power Supply Ind.*, Macau, China, 2008.

[9] G. Asplund, K. Eriksson, and K. Svensson, "DC transmission based on voltage source converters," in *Proc. CIGRE SC14 Colloquium*, South Africa, 1997.

[10] T. Larsson, Å Petersson, A. Edris, D. Kidd, and F. Aboytes, "Eagle pass back-to-back tie: A dual purpose application of voltage source converter technology," in *Proc. Power Eng. Soc. Summer Meet.*, 2001, vol. 3, pp. 1686–1691.

[11] M. P. Bahrman, J. G. Johansson, and B. A. Nilsson, "Voltage source converter transmission technologies: The right fit for the application," in *Proc. IEEE Power Eng. Soc. General Meet.*, 2003, vol. 3, pp. 1840–1847.

[12] B. Jacobson, Y. Jiang-Häfner, P. Rey, G. Asplund, M. Jeroense, A. Gustafsson, and M. Bergkvist, "HVDC with voltage source converters and extruded cables for up to ± 300 kV and 1000 MW," in *Proc. CIGRÉ Session*, 2006, pp. B4–105.

[13] B. D. Railing, J. J. Miller, P. M. Steckley, G. P. Bard, L. Ronström, and J. Lindberg, "Cross sound cable project–second generation VSC technology for HVDC," in *Proc. CIGRÉ Session*, 2004, pp. B4–102.

[14] S. Allebrod, R. Hamerski, and R. Marquardt, "New transformerless, scalable modular multilevel converters for HVDC-transmission," in *Proc. IEEE Power Electron. Spec. Conf.*, 2008, pp. 174–179.

[15] H. J. Knaak, "Modular multilevel converters and HVDC/FACTS: A success story," in *Proc. 14th Eur. Conf. Power Electron. Appl.*, 2011, pp. 1–6.

[16] S. P. Teeuwsen, "Modeling the trans bay cable project as voltage-sourced converter with modular multilevel converter design," in *Proc. IEEE Power Energy Soc. General Meet.*, 2011, pp. 1–8.

[17] E. Koldby and M. Hyttinen, "Challenges on the road to an offshore HVDC grid," in *Proc. Nordic Wind Power Conf.*, Bornholm, Denmark, 2009.

[18] H. Akagi, "Classification, terminology, and application of the modular multilevel cascade converter (MMCC)," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3119–3130, Nov. 2011.

[19] B. Gultekin and M. Ermis, "Cascaded multilevel converter-based transmission STATCOM: System design methodology and development of a 12 kV ± 12 MVAr power stage," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4930–4950, Nov. 2013.

[20] R. H. Osman, "A medium-voltage drive utilizing series-cell multilevel topology for outstanding power quality," in *Proc. IEEE 34th IAS Ann. Meet. Ind. Appl. Conf. Record*, 1999, vol. 4, pp. 2662–2669.

[21] L. M. Tolbert, P. F. Zheng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 36–44, Jan./Feb. 1999.

[22] M. Calais, V. G. Agelidis, and M. Meinhardt, "Multilevel converters for single-phase grid connected photovoltaic systems: An overview," *Solar Energy*, vol. 66, pp. 325–335, 1999.

[23] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep./Oct. 2005.

[24] G. R. Walker and P. C. Sernia, "Cascaded DC–DC converter connection of photovoltaic modules," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 1130–1139, Jul. 2004.

[25] S. Busquets-Monge, J. Rocabert, P. Rodriguez, S. Alepuz, and J. Bordonau, "Multilevel diode-clamped converter for photovoltaic generators with independent voltage control of each solar array," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2713–2723, Jul. 2008.

[26] C. H. Ng, M. A. Parker, L. Ran, P. J. Tavner, J. R. Bumby, and E. Spooner, "A multilevel modular converter for a large, light weight wind turbine generator," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1062–1074, May 2008.

[27] S. M. Muyeen, R. Takahashi, T. Murata, and J. Tamura, "A variable speed wind turbine control strategy to meet wind farm grid code requirements," *IEEE Trans. Power Syst.*, vol. 25, no. 1, pp. 331–340, Feb. 2010.

[28] M. J. Duran, S. Kouro, W. Bin, E. Levi, F. Barrero, and S. Alepuz, "Six-phase PMSG wind energy conversion system based on medium-voltage multilevel converter," in *14th Eur. Conf. Proc. Power Electron. Appl.*, 2011, pp. 1–10.

[29] J. M. Carrasco, L. G. Franquelo, J. T. Bialasiewicz, E. Galvan, R. C. P. Guisado, M. A. M. Prats, J. I. Leon, and N. Moreno-Alfonso, "Power-electronic systems for the grid integration of renewable energy sources: A survey," *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1002–1016, Jun. 2006.

[30] P. Bresesti, W. L. Kling, R. L. Hendriks, and R. Vailati, "HVDC connection of offshore wind farms to the transmission system," *IEEE Trans. Energy Convers.*, vol. 22, no. 1, pp. 37–43, Mar. 2007.

[31] L. Leclere and C. Galmiche, "A transformerless full redundant electrical propulsion solution to enhance power density, availability and low noise signature," in *Proc. IEEE Electric Ship Technol. Symp.*, 2011, pp. 296–299.

[32] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel inverters for electric vehicle applications," in *Power Electron. Transp.*, 1998, pp. 79–84.

[33] S. Bhattacharya, D. Mascarella, and G. Joos, "Modular multilevel inverter: A study for automotive applications," in *Proc. IEEE 26th Ann. Can. Conf. Electr. Comput. Eng.*, 2013, pp. 1–6.

[34] F. Khoucha, S. M. Lagoun, K. Marouani, A. Kheloui, and M. E. H. Benbouzid, "Hybrid cascaded H-Bridge multilevel-inverter induction-motor-drive direct torque control for automotive applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 892–899, Mar. 2010.

[35] F. H. Khan, L. M. Tolbert, and W. E. Webb, "Hybrid electric vehicle power management solutions based on isolated and nonisolated configurations of multilevel modular capacitor-clamped converter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 3079–3095, Aug. 2009.

[36] L. Lambertz, R. Marquardt, and A. Mayer, "Modular converter systems for vehicle applications," in *Emobility – Electr. Power Train*, 2010, pp. 1–6.

[37] M. Schulz, L. Lambertz, and R. Marquardt, "Dimensioning of modular high frequency converter for drives," in *Proc. IEEE ECCE Asia Downunder*, 2013, pp. 675–680.

[38] S. M. Goetz, M. Pfaeffl, J. Huber, M. Singer, R. Marquardt, and T. Weyh, "Circuit topology and control principle for a first magnetic stimulator with fully controllable waveform," in *Proc. IEEE Ann. Int. Conf. Eng. Med. Biol. Soc.*, 2012, pp. 4700–4703.

[39] S. M. Goetz, C. N. Truong, M. G. Gerhofer, A. V. Peterchev, H.-G. Herzog, and T. Weyh, "Analysis and optimization of pulse dynamics for magnetic stimulation," *PLoS ONE*, vol. 8, e55771, 2013.

[40] M. Marchesoni, M. Mazzucchelli, and S. Tenconi, "A nonconventional power converter for plasma stabilization," *IEEE Trans. Power Electron.*, vol. 5, no. 2, pp. 212–219, Apr. 1990.

[41] R. Claesen, T. Bonicelli, R. Öström, H. McBryan, and G. Zullo, "The JET fast power supplies," European Fusion Development Program1994.

[42] S. M. Tenconi, R. Numeroli, L. Pittera, E. Rizzo, P. L. Mondino, and A. Santagiustina, "High power, wide bandwidth linear switching amplifier using IGBTs," in *Proc. IEEE Ind. Appl. Soc. Ann. Meet. Conf. Record*, 1993, vol. 2, pp. 778–784.

[43] V. Toigo, L. Zanotto, M. Bigi, E. Gaio, J. H. Hay, R. Piovan, and S. R. Shaw, "Conceptual design of the enhanced radial field amplifier for plasma vertical stabilisation in JET," *Fusion Eng. Design*, vol. 82, pp. 1599–1606, 2007.

[44] L. Encarnação, J. F. Silva, S. F. Pinto, and L. M. Redondo, "A new modular marx derived multilevel converter," in *Technological Innovation for Sustainability,* vol. 349, L. Camarinha-Matos, Ed. Berlin, Germany: Springer, 2011, pp. 573–580.

[45] L. M. Redondo, H. Canacsinh, and J. F. Silva, "Generalized solid-state marx modulator topology," *IEEE Trans. Dielectr. Electr. Insulation*, vol. 16, no. 4, pp. 1037–1042, Aug. 2009.

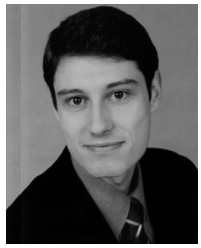
[46] M. Petkovsek, P. Zajec, J. Nastran, and D. Voncina, "Multilevel bipolar high voltage pulse source—Interlock dead time reduction," in *Proc. EUROCON Comput. Tool. IEEE Region 8*, Sep. 22–24, 2003, vol. 2, pp. 240–243.

[47] L. M. Redondo, H. Canacsinh, and J. F. Silva, "New repetitive bipolar solid-state marx type modulator," in *Proc. IEEE Int. Power Modulators High Voltage Conf.*, 2008, pp. 253–256.

[48] D. Peftitsis, G. Tolstoy, A. Antonopoulos, J. Rabkowski, J.-K. Lim, M. Bakowski, L. Ängquist, and H. P. Nee, "High-power modular multilevel converters with SiC JFETs," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 28–36, Jan. 2012.

[49] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep. 1981.

[50] P. Barbosa, P. Steimer, J. Steinke, L. Meysenc, M. Winkelnkemper, and N. Celanovic, "Active neutral-point-clamped multilevel converters," in *Proc. IEEE 36th Power Electron. Spec. Conf.*, 2005, pp. 2296–2301.
[51] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Power Tech Conf.*, vol. 3, Bologna, Italy, Jun. 23–26, 2003, p. 6.
[52] M. Glinka and R. Marquardt, "A new AC/AC multilevel converter family," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 662–669, Jun. 2005.
[53] F. H. Khan and L. M. Tolbert, "A multilevel modular capacitor-clamped DC–DC converter," *IEEE Trans. Ind. Appl.*, vol. 43, no. 6, pp. 1628–1638, Nov./Dec. 2007.
[54] R. Marquardt, "Modular multilevel converter topologies with DC-short circuit current limitation," in *Proc. IEEE 8th Int. Conf. Power Electron. ECCE Asia*, 2011, pp. 1425–1431.
[55] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modulation, losses, and semiconductor requirements of modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2633–2642, Aug. 2010.
[56] K. Ilves, F. Taffner, S. Norrga, A. Antonopoulos, L. Harnefors, and H.-P. Nee, "A submodule implementation for parallel connection of capacitors in modular multilevel converters," in *Proc. IEEE Eur. Energy Convers. Congr. Expo.*, 2013, pp. 1–10.
[57] M. Glinka and R. Marquardt, "A new AC/AC-multilevel converter family applied to a single-phase converter," in *Proc. Fifth Int. Conf. Power Electron. Drive Syst.*, Nov. 17–20, 2003, vol. 1, pp. 16–23.
[58] C. Fahrni, A. Rufer, F. Bordry, and J. Burnet, "A novel 60 MW pulsed power system based on capacitive energy storage for particle accelerators," in *Proc. Eur. Conf. Power Electron. Appl.*, 2007, pp. 1–10.
[59] D. E. Hage, Y. Birbaum, and A. Rufer, "A high current pulse-power supply for flash lamps in PV-Panel measurement-facilities," in *Proc. Int. Conf. Power Electron., Intell. Motion Power Quality 2010, PCIM*, Nuremberg, Germany, 2010, pp. 81–87.
[60] K. Ilves, A. Antonopoulos, S. Norrga, and H. P. Nee, "A new modulation method for the modular multilevel converter allowing fundamental switching frequency," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3482–3494, Aug. 2012.
[61] D. Hong, S. Bai, and S. M. Lukic, "Closed form expressions for minimizing total harmonic distortion in 3-phase multilevel converters," *IEEE Trans. Power Electron.*, 2013. doi: 10.1109/TPEL.2013.2290377.
[62] L. M. Tolbert and T. G. Habetler, "Novel multilevel inverter carrier-based PWM method," *IEEE Trans. Ind. Appl.*, vol. 35, no. 5, pp. 1098–1107, Sep./Oct. 1999.
[63] L. Li, D. Czarkowski, L. Yaguang, and P. Pillay, "Multilevel selective harmonic elimination PWM technique in series-connected voltage inverters," *IEEE Trans. Ind. Appl.*, vol. 36, no. 1, pp. 160–170, Jan./Feb. 2000.
[64] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 858–867, Aug. 2002.
[65] M. Guan and Z. Xu, "Modeling and control of a modular multilevel converter-based HVDC system under unbalanced grid conditions," *IEEE Trans. Power Electron.*, vol. 27, no. 12, pp. 4858–4867, Dec. 2012.
[66] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Trans. Power Delivery*, vol. 26, no. 3, pp. 2009–2017, Jul. 2011.
[67] M. Glinka, "Prototype of multiphase modular-multilevel-converter with 2 MW power rating and 17-level-output-voltage," in *Proc. IEEE 35th Ann. Power Electron. Spec. Conf.*, 2004, pp. 2572–2576.
[68] B. Gemmell, J. Dorn, D. Retzmann, and D. Soerangr, "Prospects of multilevel VSC technologies for power transmission," in *Proc. IEEE/PES Transmission Distrib. Conf. Expo.*, 2008, pp. 1–16.
[69] J. Qin and M. Saeedifard, "Predictive control of a modular multilevel converter for a back-to-back HVDC system," *IEEE Trans. Power Delivery*, vol. 27, no. 3, pp. 1538–1547, Jul. 2012.
[70] M. A. Perez, J. Rodriguez, E. J. Fuentes, and F. Kammerer, "Predictive control of AC–AC modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 7, pp. 2832–2839, Jul. 2012.
[71] X. Yali, S. Shan, J. Hongwei, P. Shea, and Z. J. Shen, "New physical insights on power MOSFET switching losses," *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 525–531, Feb. 2009.
[72] S. L. Epstein, "Game playing: The next moves," in *Proc. 16th Nat. Conf. Artif. Intell.*, 1999, vol. 1, pp. 987–993.
[73] M. Campbell, A. J. Hoane, Jr., and F.-H. Hsu, "Deep blue," *Artif. Intell.*, vol. 134, pp. 57–83, 2002.
[74] D. Zhang, B. S. Haran, A. Durairajan, R. E. White, Y. Podrazhansky, and B. N. Popov, "Studies on capacity fade of lithium-ion batteries," *J. Power Sources*, vol. 91, pp. 122–129, 2000.



Stefan M. Goetz received his undergraduate and graduate degrees from TU Muenchen, Germany. He obtained his doctoral training at TU Muenchen as well as Columbia University, and received the Ph.D. degree in 2012 with a thesis on medical applications of power electronics, for which he was awarded a Ph.D. thesis prize from TU Muenchen.

He worked for océ Printing Systems and the Fraunhofer Society. He is currently a Research Associate at Duke University. His research interests include precise high-power pulse synthesizers for magnetic neurostimulation and noninvasive brain stimulation as well as integrative power electronics solutions for microgrids and electric vehicle applications.

Angel V. Peterchev received the A.B. degree in physics and engineering sciences from Harvard University, Cambridge, MA, USA, in 1999, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley, USA, in 2002 and 2005, respectively.

He is currently an Assistant Professor in the Departments of Psychiatry and Behavioral Sciences, Electrical and Computer Engineering, and Biomedical Engineering at Duke University. Previously, he was an Assistant Professor at Columbia University and spent a summer working at the Portable Power Systems Group, National Semiconductor Corp. (now Texas Instruments). His research interests include the design, modeling, and optimization of systems for noninvasive brain stimulation and for electrical energy conversion. In the field of brain stimulation, he has contributed to novel devices for transcranial magnetic stimulation with controllable pulse parameters, models and analysis of the electric field induced by transcranial magnetic and electric stimulation, and in vivo studies exploring the relationship between stimulation parameters and physiological response. In the field of energy, he has contributed to the development of control systems and topologies for fast, efficient power converters including applications to microprocessor power supplies, portable electronics, integrated magnetics, and modular multilevel converters. He has authored some 40 peer-reviewed publications that have been cited more than 700 times.

Thomas Weyh received the Diploma degree in physics in 1989, and the Ph.D. degree in electrical engineering from TU Muenchen, Germany, in 1995.

He developed his research profile in power electronics for medical and drive applications for his Habilitation (2003). He served as a Consultant in various industrial positions for medical and energy solutions. Furthermore, he has successfully commercialized his research with a start-up company. Currently, he is a Professor of electrical engineering and the Chair of power distribution at the Universitaet der Bundeswehr Muenchen. He is an expert for the generation of pulsed power and electromagnetic fields. In addition to traditional power engineering, he also contributed to leading research on nanomagnetic carriers for guiding drug molecules as well as *in-vivo* transfection controlled by magnetic fields and electromechanical actuators that function as motors, as highly accurate angle, and as torque transducers. His special focus in power application is dc power transmission.