Isolated DC/DC Structure Based on Modular Multilevel Converter

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***Abstract*—In the future, new aspects from decentralized generation using different dc voltage levels are expected to influence the general concept of power exchange. Converter are needed to adapt the voltage between low voltage (LV), medium voltage (MV), and high voltage (HV). In this paper, a galvanic isolated bidirectional dc/dc converter based on the modular multilevel converter is studied, with a large potential for secure and flexible dc power flow control. The use of medium frequency transformation allows savings in copper and iron. A fundamental frequency modulation method is introduced for the presented converter, that enables variable stepup or step-down between primary and secondary dc voltage in discrete steps. The balancing mechanism of the internal power storage components is explained and verified by simulation and experiment.**

***Index Terms*—DC/DC converter, dc power systems, modular multilevel converter, M2C, power electronics.**

I. Introduction

THE crucial elements to any distribution system, ac or dc, are the voltage transformation devices. In an ac system, transformers can easily adapt the voltage to higher levels for energy transportation or reduce it to meet the load requirements. Besides that it provides galvanic isolation. It was the transformer that decided the historic "battle of currents" [1], which made ac the preferred technology for transmission and distribution until today. Since the introduction of the semiconductor technology in the 1970, dc systems have become again an attractive alternative to ac systems for some applications [2]. The initial cost of an HVDC system is still high in comparison to an equivalent ac system; Fig. 1 shows that dc only becomes economically interesting for transmission of power over larger distance [3].

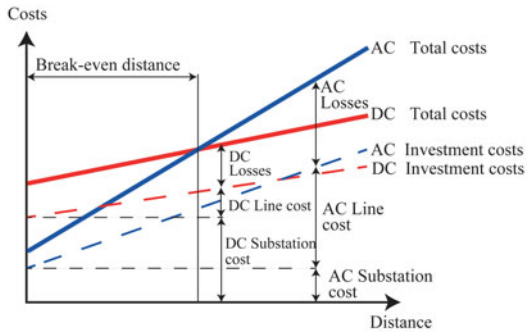

Fig. 1. Proportional break-even distance of HVDC versus HVAC [3].

In general, the break even distance depends on various aspects, such as right of way (the required corridor around a power line is almost half for HVDC systems with respect to HVAC systems), the transmission medium (cable or overhead lines), the type of substation (HVAC, thyristor-based HVDC, VSC-HVDC), and environmental aspects (generally in disfavor of ac systems). For a thyristor HVDC system, the break even distance using overhead lines is of around 500 to 800 km [4]. For cabled systems (underground or in the sea), the break even distance is much shorter, generally between 40 and 80 km [5], [6]. For shorter distances, the total losses for HVDC are more important than for HVAC systems, since the efficiency of the HVDC converter cannot match the efficiency of the transformer in an ac system. On the other side, line losses are smaller for HVDC [7]. To a certain extent, this consideration is not only valid for HVDC systems but can also be applied for distribution systems at MVDC level.

In an ac system, the high-, medium- and low-voltage networks are interfaced by the mean of multiple low-frequency transformers. In a dc system, galvanically isolated voltage conversion requires use of both transformers and power electronics, or an equivalent structure often termed as dc transformer [8]–[11]. The efficiency of conventional distribution transformer is generally higher than 98% [12], [13]. To be competitive, the efficiency of a dc transformer should be at least the same, or preferably better in order to stimulate investments into the new technology.

Another decisive element of a distribution and transmission network is the protection. AC circuit breakers are available for all power levels, whereas dc circuit breakers are not yet easily available for high powers. New dc/dc topologies lead to a more secure power transport and even can have inherent protection [14]–[19].

This paper is dedicated to an isolated bidirectional dc/dc converter, that takes the role of a tap changer for dc grids. Discrete voltage steps can be produced by changing the depth of

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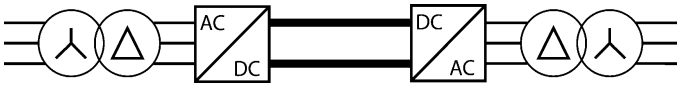

Fig. 2. Point to point connection of an HVDC line based on MMC.

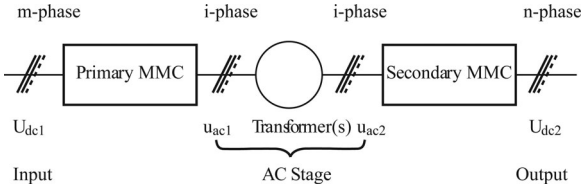

Fig. 3. General concept of the proposed topology.

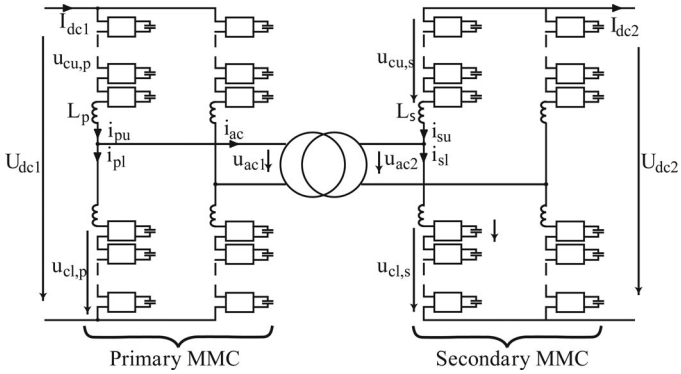

Fig. 4. Single-phase converter with single phase ac stage.

modulation. The converter is also able to interrupt power flow without using a circuit breaker [19] and presents therefore a secure solution for the dc grid. The paper is organized as follows. Section II describes the proposed dc/dc converter topology which is based on a modular multilevel structure. Section III explains a novel modulation method based on a two-level modulation, that achieves high voltage elevation factors that are variable at the same time. Section IV explains the energy balancing mechanism at the level of the submodules and the branches. Section V shows simulation results and Section VI the experimental results. Section VII summarizes the main findings.

II. DC/DC Converter Based on Modular Multilevel Converter

The modular multilevel converter (MMC) [20] is normally used as an interface between the ac grid and an HVDC line, often in a setup where two MMCs are connected at their dc terminal over an HVDC transmission line [21], [22], as illustrated in Fig. 2. The galvanic isolation is achieved on the ac grid side, with bulky transformers at 50 or 60 Hz. The modular construction of the MMC makes it possible to scale up to high voltage levels, while assuring a uniform stress on the semiconductors devices. The MMC is a highly efficient converter with efficiencies up to 99.5% [23]–[26] for high powers.

Lately multiterminal dc grids using MMC have been proposed [27]–[29]; however, even in this configuration the MMC is still mainly used to interface a low-frequency ac source (50 or 60 Hz) with a dc line. Several different configurations of the MMC have been proposed: a single-phase ac to single-phase ac converter [30], a multiphase matrix converter [31], [32] or even nonisolated dc/dc converter [14], [33]–[35].

A front-to-front configuration is presented in [31], using a transformer between two MMCs for galvanic isolation. AC respectively dc output can be achieved, if unipolar respectively bipolar submodules are used, shown in Fig. 7. This topology is limited to single-phase applications because a center-tapped transformer is used.

A generalization of this concept is presented in Fig. 3. The bidirectional converter consists of two MMCs, called in the following primary MMC and secondary MMC. The primary and the secondary are connected to one or several transformers which are referred to as the "medium frequency ac stage." The transformer may be a single transformer with multiple phases or several transformers connected together in different configurations. Primary and secondary MMCs are built of several branches in a bridge or matrix arrangement. The number of input phases can vary from the number of output phases; however, the number of phases connected to the ac stage is the same for the primary and secondary MMC. The advantage of this structure is the possibility to use higher frequencies at the transformer. The size of passive components within the converter is proportional to the frequency; therefore, a higher operation frequency decreases the volume of transformer, capacitors, and branch inductances [19], [20], [36].

The upper limit of the ac frequency of the transformer is given by the switching frequency of the semiconductors and the associated switching losses. In addition to that, the transformer insulation requirements may limit the increase of the switching frequency. Lowest switching losses are achieved with a step modulation [37], i.e., the average switching frequency of the switches is equal to the frequency of the transformer.

This paper focuses on the particular application of a dc/dc converter, as shown in Fig. 4. Primary and secondary MMCs are built of four branches in a bridge arrangement. On the left side is the low-voltage dc terminal U_{dc1} and on the right side is the high-voltage dc terminal U_{dc2}. The voltage is elevated and inverted from U_{dc1} to u_{ac1} by the primary MMC and elevated and rectified from u_{ac2} to U_{dc2} by the secondary MMC. The elevation has an influence on the type and number of submodules. For example, a voltage elevation in the primary MMC requires full-bridge submodules, illustrated in Fig. 7. In the case where U_{dc1} and U_{dc2} are equal, the same number of half-bridge submodules can be employed.

III. Converter Modulation

With the motivation of elevating the dc voltage from the primary to the secondary dc side without necessarily using the transformer, a dual active bridge (DAB) like modulation method is applied. The magnitude of the square waves and the dc voltages at the terminals can be controlled in discrete steps. Similar to the DAB converter, the switching actions in the secondary converter are phase shifted with respect to the primary converter and several switching actions take place at the same time in the

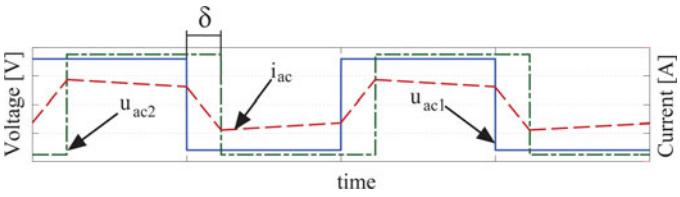

Fig. 5. Two-level modulation.

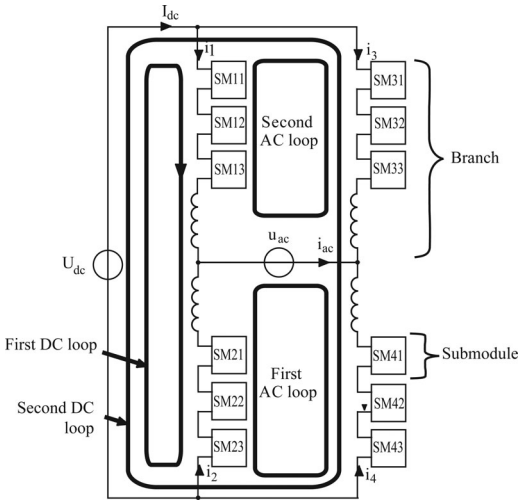

Fig. 6. Principle of voltage elevation.

primary respectively secondary converters. Typical waveforms at the transformer terminals are shown in Fig. 5.

The power flow in the converter is controlled by the phase shift δ of the ac quantities. A PI controller can be used for this purpose [19].

The modulation of the primary MMC can be distinguished from the modulation of the secondary MMC. To make an elevation possible in the primary MMC, bipolar submodules must be used. In the secondary MMC, unipolar submodules are sufficient to achieve a voltage elevation. The structure of Fig. 6 is used to explain the concept of voltage elevation and can be part of the primary or the secondary converter.

In Fig. 6, a Kirchhoff loop is called "ac-loop," when it forms a closed loop with the transformer ac voltage and two of the MMC branches. There are two parallel "ac-loops" supplying the ac voltage. The "dc-loop" on the other hand is a loop formed with the dc source and two branches. In Fig. 6, there are two different "dc-loops." Each branch is physically included in both an "ac-loop" and a "dc-loop."

The voltage elevation of the primary MMC is determined by the ratio of the number of submodules actively connected in the "ac-loops" $N_{\mathrm{ac},p}$ over the number of submodules connected in the "dc-loops" $N_{\mathrm{dc},p}$.The elevation factor k_p of the primary is defined by

$$k_p = \frac{N_{\mathrm{ac},p}}{N_{\mathrm{dc},p}}. \tag{1}$$

If a voltage elevation is desired for the primary side, bipolar submodules are required.

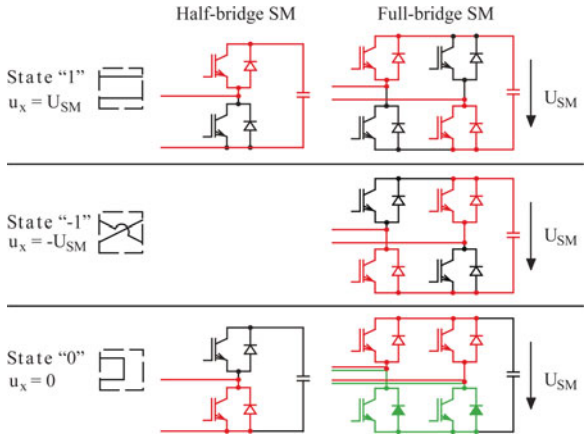

Fig. 7. Submodule states "1" and "0" for the half-bridge submodule and states "1", "−1" and "0" for the full-bridge submodule.

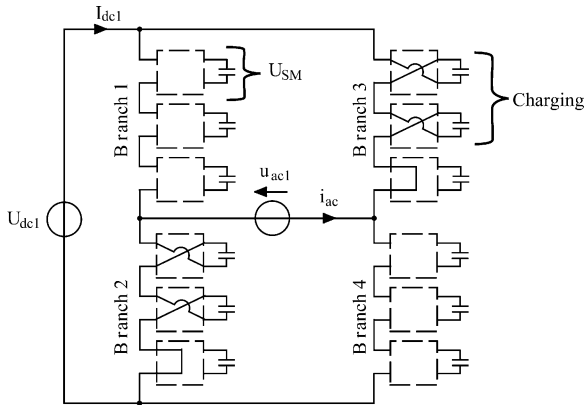

Fig. 8. Primary modulation strategy for full-bridges with a "3/-2"-modulation.

As for the secondary MMC the elevation is given by the ratio of the number of active submodules in the "dc-loops" $N_{\mathrm{dc},s}$, over the number of submodules in the "ac-loops" $N_{\mathrm{ac},s}$. $u_{\mathrm{ac}2}$ is the low-voltage ac input and $U_{\mathrm{dc}2}$ is the high-voltage dc output; therefore, unipolar submodules can be employed. The elevation factor of the secondary MMC is defined by

$$k_s = \frac{N_{\mathrm{dc},s}}{N_{\mathrm{ac},s}}. \tag{2}$$

Similar to a tap changer in ac systems, different discrete voltage steps can be achieved by changing the number of the connected submodules. The total voltage elevation of the converter is the product of the elevation of the primary converter times the elevation of the secondary converter $k_p k_s$. These factors can be changed during operation. In the following, the type of elevation will be referred to as "$N_{\mathrm{upper}}/N_{\mathrm{lower}}$"-modulation, i.e., there will be inserted N_{upper} submodules in the upper branch and N_{lower} submodules in the lower branch during the positive halfwave. The different submodule states are explained in Fig. 7.

a) Example for an elevation ratio of $k_p = 5$: As an example, an MMC with three full-bridge submodules per branch is considered with a "3/-2"-modulation. In this modulation, two "ac-loops" are created, illustrated in Fig. 8. The upper "ac-loop" is formed by the ac voltage $u_{\mathrm{ac}1}$, branch 1 and branch 3 and the

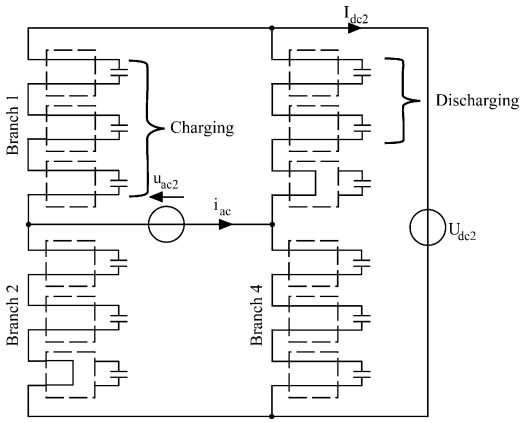

Fig. 9. Secondary elevation ratio of 5 with a "3/2"-modulation.

TABLE I
SWAPPING BALANCING SCHEME

Label	Cycle	Submodule order							Energy flow
A	+	1	2	3	4	5	6	7	Charge
B	−	1	2	3	4	5	6	7	Discharge
C	+	2	3	4	5	6	7	1	Charge
D	−	2	3	4	5	6	7	1	Discharge
E	+	3	4	5	6	7	1	2	Charge
F	−	3	4	5	6	7	1	2	Discharge
G	+	4	5	6	7	1	2	3	Charge
H	−	4	5	6	7	1	2	3	Discharge
I	+	5	6	7	1	2	3	4	Charge
J	−	5	6	7	1	2	3	4	Discharge
K	+	6	7	1	2	3	4	5	Charge
L	−	6	7	1	2	3	4	5	Discharge
M	+	7	1	2	3	4	5	6	Charge
N	−	7	1	2	3	4	5	6	Discharge

lower "ac-loop" is formed by the voltage $u_{\mathrm{ac}1}$, branch 2 and branch 4. The sum of the positively and negatively inserted submodules is the same for both "ac-loops" and in this example equal to $N_{\mathrm{ac},p} = 3 + 2 = 5$ submodules. Two "dc-loops" appear, the first consisting of the input voltage $U_{\mathrm{dc}1}$, branch 1 and branch 2 and the second formed by the input voltage $U_{\mathrm{dc}1}$, branch 3 and branch 4. The equivalent number of activated submodules (in state "1" or "-1") is identical for both "dc-loops" and in this example equal to $N_{\mathrm{dc},p} = 3 - 2 = 1$ submodule. The elevation ratio for this example is therefore $k_p = \frac{N_{\mathrm{ac},p}}{N_{\mathrm{dc},p}} = 5$.

The ac current i_{ac} is shared between the two "ac-loops" and the current stress for the submodules is therefore decreased. The input current $I_{\mathrm{dc}1}$ is shared between the two "dc-loops."

b) Example for an elevation ratio of $k_s = 5$: In this example, a "3/2"-modulation has been applied using half-bridge submodules. Two "ac-loops" are created, illustrated in Fig. 9. The upper "ac-loop" is formed by the ac voltage $u_{\mathrm{ac}2}$, branch 1 and branch 3, and the lower "ac-loop" is formed by the voltage $u_{\mathrm{ac}2}$, branch 2 and branch 4. The sum of the positively inserted submodules is the same for both "ac-loops" and in this example equal to $N_{\mathrm{ac},s} = 3 - 2 = 1$ submodule. The sum of the submodule terminal voltage in either "ac-loop" should be low if a high-voltage elevation ratio is desired.

Two "dc-loops" appear, the first consisting of the output voltage $U_{\mathrm{dc}2}$, branch 1 and branch 2 and the second formed by the voltage $U_{\mathrm{dc}2}$, branch 3 and branch 4. The equivalent number of activated submodules is identical for both "dc-loops" and in this example equal to $N_{\mathrm{dc},s} = 2 + 3 = 5$ submodules. The number of equivalently activated submodules should be high in order to obtain a high-voltage elevation ratio. The elevation ratio for this example is therefore $k_s = \frac{N_{\mathrm{dc},s}}{N_{\mathrm{ac},s}} = 5$.

Again the ac current i_{ac} respectively the dc current $I_{\mathrm{dc}2}$ are shared between the two "ac-loops" respectively the two "dc-loops."

IV. ENERGY BALANCING

To ensure a stable converter behavior, it must be assured that the different state variables such as the submodule capacitors respect the margins they have been given. That implies that the submodules voltages of a branch are balanced and that the energy in the upper and lower branch of a phase leg is equal over a whole cycle.

A. Balancing of the Submodules

The conventional way of assuring balanced submodules within an MMC branch is to measure the capacitor voltages and to establish a ranking of their voltages [20], [38]. In dependence of the current polarity and the established ranking of the voltages of the submodules, a selection algorithm decides on which submodule to insert or short-circuit in order to maintain the submodule voltages balanced. This procedure can represent a significant part of the computational burden.

In contrast, fixed switching pattern as in [39] does neither require submodule voltage measurements nor the logic necessary to decide on which submodule to insert. Drawbacks are the slower balancing process during transients and the impossibility to work with faulty submodules, which now have to be detected by a different method. To achieve voltage balancing with a fixed swapping pattern, all submodules must charge and discharge equally over one complete sequence. In the two-level modulation the submodules are connected during a fixed time, which is the same for all the active submodules. A complete cycle defines the number of different states which have to be run through in order to charge and discharge all the submodules equally. For a converter with N submodules per branch, at least N states are needed for the charging and at least N states are needed for the discharging. Therefore, a complete cycle is defined with $2N$ states, that makes N periods of the ac signal. A fixed switching pattern with the size of the complete cycle is applied as in [39]. Transients may lead to an unbalance in the submodule voltages. However, the energy balance will be restored, as it has been explained in Section IV-B.

An example illustrates the problem. The sequence from Table I is applied to the secondary MMC. A converter with seven submodules per branch realizes an elevation of $k_s = 6$ using a "7/5"-modulation. During the positive half-wave of the two-level voltage waveform, seven submodules are connected (which are charged) and during the negative half wave five

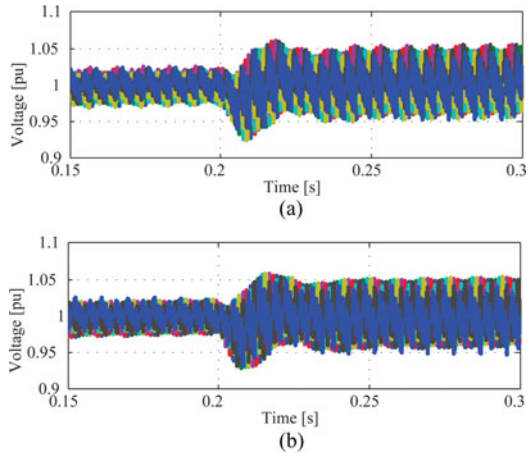

Fig. 10. Simulation results with (a) a predefined switching pattern defined in Table I. (b) The sorting function for a load step from 2.5 to 5 MW at $t = 0.2$ s.

submodules are connected (which are discharged). Table I defines the insertion order, which for the conventional balancing algorithm is based on measurements and the sorting of the submodule voltages. The letters A-N label 14 different switching patterns and the numbers 1–7 are the numbers identifying each submodule. The submodules that are inserted are framed with gray. Every line corresponds alternatively to the positive or negative half wave of the ac waveform.

Each submodule is charged seven times and discharged five times.

The discharging current is higher than the charging current, since the branch current is an alternative current with a dc offset.

Simulation results in Fig. 10(a) show that the submodule voltages stay perfectly balanced by applying this predefined switching pattern. A converter with seven submodules in the secondary has been simulated and a load step from 2.5 to 5 MW is produced at time instant $t = 0.2$ s. In steady-state conditions, each submodule has the same voltage again after the whole sequence of seven periods.

Simulation results based on the conventional sorting algorithm are shown in Fig. 10(b). The envelopes of the predefined pattern and the conventional sorting and selection algorithm follow the same dynamics.

B. Balancing of the Branch Energies

Given the discrete switching pattern of the two-level modulation, the energy balancing between the lower and upper branch cannot be influenced by modifying the switching instants.

In order to facilitate the calculation, instead of using the discrete voltage waveform of a two-level modulation, the voltage is approximated by its first harmonic given by the Fourier series, shown in

$$u_{\mathrm{ac}}^{1} \approx \frac{4}{\pi}\hat{U}_{\mathrm{rect}}\sin(\omega t + \delta). \tag{3}$$

Lets consider Fig. 11(a), where a single MMC phase leg is shown. The branch impedance is neglected in this example and the capacitors are modeled as a voltage source. An unbalance in the branch energies with an unchanged modulation has the

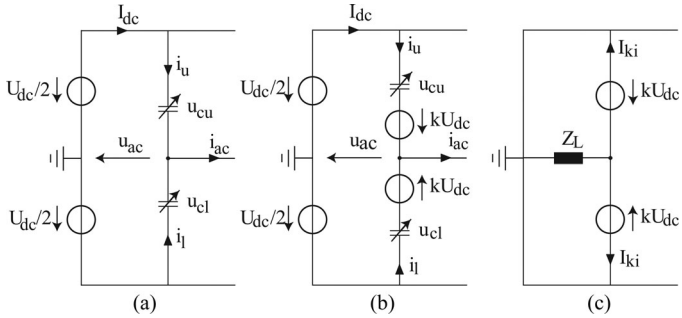

Fig. 11. (a) Balanced single leg. (b) DC bias of the branch voltage. (c) Using the superposition principle.

effect of creating a dc component on the ac signal u_{ac} on the load side.

The unbalance of the branch energies respectively branch total voltages is modeled with the introduction of additional dc voltage sources in the branches, as shown in Fig. 11(b). The additional dc source has to be added in both branches in a complementary way, since the sum of the voltages must still respect the condition

$$U_{\mathrm{dc}} = u_{\mathrm{cu}} + u_{\mathrm{cl}}. \tag{4}$$

In order to normalize the magnitudes, the parameters m and n are introduced

$$m = \frac{2\hat{U}_{\mathrm{ac}}}{U_{\mathrm{dc}}} \tag{5}$$

$$n = \frac{\hat{I}_{\mathrm{ac}}}{2I_{\mathrm{dc}}}. \tag{6}$$

The branch voltages u_{cu} and u_{cl} are now defined by (7). The parameter k expresses the dc unbalance in the upper and lower branches and relates it to the dc input voltage U_{dc},

$$\begin{aligned} u_{\mathrm{cu}} &= \frac{U_{\mathrm{dc}}}{2} - \hat{U}_{\mathrm{ac}}\sin\omega t + kU_{\mathrm{dc}} = \frac{U_{\mathrm{dc}}}{2}\left(1 + 2k - m\sin\omega t\right) \\ u_{\mathrm{cl}} &= \frac{U_{\mathrm{dc}}}{2} + \hat{U}_{\mathrm{ac}}\sin\omega t - kU_{\mathrm{dc}} = \frac{U_{\mathrm{dc}}}{2}\left(1 - 2k + m\sin\omega t\right). \end{aligned} \tag{7}$$

The unbalance causes a dc bias of the ac load. According to the Kirchhoffs laws, the dc offset will give place to a dc current, called I_{ki}, which can be found by applying the superposition principle to the circuit in Fig. 11(b), resulting in a reduced circuit of Fig. 11(c). The parameter k_i given in (8) is relating the additional dc branch current I_{ki} to the initial dc branch current I_{dc} and is depending on the parameter k. The details on the calculation are given in Appendix A

$$k_i = \frac{I_{\mathrm{ki}}}{I_{\mathrm{dc}}} = \frac{8k}{m^2\cos\phi}. \tag{8}$$

The branch currents are defined as

$$\begin{aligned} i_u &= I_{\mathrm{dc}} + \frac{\hat{I}_{\mathrm{ac}}}{2}\sin\omega t - I_{\mathrm{ki}} = I_{\mathrm{dc}}\left(1 - k_i + n\sin(\omega t + \phi)\right) \\ i_l &= I_{\mathrm{dc}} - \frac{\hat{I}_{\mathrm{ac}}}{2}\sin\omega t + I_{\mathrm{ki}} = I_{\mathrm{dc}}\left(1 + k_i - n\sin(\omega t + \phi)\right). \end{aligned} \tag{9}$$

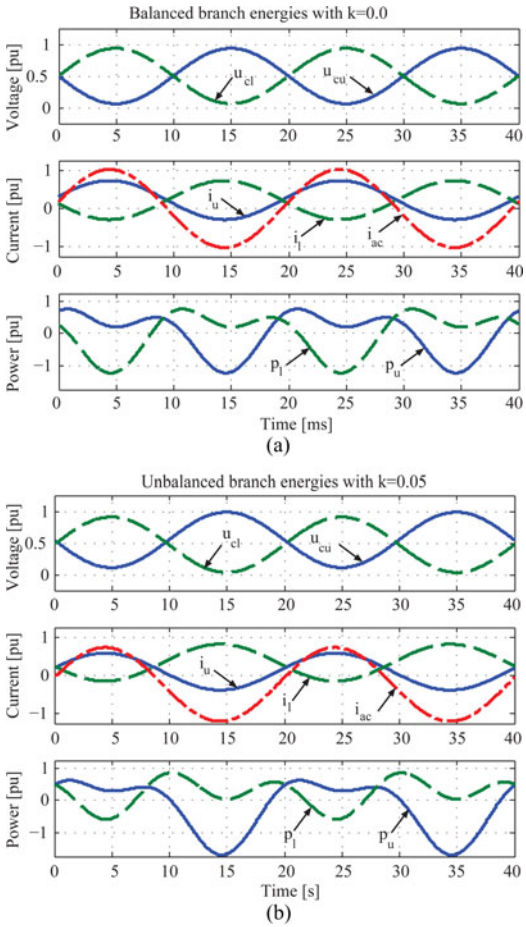

Fig. 12. Branch voltages, branch currents, and instantaneous branch powers in (a) balanced state with $k = 0.0$ and (b) unbalanced state with $k = 0.05$.

The instantaneous power issued by the capacitors $P_u = u_{\mathrm{cu}} i_u$, respectively $P_l = u_{\mathrm{cl}} i_l$ is the product of their voltage and current

$$P_u = \frac{1}{2} U_{\mathrm{dc}} I_{\mathrm{dc}} \left(1 + 2k - m \sin \omega t\right) \left(1 - k_i + n \sin(\omega t + \phi)\right)$$
$$P_l = \frac{1}{2} U_{\mathrm{dc}} I_{\mathrm{dc}} \left(1 - 2k + m \sin \omega t\right) \left(1 + k_i - n \sin(\omega t + \phi)\right). \tag{10}$$

Fig. 12(a) shows the variables of the converter in a balanced state with $k = 0.0$, whereas Fig. 12(b) shows the case of an unbalance between the branch voltages of the upper and the lower branches. The positive value of the parameter $k = 0.05$ reflects the fact that the upper branch is charged to a higher level. The branch currents i_u, i_l as well as the instantaneous power P_u, P_l are altered due to the introduction of the voltage unbalance.

The integral of the instantaneous power over one period defines the energy increase of the branch, whether on the long term the energy of the branch is increasing or decreasing. Using

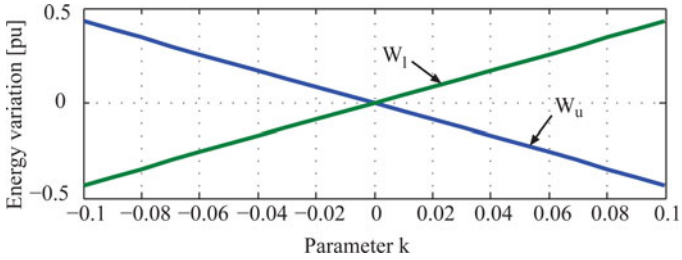

Fig. 13. Energy increase over a period in dependence of the parameter k.

TABLE II
SIMULATION PARAMETERS

Input voltage U_{dc1}	1.2kV
Output voltage U_{dc2}	18kV, 25.2kV
Nominal power P	0.36MW
Transformer ratio	1:1
AC frequency, switching frequency	1kHz
Number of submodules in the primary	4
Number of submodules in the secondary	12
Rated voltage of 1 submodule	1.25kV
Nominal phase shift δ_{max}	12°

trigonometric relations, the energy variation over a period T is

$$W_u = \int_0^T P_u \, dt = \frac{1}{2} U_{\mathrm{dc}} I_{\mathrm{dc}} \left((1 + 2k)(1 - k_i) - \frac{mn}{2} \cos \phi\right)$$
$$W_l = \int_0^T P_l \, dt = \frac{1}{2} U_{\mathrm{dc}} I_{\mathrm{dc}} \left((1 - 2k)(1 + k_i) - \frac{mn}{2} \cos \phi\right). \tag{11}$$

As it has been shown in Appendix B, a relation between the parameter n and m exist, which is defined in (18).

The energy variation is therefore given by

$$W_u = \frac{1}{2} U_{\mathrm{dc}} I_{\mathrm{dc}} \left((1 + 2k)(1 - k_i) - \left(1 - \frac{8k^2}{m^2 \cos \phi}\right)\right)$$
$$W_l = \frac{1}{2} U_{\mathrm{dc}} I_{\mathrm{dc}} \left((1 - 2k)(1 + k_i) - \left(1 - \frac{8k^2}{m^2 \cos \phi}\right)\right). \tag{12}$$

Fig. 13 depicts the quantities W_u and W_l with respect to the parameter of unbalance k. If k is positive, it means that the energy in the upper branch is higher than the energy in the lower branch. In this case, W_u is negative which means that there is a tendency to decrease the energy in the upper branch. As soon as there is an unbalance in the branch energy, which results to a condition where $k \neq 0$, the respective energy variation is favorable to establish a balanced system.

V. SIMULATION RESULTS

The single-phase structure of Fig. 4 has been simulated in MATLAB Simulink using the PLECS library. The following simulation results are based on the parameters of Table II. A multiplication of the input voltage of 15 respectively 21 times is

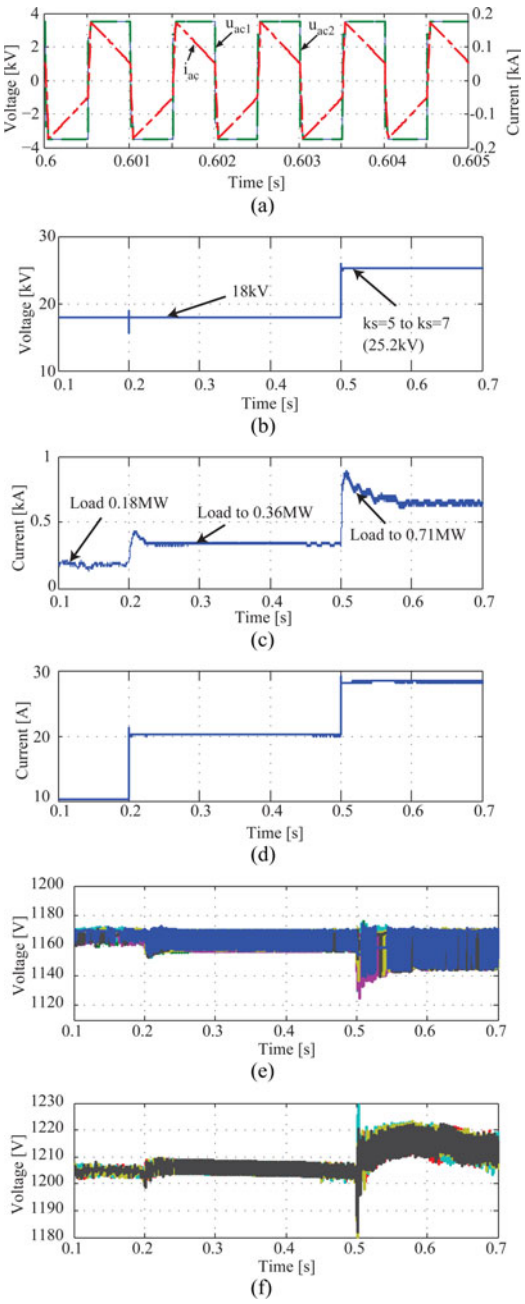

Fig. 14. Simulation results: (a) AC stage quantities u_{ac1}, u_{ac2} and i_{ac}. (b) Output voltage U_{dc2}. (c) Input current I_{dc1}. (d) Output current I_{dc2}. (e) Primary submodule voltages. (f) Secondary submodule voltages.

achieved with a transformer ratio of 1:1. The dc-link controller from [19] acts on the phase shift between the two square wave voltages at the terminals of the transformer.

In Fig. 14(a), the ac voltages and current are shown with the predicted two-level waveforms of 1 kHz. In the primary MMC an elevation of $k_p = 3$ is achieved with an "2/-1"-modulation. Therefore, the amplitude of the primary transformer voltage is $\hat{U}_{\mathrm{ac1}} = k_p U_{\mathrm{dc1}} = 3.6$ kV (without taking into account the voltage drop on the branch inductance and resistance). Since the transformer leakage inductance is low, the ac voltage waveforms require little phase shift to produce the nominal power flow.

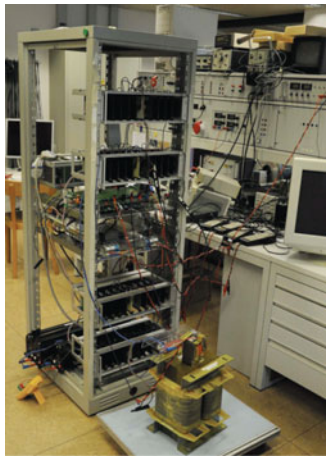

Fig. 15. Scaled down laboratory prototype.

TABLE III
PROTOTYPE PARAMETERS FOR TWO-LEVEL MODULATION

Input voltage U_{dc1}	75V
Output voltage U_{dc2}	$k_p k_s U_{dc1} = 225V$
Elevation factor	$k_p = 1$, $k_s = 3, 5$
Rated power	1kW
AC frequency, switching frequency	1kHz
Number of primary submodules N_p	4
Number of secondary submodules N_s	4

The secondary MMC is elevating the voltage by a factor $k_s = 5$; therefore, the output voltage is $U_{\mathrm{dc2}} = k_p k_s U_{\mathrm{dc1}} = 18$ kV. A "9/6"-modulation has been used, leaving three submodules for redundancy reasons. At $t = 0.2$ s, a load step from 0.18 to 0.36 MW shows the performance of the dc output voltage regulator, which controls the phase shift between the two-level ac waveforms u_{ac1} and u_{ac2}. Except for a small transient, the output voltage U_{dc2} in Fig. 14(b) remains unaffected by the load step and the currents I_{dc1} and I_{dc2} in Fig. 14(c) and 14(d) double, respectively. In Fig. 14(e) and 14(f), the voltages of the primary and secondary submodules are shown. The voltage ripple on the capacitor increases with a higher load.

At time instant $t = 0.5$ s, the elevation factor of the secondary MMC is changed from $k_s = 5$ to $k_s = 7$. The output voltage U_{dc2} rises from 18 to 25.2 kV, shown in Fig. 14(b). The consumed power in the load is almost doubled, visible in Fig. 14(c), however the output current I_{dc2} in Fig. 14(d) increases only to 28 A.

An analysis of efficiencies and component stress is outside the scope of the paper and already presented in [40].

VI. EXPERIMENTAL RESULTS

In order to validate the study, a scaled down prototype has been developed, illustrated in Fig. 15.

The parameters for the experimental tests are given in Table III. The elevation is only performed in the secondary MMC ($k_p = 1$). At time instant $t = 0.02$ s, a load step is applied from 0 to 200 W, visible in Fig. 16. The current i_{ac} shows the dynam-

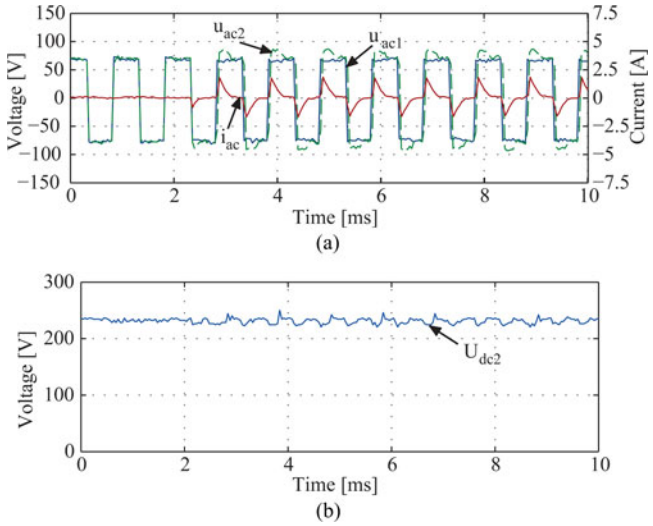

Fig. 16. Experimental results: Load step from 0 to 200 W at $t = 0.02$ s (a) AC quantities. (b) Secondary dc voltage.

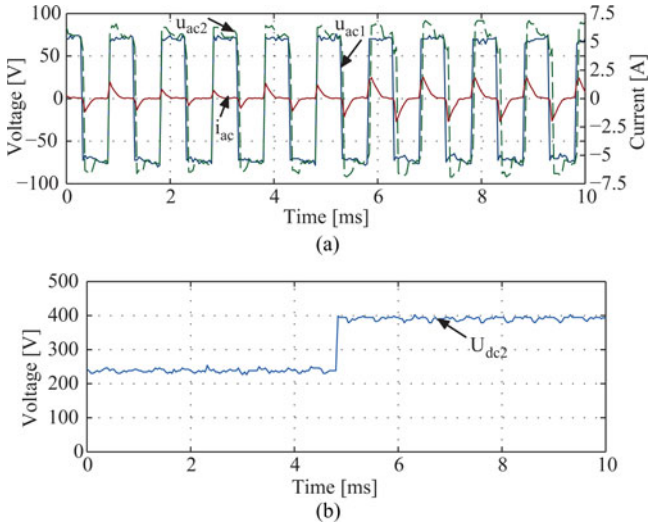

Fig. 17. Experimental results: Step change from $k_s = 3$ to $k_s = 5$ with identical resistive load (a) AC quantities (b) Secondary dc voltage.

ics of an RL-circuit, decreasing asymptotically. The relatively high branch resistance has a negative influence on the gradient and therefore the current decreases quickly. The load step does not influence the submodule voltage balancing with the fixed switching patterns, since no offset is detected on the ac signals.

In a second example, a step change in the elevation factor from $k_s = 3$ to $k_s = 5$ is produced at time instant $t = 4.8$ ms, visible in Fig. 17. The modulation method is changed from a "2/1"-modulation to a "3/2"-modulation. The initial load of 200 W at 225-V output voltage steps up to 555 W at 375-V output voltage. The feed forward controller adapts to the new set-point and regulates the output voltage at $U_{\mathrm{dc2}} = k_p k_s U_{\mathrm{dc1}} = 375$ V. The higher output voltage results in an increased power flow and a higher transformer current, since the same resistive load is connected.

VII. Conclusion

In this paper, a bidirectional dc/dc converter topology based on the MMC is proposed that consists of an MMC on the primary side, a medium frequency transformer, and another MMC at the secondary side. The presented dc/dc converter topology can be understood as a power electronic tap changer, which adapts the dc voltage levels between LV, MV, and HV dc networks. A particular modulation method that is inspired by the two-level voltage waveforms of the DAB converter has been presented. It utilizes fundamental frequency switching in the medium frequency range in order to reduce the passive components such as branch inductances and capacitors. The presented modulation method leads to adaptable and high-voltage elevation ratios at discrete levels. The energy balancing of the capacitors has been addressed both at the level of a branch and an arm. It has been shown that the energy has an intrinsic tendency to be balanced between the upper and lower branch. The proposed modulation has been verified by simulation and experimental results on a reduced scale prototype with four cells per branch.

Appendix A
Determination of the Current Coefficient Due to an Unbalance of the Branch Energies

The circuit which models the unbalance of the branch voltages is shown in Fig. 11(c). Since the two voltage sources are only dc, the current that circulates in the circuit is dc as well. The load has been represented as an slightly inductive impedance; however, if a dc current is flowing through the impedance only the resistive part is of interest. The value of the resistor can be found by considering that the power coming from the dc side is the same as the power consumed on the ac side in steady-state conditions

$$P = U_{\mathrm{dc}} I_{\mathrm{dc}} = \frac{\hat{U}_{\mathrm{ac}} \hat{I}_{\mathrm{ac}}}{2} \cos\phi \Rightarrow R = \frac{\hat{U}_{\mathrm{ac}}^2 \cos\phi}{2P}. \tag{13}$$

The additional dc current I_{ki} in the branch can therefore be calculated and simplified via the following relation:

$$I_{\mathrm{ki}} = \frac{kU_{\mathrm{dc}}}{R} = \frac{8kP}{m^2 \cos\phi U_{\mathrm{dc}}}. \tag{14}$$

Finally, the coefficient k_i can be defined by the ratio of the additional dc branch current I_{ki} and the input dc current I_{dc}:

$$k_i = \frac{I_{\mathrm{ki}}}{I_{\mathrm{dc}}} = \frac{8k}{m^2 \cos\phi}. \tag{15}$$

Appendix B
Relating AC and DC Quantities

From the analysis of the power flow, the incoming power must be equal to the outgoing power. If no unbalance of the upper and lower branch energies is given, the dc power from the source U_{dc} equals the ac power consumed by the load. If an unbalance

happens, the ac load is biased by a dc component which in turn has to be paid attention to. To the consumed power on the ac side, a term with respect to the power dissipation due to the unbalance is introduced

$$P = U_{\mathrm{dc}} I_{\mathrm{dc}} = \frac{\hat{U}_{\mathrm{ac}} \hat{I}_{\mathrm{ac}}}{2} \cos\phi + 2 I_{\mathrm{ki}} k U_{\mathrm{dc}}. \tag{16}$$

By using (14), it is possible to reformulate the power balance

$$P = U_{\mathrm{dc}} I_{\mathrm{dc}} = \frac{\hat{U}_{\mathrm{ac}} \hat{I}_{\mathrm{ac}}}{2} \cos\phi + 2 \frac{8kP}{m^2 \cos\phi U_{\mathrm{dc}}} k U_{\mathrm{dc}}. \tag{17}$$

Finally, with the help of (5) and (6), a relation between m and n can be found

$$\frac{2}{m \cos\phi} \left(1 - \frac{8k^2}{m^2 \cos\phi} \right) = n. \tag{18}$$

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