Hybrid AC Power Source Based on Modular Multilevel Converter and Linear Amplifier

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***Abstract*—This paper presents a hybrid amplifier for an ac power source (ACPS). The topology is composed of a modular multilevel converter (MMC), operating as main amplifier, connected in series with a linear power amplifier (LPA), which operates as correction amplifier. This way, it is possible to gather the modularity, reliability, and high efficiency provided by the MMC and the high waveform fidelity provided by the LPA. Additionally, it is possible to reproduce a voltage waveform with a high bandwidth and, differently from previous works, with a topology that requires a unique dc voltage source for the main amplifier. The inner current and the submodule capacitor voltages are controlled in the MMC. Meanwhile, the LPA is controlled to define the output voltage. A design methodology and experimental results are included to demonstrate the operation of the ACPS topology.**

***Index Terms*—Hybrid ac power source (ACPS), modular multilevel converter (MMC), series configuration.**

I. Introduction

In last decades, the development of power electronics technology has driven the evolution of static power converters in terms of dynamic response, efficiency, and power density [1]–[3]. These features have prompted the power electronic engineers to look for new applications. Among these new applications stands out the power amplifiers, which formerly employed only linear electronic systems (such as class-A, class-B, and class-AB amplifiers). Despite the high fidelity provided by the linear technology, these systems inherently have low efficiency due to the transistor bias circuit [4].

On the other hand, in applications where the fidelity is not the main concern, switching mode amplifier technologies, such as class-D and class-E amplifiers, can be used. It is well known that such switching amplifiers usually present high efficiency, since they employ transistors operating just in the cutoff and saturation regions. However, the switching amplifiers suffer with time-delays, nonlinearities, electromagnetic emissions, and limited bandwidth due to passive filtering requirements [5], [6].

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Based on these features, the interest in hybrid power amplifiers (HPA) has emerged recently, aiming to overwhelm the aforementioned limitations, gathering, into the same topology, the high fidelity waveforms provided by the linear power amplifier (LPA) and the high efficiency achieved with switched-mode power amplifiers (SMPA). The HPAs have been implemented through the association of an LPA and an SMPA in series [5]–[8], parallel [9]–[11] or envelope configurations [12], [13]. In the series configuration, the SMPA synthesizes a voltage waveform close to the reference signal, while the LPA makes only small corrections, mitigating the differences between the SMPA voltage waveform and the reference signal. Hence, the LPA (correction amplifier) processes a small amount of the load power whereas the SMPA (main amplifier) supplies the most of the load power. As discussed in [7], the series configuration is suitable for ac power source (ACPS) applications, where the high efficiency of an SMPA together with the fast dynamic response and reliability of an LPA result in a suitable performance [14]–[16].

Regarding to the main amplifier, multilevel converters enable the use of semiconductors with low blocking voltage and associated low on-state voltage drop, so that it is possible to reduce the conduction losses [17]–[22]. Usually, cascaded multilevel converters have been used to implement the main amplifier stage due to its inherent modularity [6], [7]. However, the conventional cascaded multilevel converter requires isolated dc voltage sources to supply each cell, increasing the complexity, weight, and system cost implementation. To overcome this disadvantage, a new multilevel configuration called modular multilevel converter (MMC) was proposed recently [18]. Nowadays, the MMC is one of the main state-of-the-art power converters for high power and high voltage applications (e.g., high voltage direct current transmission), but it can also be attractive for low power applications, since it is possible to increase the number of levels easily, even using a unique dc voltage source [18]–[34].

Based on this fact, this paper presents an HPA topology, which uses the MMC operating as main amplifier [25]. This topology requires only one dc voltage source to supply the main amplifier, simplifying the HPA input power stage in comparison with previous works [6], [7]. A theoretical analysis is shown to demonstrate the basic operation of the HPA and its control system. In addition, a design methodology is proposed to define the main parameters of the MMC and the dc bus voltage level of the LPA. Experimental results are also included to evaluate the proposed HPA under distinct operating conditions.

This paper is organized as follows: Section II presents the proposed hybrid ACPS topology. Section III discusses the control approach of the main and correction amplifiers. In Section IV, a

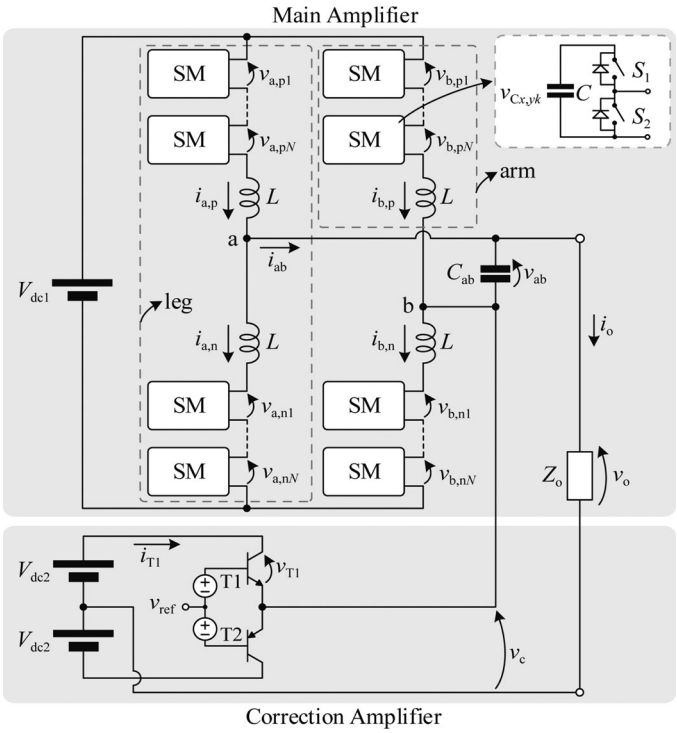

Fig. 1. Proposed hybrid ACPS topology.

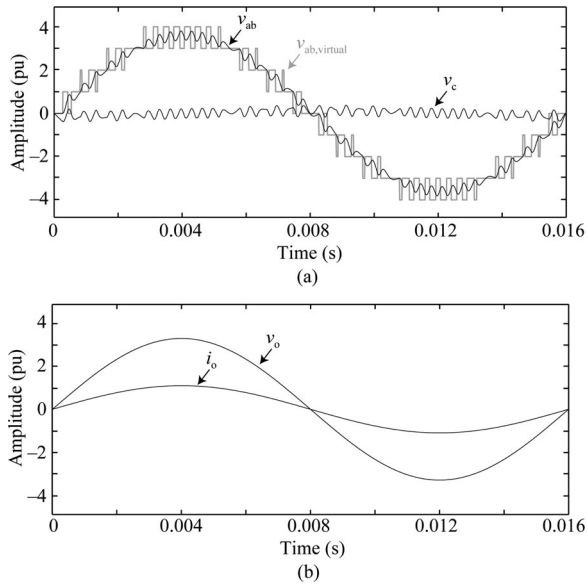

Fig. 2. Theoretical waveforms with sinusoidal reference and resistive load.

design methodology is explained. Section V presents the experimental validation of the proposed topology. Finally, Section VI summarizes the paper and presents the main conclusions.

II. Hybrid ACPS Topology

The ACPS considered hereinafter is based on a series HPA topology, composed of an MMC, operating as main amplifier, and an LPA, operating as correction amplifier. This ACPS should synthesize a controlled voltage waveform to the load Z_o, as presented in Fig. 1. Basically, the LPA acts as a series active power filter with a high bandwidth, processing a small amount of the load power. On the other hand, the MMC is designed to supply most of the load power, since it has a better efficiency than the LPA.

A. Basic Operation of the MMC

The adopted MMC structure, shown in Fig. 1, is based on a full-bridge configuration to reduce the amplitude of the dc bus voltage level $V_{\rm dc1}$ for a given output voltage amplitude. Each leg x ($x = \{\rm a,b\}$) is composed of two arms y ($y = \{\rm p,n\}$). These arms have a series connection of N half-bridge submodules (SM) and also include an inductance L to limit the current ripple at switching frequency through the arms. As can be seen in Fig. 1, an output capacitor $C_{\rm ab}$ is added to the MMC ac output to implement an equivalent second-order low-pass filter with the effective ac inductance caused by the arm inductors. This second-order low-pass filter should reduce the $v_{\rm ab}(t)$ switching harmonics and guarantee that the voltage ripple amplitude is within the limits of the LPA output voltage capability.

Each arm synthesizes a multilevel voltage, which depends on each SM output voltage $v_{x,yk}(t)$ ($k = 1, 2, \ldots, N$). To synthesize the multilevel arm voltages, the modulating signals of each SM are compared with phase-shifted triangular carriers to generate the command signals for the SM switches. With a phase-shift (PS) modulation strategy it is possible to synthesize $2N+1$ levels in the leg voltages and, consequently, $4N+1$ levels in the MMC output (phase-to-phase) voltage [21], [24].

The SM voltages $v_{x,yk}(t)$ generates a virtual voltage before the second-order filter, which is composed of each arm voltage $v_{x,y}(t)$, defined as

$$v_{\rm ab,virtual}(t) = \frac{v_{a,n}(t) - v_{a,p}(t) - v_{b,n}(t) + v_{b,p}(t)}{2} \quad (1)$$

where

$$v_{x,y}(t) = \sum_{k=1}^{N} v_{x,yk}(t). \quad (2)$$

The virtual voltage $v_{\rm ab,virtual}(t)$ is filtered by the second-order low-pass filter, resulting in the MMC output voltage $v_{\rm ab}(t)$. And, the ACPS output voltage $v_o(t)$ is given by

$$v_o(t) = v_c(t) + v_{\rm ab}(t). \quad (3)$$

It is important to highlight that the output voltage waveform $v_o(t)$, obtained from the voltages synthesized by the MMC $v_{\rm ab}(t)$ and by the LPA $v_c(t)$, presents a high-fidelity, when compared to the reference signal. The main theoretical voltage waveforms for eight SMs in the main amplifier ($N = 2$) are shown in Fig. 2(a). The filtered output voltage of the main amplifier $v_{\rm ab}(t)$ can be seen together with the virtual multilevel pulse-width modulation (PWM) voltage $v_{\rm ab,virtual}(t)$ in Fig. 2(a). The waveform synthesized by the linear amplifier is the compensation voltage $v_c(t)$. According to (3), the association of these two voltage waveforms results in a high fidelity output voltage $v_o(t)$, as can be observed in Fig. 2(b).

With the MMC operation, the arm currents $i_{x,p}(t)$ and $i_{x,n}(t)$ ideally have a dc component and a fundamental frequency ac component. This ac fundamental component of the arm current flows through the SMs capacitors, resulting in an SM capacitor voltage ripple at the fundamental frequency and its multiples [27]. The interaction between the arm inductors and the SM capacitors also results in circulating currents composed predominantly of the second-order component $i_{2f,x}(t)$. Moreover, high-frequency components also occur if the modulation strategy results in nonzero voltage across the arm inductors [33], [34]. So, the arm currents can be defined as

$$i_{x,p}(t) = i_{\mathrm{dc},x}(t) + \frac{i_x(t)}{2} + i_{2f,x}(t) + i_{fs,x}(t) \tag{4}$$

$$i_{x,n}(t) = i_{\mathrm{dc},x}(t) - \frac{i_x(t)}{2} + i_{2f,x}(t) + i_{fs,x}(t) \tag{5}$$

where $i_{\mathrm{dc},x}(t)$ refers to the active power extracted from the dc source and it is equally distributed in all SMs of one leg, $i_x(t)$ is the output leg current, $i_{2f,x}(t)$ is the low-frequency circulating current component at twice the fundamental frequency and $i_{fs,x}(t)$ is the high-frequency circulating current component that appears when the modulation strategy produces nonzero voltage across the arm inductors L.

In addition, the MMC operation results in an internal current $i_{\mathrm{int},x}(t)$ in each leg x, which is composed of the common components of the arm currents $i_{x,p}(t)$ and $i_{x,n}(t)$ [22]–[34], given by

$$i_{\mathrm{int},x}(t) = \frac{i_{x,p}(t) + i_{x,n}(t)}{2}. \tag{6}$$

B. MMC Equivalent Circuit

An MMC equivalent circuit is developed in this section. This helps on the understanding of MMC concepts related to the power balance in the circuit, as well as to derive simplified dynamic models for the MMC control system and ACPS design.

Applying the Kirchhoff voltage law to an MMC leg leads to the following equivalent dc and ac side dynamic equations related to the current variables

$$2L\frac{di_{\mathrm{dc},x}(t)}{dt} = V_{\mathrm{dc1}} - \bar{v}_{x,p}(t) - \bar{v}_{x,n}(t) \tag{7}$$

$$\frac{L}{2}\frac{di_x(t)}{dt} = \frac{v_{x,n}(t) - v_{x,p}(t)}{2} - v_x(t) \tag{8}$$

where $\bar{v}_{x,y}(t)$ are the dc components of the MMC arm voltages.

The inductances in (7) and (8) can be used to define equivalent dc and ac side inductances, respectively, as

$$L_{\mathrm{e,dc}} = 2L \text{ and } L_{\mathrm{e,ac}} = \frac{L}{2}. \tag{9}$$

Moreover, the SMs operation inserts or bypasses the capacitors in an arm, connecting these ones in series. This way, the minimum capacitance $C_{\min}$ that arises in the MMC arm, used in the MMC equivalent circuit, can be calculated through [23], [27]:

$$C_{\min} = \frac{C}{N}. \tag{10}$$

On the other hand, the current and voltage components through $C_{\min}$ can be represented by dependent current and voltage sources, which vary according to the modulating signals. These dependent sources relate the currents $i_{\mathrm{dc},x}(t)$ and $i_x(t)$, defined in the previous section, with the capacitor currents $\bar{i}_{\mathrm{C},x,y}(t)$ and $\tilde{i}_{\mathrm{C},x,y}(t)$, such as

$$\bar{i}_{C,x,y}(t) = m_{\mathrm{dc},x}(t) i_{\mathrm{dc},x}(t) \tag{11}$$

$$\tilde{i}_{C,x,y}(t) = [m_{\mathrm{ac},x}(t) \mp m_{\mathrm{ref},x}(t)]\frac{i_x(t)}{2} \tag{12}$$

and relates the arm capacitor voltages $v_{C,x,y}(t)$ with the output SM voltages $\bar{v}_{x,y}(t)$ and $v_{x,y}(t)$

$$\bar{v}_{x,y}(t) = m_{\mathrm{dc},x}(t) v_{C,x,y}(t) \tag{13}$$

$$v_{x,y}(t) = m_{x,y}(t) v_{C,x,y}(t) \tag{14}$$

where

$$m_{x,\mathrm{p}}(t) = m_{\mathrm{dc},x}(t) + m_{\mathrm{ac},x}(t) - m_{\mathrm{ref},x}(t) \tag{15}$$

$$m_{x,\mathrm{n}}(t) = m_{\mathrm{dc},x}(t) + m_{\mathrm{ac},x}(t) + m_{\mathrm{ref},x}(t). \tag{16}$$

According to (15) and (16), the modulating signals for the positive and negative arms, $m_{x,p}(t)$ and $m_{x,n}(t)$, respectively, are composed of a dc component $m_{\mathrm{dc},x}(t)$, an ac component $m_{\mathrm{ac},x}(t)$ and an ac reference component $m_{\mathrm{ref},x}(t)$. The component $m_{\mathrm{dc},x}(t)$ is used to regulate the sum of the dc capacitor voltages in each leg to $2V_{\mathrm{dc1}}$, and its value is ideally equal to 0.5. The term $m_{\mathrm{ref},x}(t)$ is the main ac component used to define the ACPS output voltage waveform, where $m_{\mathrm{ref},a}(t) = -m_{\mathrm{ref},b}(t)$. Moreover, the component $m_{\mathrm{ac},x}(t)$ is an ac contribution produced by the control system to balance the arm voltages in each leg.

An equivalent circuit for an MMC leg can be conceived from (7)–(14) as shown in Fig. 3. Basically, this circuit presents the virtual power transfer from dc side to ac side through one MMC leg, which occurs when a load is connected to the ac side.

From this circuit, it is also possible to obtain dynamic equations related to the sum and subtraction of the equivalent capacitor voltages, since they have to be controlled [33], [34]. Considering just the components that contribute to the active power processing, the dynamic equations are given by

$$C_{\min}\frac{dv^{+}_{\mathrm{C},x}(t)}{dt} = 2i_{\mathrm{dc},x}(t)m_{\mathrm{dc},x}(t) - i_x(t)m_{\mathrm{ref},x}(t) \tag{17}$$

$$C_{\min}\frac{dv^{-}_{\mathrm{C},x}(t)}{dt} = i_x(t)m_{\mathrm{ac},x}(t) \tag{18}$$

where $v^{+}_{C,x}(t)$ is the sum of the equivalent capacitor voltages and $v^{-}_{C,x}(t)$ is the subtraction of these ones.

C. Linear Power Amplifier

The LPA guarantees the desired high fidelity voltage waveform (compared to the reference signal) at the output of the ACPS. Therefore, the called correction amplifier should compensate for the voltage ripple of the main amplifier, phase displacement and possible under/overshoot caused by load changes.

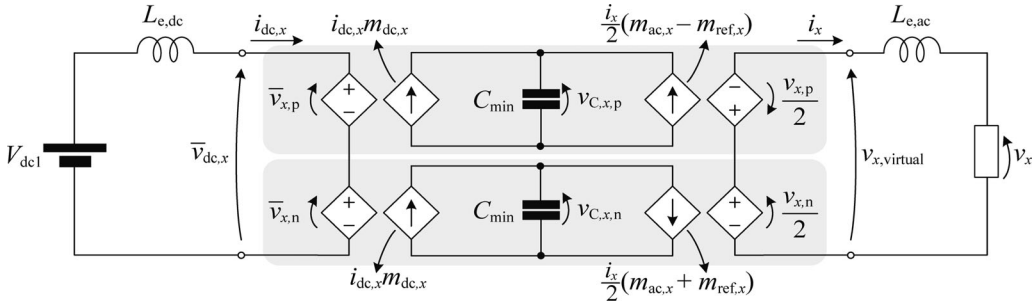

Fig. 3. Equivalent model for an MMC leg.

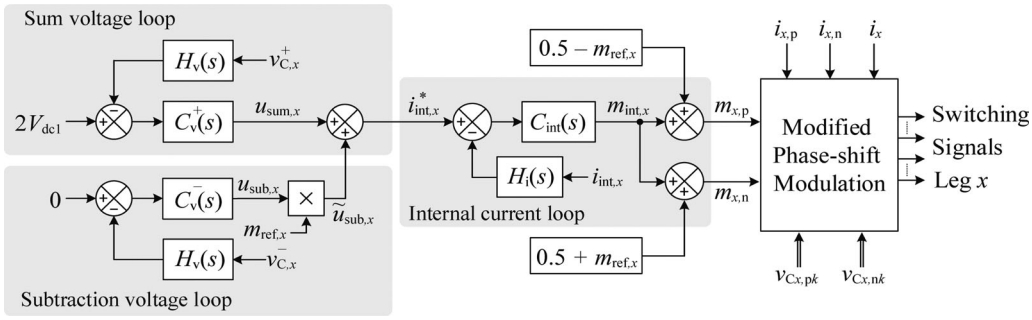

Fig. 4. MMC control system applied to the leg x.

The compensation capability of the correction amplifier is limited by its dc bus voltage level $V_{\rm dc2}$, which directly influences the LPA conduction losses. As already known, the linear technology has low efficiency, such as the class A that has a maximum efficiency of 50% or class AB with efficiencies around 75% [8]. To maximize the LPA efficiency and, consequently, the overall ACPS efficiency, the LPA dc bus voltage should be adequately designed, as addressed in Section IV.

III. HPA Control System

The proposed HPA control system should guarantee high fidelity of the ACPS output voltage. Based on this specification, the main amplifier output voltage $v_{\rm ab}(t)$ is open-loop controlled, while the correction amplifier is closed-loop controlled to synthesize the output voltage $v_o(t)$ as close as possible to the reference $v_{\rm ref}(t)$. Therefore, the output impedance and the overall stability of the HPA are determined exclusively by the correction amplifier [6], [7], [14].

A. MMC Control Approach

The MMC control system has three control loops for each leg: one to control the inner current, reducing the circulating components, and other two to set the inner current reference through the sum and subtraction capacitor voltages loops [33].

Fig. 4 shows the block diagram of the complete MMC control system. The outer voltage control loops aim to provide the reference of the inner current loop and, consequently, to maintain the power flow balance between the load and dc bus. The sum and subtraction voltage control loops ensure, respectively, that the sum of all capacitor voltages in a leg is equal to $2V_{\rm dc1}$ and the difference between the arm capacitor voltages is equal to zero. With these control loops, the power balance of the converter is guaranteed [33], [34].

Therefore, the arm modulating signal $m_{x,y}(t)$ is obtained by adding up the resulting control action of the inner current loop to the reference signal

$$\begin{aligned} m_{x,p}(t) &= \overbrace{\frac{1}{2}+\Delta m_{{\rm dc},x}(t)}^{m_{{\rm dc},x}(t)} + m_{{\rm ac},x}(t) - m_{{\rm ref},x}(t) \\ &= \frac{1}{2} + m_{{\rm int},x}(t) - m_{{\rm ref},x}(t) \end{aligned} \tag{19}$$

$$\begin{aligned} m_{x,n}(t) &= \frac{1}{2} + \Delta m_{{\rm dc},x}(t) + m_{{\rm ac},x}(t) + m_{{\rm ref},x}(t) \\ &= \frac{1}{2} + m_{{\rm int},x}(t) + m_{{\rm ref},x}(t) \end{aligned} \tag{20}$$

where $m_{{\rm ref},x}(t)$ is the open-loop reference signal, which represents the desired output voltage waveform, and $m_{{\rm int},x}(t)$ is the resulting control action of an MMC leg, which is the sum of the dc component variation $\Delta m_{{\rm dc},x}(t)$ and the ac component $m_{{\rm ac},x}(t)$. The term $\Delta m_{{\rm dc},x}(t)$ controls the dc component of the inner current and, as mentioned before, the ac component $m_{{\rm ac},x}(t)$ controls the fundamental component of the inner current for the positive and negative arm voltage balance.

Since dc reference signals are applied to the inner current and outer voltage control loops, proportional-integral (PI) controllers are used in $C_{\rm int}(s)$, $C_v^+(s)$, and $C_v^-(s)$. Additionally, to minimize the ac component in the inner current at twice of the output fundamental frequency, the outer control loops bandwidths should be slower than the ripple frequencies present in the sum and subtraction of the capacitor voltages. Additionally, the inner current control loop should have a high bandwidth

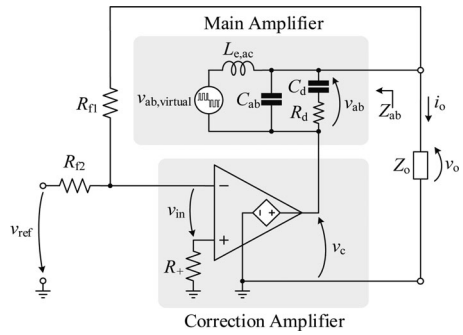

Fig. 5. HPA output voltage control system (similar to [6]).

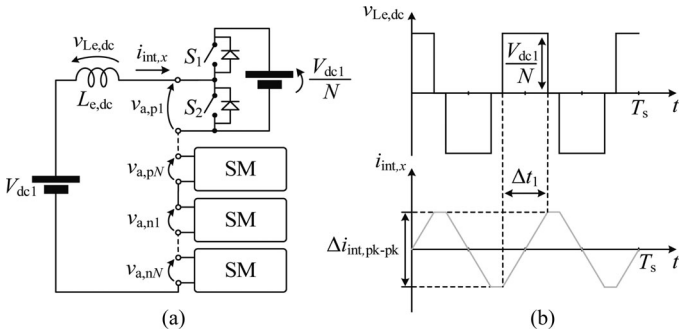

Fig. 6. Arm inductor current ripple analysis. (a) Equivalent circuit. (b) Theoretical voltage and current ripple waveforms.

to track the inner current reference with satisfactory dynamic performance.

It is important to highlight that the outer voltage control loops do not guarantee the individual capacitor voltages balancing for the SMs of the same arm. This way, the individual capacitor voltages are balanced by a sorting algorithm combined with PS modulation, which selects the SMs according to the capacitor voltages and arm current direction [34].

B. LPA Control Approach

In series configuration of HPAs the output voltage of the main amplifier is usually open-loop controlled. On the other hand, the correction amplifier is controlled in closed-loop to guarantee that the output voltage tracks the reference signal [6], [7]. Fig. 5 shows the control diagram of the correction amplifier, which controls the output voltage of the ACPS [6]. The main amplifier reference $v_{\rm ref}(t)$ is applied directly to the correction amplifier terminals through the resistor R_{f2}.

IV. ACPS Design Methodology

This section presents an ACPS design methodology to define all dc bus voltage levels, passive components of the output low-pass filter as well as SMs capacitance. For this analysis, the following assumptions are considered:

1) the output low-pass filter cut-off frequency is around one decade below the equivalent main amplifier output switching frequency (i.e., $f_n = 4Nf_s$ /10);
2) the ACPS must guarantee a high-quality voltage waveform for a load step from no-load to 40% of the nominal load;
3) the output voltage reference of the ACPS is a sinusoidal waveform.

A. Main Amplifier DC Bus Voltage Level

The main amplifier has a single dc bus, which is defined by the maximum output voltage amplitude that the ACPS should synthesize, given by

$$V_{\rm dc1} = \frac{V_{o,\rm pk,max}}{m_{\rm a}} \tag{21}$$

where $V_{o,\rm pk,max}$ is the maximum amplitude of ACPS output voltage and m_a is the desired amplitude modulation index.

B. Output Second-Order Low-Pass Filter

The output second-order low-pass filter is composed of a capacitor $C_{\rm ab}$ and an equivalent output inductance $L_{e,\rm ac}$. This inductance can be computed from the arm inductance L, which can be determined from the specification of the maximum arm inductor current ripple. Then, the capacitor $C_{\rm ab}$ can be determined from the specified cut-off frequency of the output filter, which had been defined at one decade below the equivalent output switching frequency ($4Nf_s$/10) to minimize the dc bus voltage level of the correction amplifier. However, it is necessary to verify if the output voltage ripple is below the voltage capability of the LPA.

Therefore, to obtain the instantaneous and the maximum current ripple in $L_{e,\rm dc}$, an equivalent circuit is shown in Fig. 6, based on the dc side of the equivalent circuit analysis presented in Section II. In this circuit, the SM capacitors are replaced by dc voltage sources, to guarantee that only the high-frequency circulating current components are present.

Applying PS PWM in the equivalent circuit shown in Fig. 6(a), the arm inductor voltage $v_{\rm Le,dc}(t)$ and the instantaneous peak-to-peak current ripple $\Delta i_{\rm int,pk\text{-}pk}(t)$ can be obtained, as shown in Fig. 6(b). The peak-to-peak value of the current ripple can be found as

$$\Delta i_{\rm int,pk\text{-}pk}(t) = \frac{V_{\rm dc1}\Delta t_1(t)}{L_{e,\rm dc}N} \tag{22}$$

where Δt_1 is the time interval in which voltage $V_{\rm dc1}$/N is applied across $L_{e,\rm dc}$.

To define the maximum current ripple in $L_{e,\rm dc}$, the time interval Δt_1 is obtained in sectors. This time interval is used to define the peak-to-peak current ripple through the arm inductors in each sector and is obtained by subtracting the nearest voltage level $f(t)$ from the sinusoidal reference waveform $g(t)$, as illustrated in Fig. 7(a). In addition, in some levels, the resultant waveform must be multiplied by –1, as can be seen in the lower graphic of Fig. 7(a). So, the instantaneous time interval can be

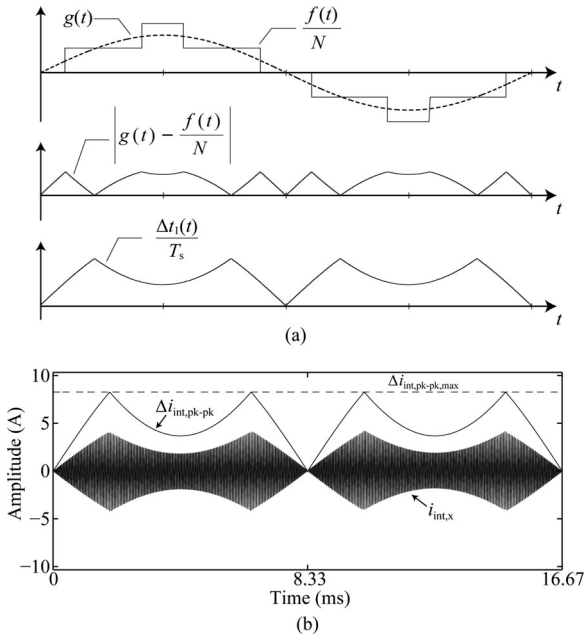

Fig. 7. Current ripple analysis. (a) Auxiliary waveforms to obtain the peak-to-peak current ripple. (b) Theoretical peak-to-peak value of the current ripple and simulated current ripple waveforms with PS PWM and odd number of SMs ($V_{\rm dc1} = 400$ V, $N = 2$, $L = 0.3$ mH, $f_s = 10.08$ kHz, $m_a = 0.78$, and $\omega_x = 2\pi 60$ rad/s).

computed as follows:

$$\Delta t_1(t) = \begin{cases} \left[(-1)^{f(t)} \cdot \left| g(t) - \dfrac{f(t)}{N} \right| + \dfrac{(-1)^{f(t)+1}+1}{2N}\right] T_{\rm s}, \\ \qquad\qquad N \rightarrow \text{even} \\ \left[(-1)^{f(t)+1} \cdot \left| \dfrac{f(t)}{N} - g(t) \right| + \dfrac{(-1)^{f(t)}+1}{2N}\right] T_{\rm s}, \\ \qquad\qquad N \rightarrow \text{odd} \end{cases} \tag{23}$$

where

$$g(t) = m_a \sin(\omega_x t) \tag{24}$$

$$f(t) = \text{round}(N m_a \sin(\omega_x t)) \tag{25}$$

and the function round(z) rounds the value of z to the nearest integer.

The maximum peak-to-peak current ripple can be obtained from (22), and it is given by

$$\Delta i_{\rm int,pk\text{-}pk,max} = \frac{V_{\rm dc1}}{4 L f_{\rm s} N^2}. \tag{26}$$

For instance, Fig. 7(b) presents the theoretical peak-to-peak current ripple, obtained from (22) for $N = 2$, and the simulated current ripple from the equivalent circuit shown in Fig. 6(a).

C. Correction Amplifier DC Bus Voltage Level

As discussed before, the LPA dc bus voltage level should be enough to compensate for the output voltage ripple and phase lag introduced by the second-order low-pass filter and the modulation strategy of the main amplifier. In addition, the voltage drop in the inductor as well as the voltage variations over SM capacitors are both included as design parameters (note that an undershoot over SM capacitors limits maximum modulation index of the main amplifier). Thus, the minimum dc voltage of the correction amplifier can be expressed as

$$V_{\rm dc2,min} = \frac{\Delta v_{\rm ab,ripple} + \Delta v_{\rm cap,ripple}}{2} + \Delta v_{\rm ab,phase} + \max(\Delta v_{\rm ab,pert}, \Delta v_{\rm ab,ctrl}) \tag{27}$$

where $\Delta v_{\rm ab,ripple}$ is the maximum output voltage ripple of the MMC output voltage, $\Delta v_{\rm cap,ripple}$ is the maximum SM capacitor voltage ripple, which contributes to the output voltage oscillation mainly when low-frequency waveform is synthesized, and $\Delta v_{\rm ab,phase}$ is the maximum output voltage error introduced by the phase displacement of the output filter and phase lag of the modulation strategy under nominal load. Moreover, $\Delta v_{\rm ab,pert}$ and $\Delta v_{\rm ab,ctrl}$ are the output voltage variations when a load step occurs, as illustrated in Fig. 8, which have distinct dynamics. The function $\max(z_1, z_2)$ returns only the largest element.

The variables $\Delta v_{\rm ab,ripple}$ and $\Delta v_{\rm ab,phase}$ were already analyzed in [7]. On the other hand, the variables $\Delta v_{\rm ab,pert}$ and $\Delta v_{\rm ab,ctrl}$ resulting from a load step can be obtained from the equivalent circuits shown in Fig. 9. One can observe from Fig. 9(a) that the dynamic response of the total dc bus voltage control loop [which uses the controller $C_v^+(s)$] is taken into

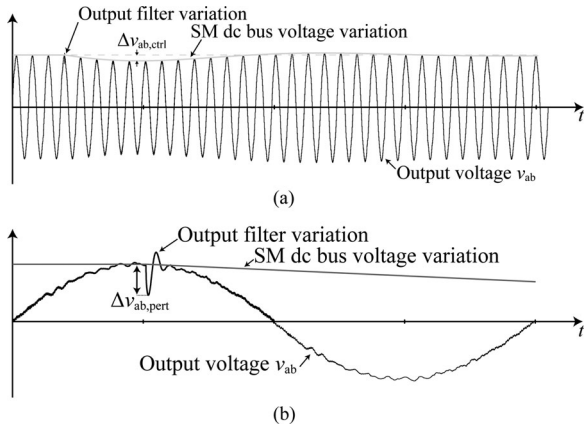

Fig. 8. Voltage variations for a load step change: (a) SM dc bus voltage variation $\Delta v_{\rm ab,ctrl}$ and (b) output filter voltage variation $\Delta v_{\rm ab,pert}$.

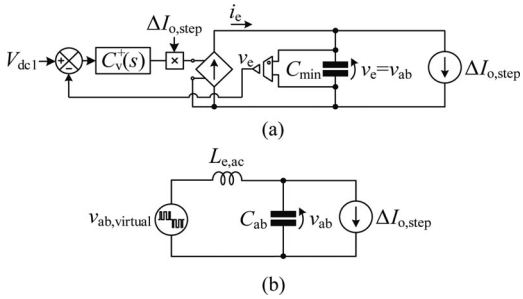

Fig. 9. Equivalent models used in the voltage undershoot analysis. (a) Equivalent circuit to determine SM dc bus voltage variation $\Delta v_{\rm ab,ctrl}$. (b) Equivalent circuit to determine the output filter voltage variation $\Delta v_{\rm ab,pert}$.

TABLE I
PROPOSED ACPS PARAMETERS

System	Parameter	Value
ACPS	Maximum output power	S_o = 1 kVA
	Maximum output voltage	$V_{o,pk}$ = [0 311] V
	Output frequency limits	f_a = [30 400] Hz
LPA (MP111A)	Dc bus voltage	V_{dc2} = 25 V
	Feedback resistors	R_{f1} = 270 kΩ
		R_{f2} = 8.89 kΩ
MMC	SMs per arm	N = 2
	Number of levels (v_{ab})	m = 9
	Total dc bus voltage	V_{dc1} = 400 V
	SM capacitor voltages	$V_{Cx,yk}$ = 200 V
	Switching frequency	f_s = 10.08 kHz
	Sampling frequency	f_{sp} = 20.16 kHz
	Arm inductance	L = 300 µH
	SM capacitance	C = 940 µF
	Passive damping	C_d = 3 µF
		R_d = 3.9 Ω
	Output filter capacitance	C_{ab} = 940 nF
	Amplitude modulation index	m_a = 0.7778

account for estimating the SM dc bus voltage variation $\Delta v_{\mathrm{ab,ctrl}}$ caused by a load step $\Delta I_{o,\mathrm{step}}$. As the dynamic of the output low-pass filter is fast compared to the dynamic of dc bus voltage, the output low-pass filter is disregarded in the model shown in Fig. 9(a). On the other hand, to obtain the parameter $\Delta v_{\mathrm{ab,pert}}$ when a load step $\Delta I_{o,\mathrm{step}}$ occurs, the dc capacitor voltages are considered constant and the output second-order low-pass filter is represented by the equivalent ac inductor $L_{e,\mathrm{ac}}$ and the output capacitor C_{ab}, as presented in Fig. 9(b).

D. SM Capacitor

The SM capacitor design should guarantee that the voltage undershoot in all SMs capacitors due to a load step does not exceed the dc bus voltage capability of the LPA. To simplify the analysis, the voltage undershoot on the SM capacitors can be disregarded if it is smaller than the output voltage undershoot on C_{ab} for the same load condition. Therefore, assuming that $\Delta v_{\mathrm{ab,ctrl}} < \Delta v_{\mathrm{ab,pert}}$ and considering that these two perturbations do not occur at the same time, the $\Delta v_{\mathrm{ab,ctrl}}$ can be neglected in (27). This condition must be guaranteed during the design (as shown in the next section).

E. Design Example

Based on the proposed design methodology and using the parameters presented in Table I, the abaci shown in Fig. 10 are obtained and the HPA is designed.

Initially, a maximum peak-to-peak current ripple through the arm inductors is defined. For this example, the maximum peak-to-peak current ripple was defined as 65% of $I_{o,\mathrm{pk}}$. Therefore, using (26), the minimum inductance that guarantees this current ripple is $L_{\min} = 300$ μH. Moreover, the capacitor C_{ab} can be determined using $L_{\min}$ and the output filter cut-off frequency specified in the design assumptions ($4Nf_s/10$). With this, the capacitance C_{ab} is 0.94 μF.

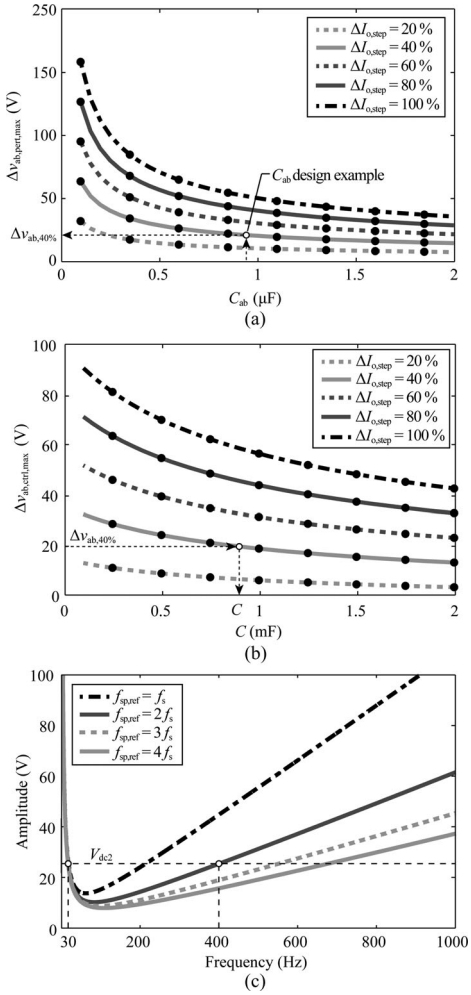

Fig. 10. Design example. (a) Selection of $\Delta v_{\mathrm{ab,pert}}$. (b) Selection of the capacitance C. (c) Output frequency limits for different sampling frequencies of the modulating signals.

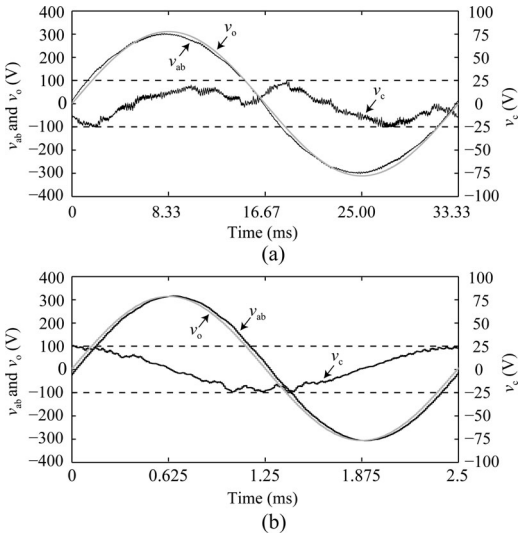

Fig. 11. Simulation results for minimum and maximum frequency limits of the designed ACPS. (a) ACPS voltage waveforms for $f_a = 30$ Hz. (b) ACPS voltage waveforms for $f_a = 400$ Hz.

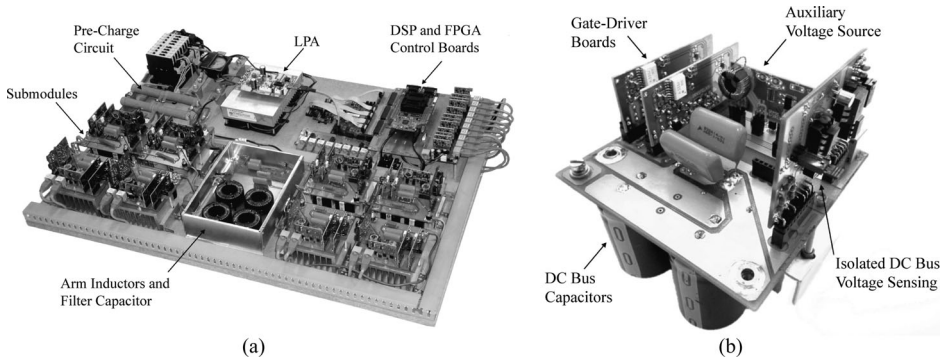

Fig. 12. Experimental setup. (a) ACPS. (b) Detail of a half-bridge SM.

After defining the output filter capacitance $C_{\rm ab}$, one can obtain the output voltage variation $\Delta v_{\rm ab,pert}$ when a load step $\Delta I_{o,\rm step}$ occurs by using the abacus presented in Fig. 10(a). In this example, the load step from no-load to 40% of the nominal load is used in Fig. 10(a) to obtain the voltage variation $\Delta v_{\rm ab,pert}$, which is defined as $\Delta v_{\rm ab,40\%}$ and is equal to 20 V.

In addition, Fig. 10(b) shows the abacus used to design the SM capacitors, using an outer voltage control loop bandwidth equal to 6 Hz. In this design, the $\Delta v_{\rm ab,ctrl}$ must be lower than $\Delta v_{\rm ab,pert}$. With this, a minimum SM capacitance equal to $C =$ 0.94 mF should be used, considering the critical voltage variation $\Delta v_{\rm ab,ctrl} = \Delta v_{\rm ab,pert} = \Delta v_{\rm ab,40\%}$, as shown in Fig. 10(b). This capacitance is the minimum value that guarantees the condition $\Delta v_{\rm ab,ctrl} < \Delta v_{\rm ab,pert}$.

It is important to note that voltage oscillation across the SM capacitors become significant when a low frequency is synthesized [29], limiting the minimum output frequency of the ACPS. On the other hand, if a high frequency reference should be synthesized by the ACPS, the phase displacement of the output filter and the phase lag of the modulation strategy become significant. To analyze these effects, the minimum dc voltage of the correction amplifier $V_{\rm dc2,min}$ is obtained for different output frequencies of the ACPS, as shown in Fig. 10(c). In this design example, the minimum and maximum output frequencies of the ACPS are 30 and 400 Hz, when the sampling frequency of the modulating signals $f_{\rm sp,ref}$ is twice the switching frequency f_s. However, if the sampling frequency of the modulating signals $f_{\rm sp,ref}$, the SM capacitances and/or the dc voltage level of correction amplifier are increased, the bandwidth of the ACPS can also be increased.

In addition, to demonstrate the behavior of the ACPS with minimum and maximum reference frequencies, simulation results are presented in these frequencies. Fig. 11(a) shows the voltage waveforms synthesized by the main amplifier $(v_{\rm ab})$ and correction amplifier (v_c), as well as the ACPS output voltage (v_o) for minimum reference frequency. Fig. 11(b) presents the same waveforms for the maximum reference frequency. These simulation results demonstrate that the LPA is operating close to the clamp condition, i.e., near to the designed dc bus voltage $V_{\rm dc2}$ (25 V).

V. Experimental Results

Some experimental results are presented in this section to verify the performance of the proposed topology. Pictures of the experimental setup are shown in Fig. 12 and Table I summarizes its main parameters. The main amplifier is controlled by a DSP TMS320F28335 (Texas Instruments), which transmits the control actions to the FPGA Spartan 6E (Xilinx). The FPGA implements the modified PS modulation to select the SMs accordingly with their dc bus voltage level. The correction amplifier used is the commercial MP111A amplifier from Apex. The output voltage total harmonic distortion (THD) and efficiency results were obtained with the digital power meter Yokogawa WT1600.

First, the nine level virtual multilevel waveform ($v_{\rm ref,rms} =$ 220 V at 60 Hz) synthesized by the MMC is shown in Fig. 13(a), which is computed from (1). On the other hand, Fig. 13(b) shows the performance of the MMC control system under a load step change from 0 to 1 p.u. (P_o from 0 to 1 kW). One can observe that the SMs dc bus voltages remain regulated even under this large disturbance.

The MMC output voltage, the correction amplifier voltage, the ACPS output voltage and current waveforms for a sinusoidal reference signal ($v_{\rm ref,rms} = 220$ V at 60 Hz) and resistive load ($P_o = 1$ kW) are shown in Fig. 14(a). As can be seen, the output voltage waveform presents a high quality, with THD equal to 0.25%.

It must be remembered that dynamic response of the whole system is defined by the correction amplifier, which also compensates the ripple produced in steady-state condition by the main amplifier as well as in transients due to a suitable amplitude for $V_{\rm dc2}$ (designed for a load step equal to 40%). The use of a small $V_{\rm dc2}$ allows reducing the conduction losses of LPA, which makes the ACPS efficiency higher. To validate the ACPS design, Fig. 14(b) shows the dynamic behavior of the system under a load step change from 0 to 0.4 p.u. (P_o from 0 to 405 W). As shown in Fig. 14(b), the load step change does not affect directly the output voltage of ACPS, which maintains a high fidelity.

Fig. 14(c) shows the ACPS output voltage transient under a load step from 0 to 1 kW, in order to shown the behavior

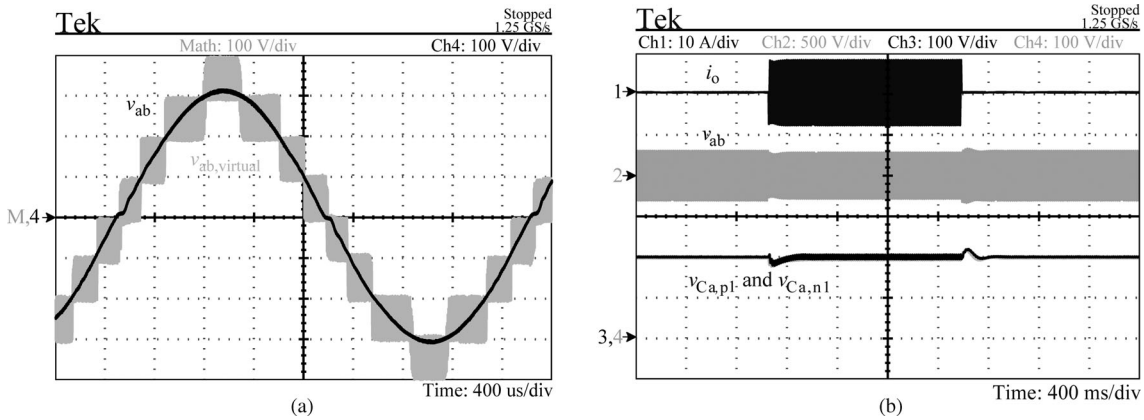

Fig. 13. Experimental waveforms for a sinusoidal waveform ($v_{\mathrm{ref,rms}} = 220$ V at 60 Hz). (a) Main amplifier output voltage $v_{\mathrm{ab}}(t)$ and virtual voltage $v_{\mathrm{ab,virtual}}(t)$ obtained through (1). (b) MMC waveforms under resistive load step from 0 to 1 kW.

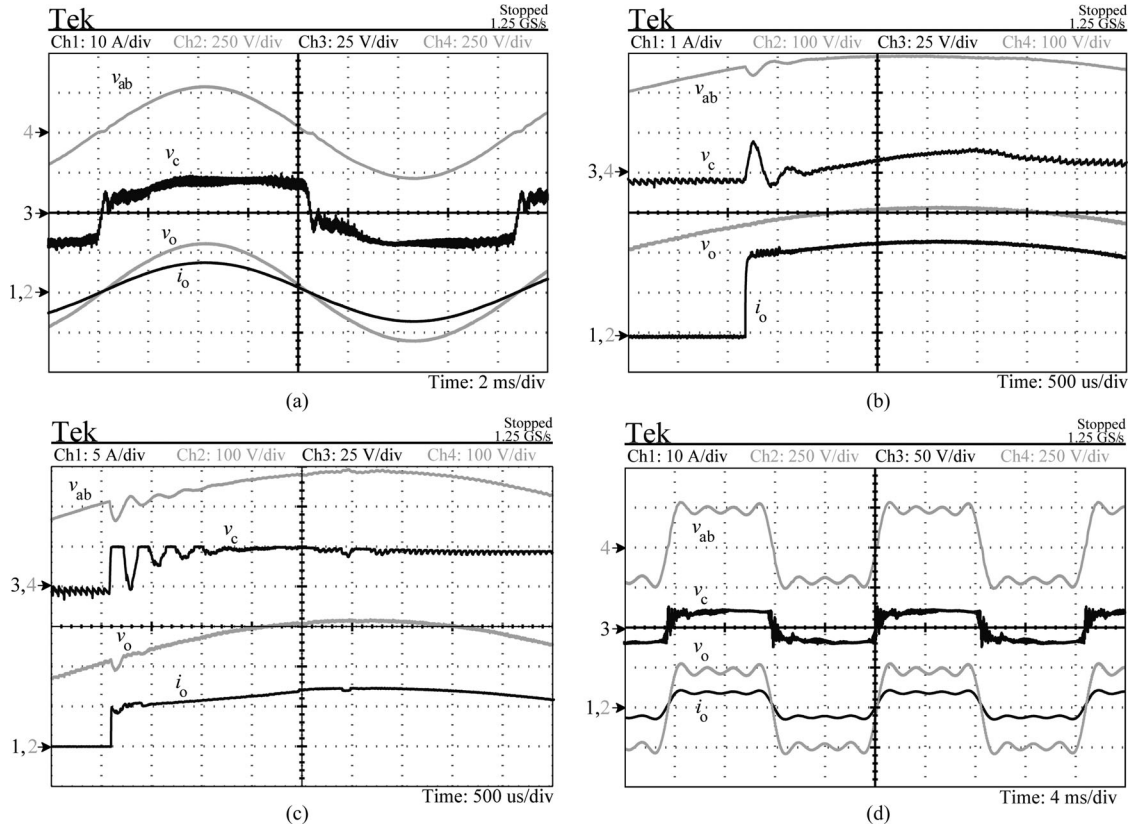

Fig. 14. Experimental waveforms for (a) a sinusoidal waveform ($v_{\mathrm{ref,rms}} = 220$ V at 60 Hz). Output voltages with a load step from (b) 0 to 405 W (FP = 1) and (c) 0 to 1 kW (FP = 1). (d) Arbitrary waveform results ($v_{\mathrm{ref,rms}} = \{220, 220/3, 220/5, 220/7\}$ V at $\{60, 180, 300, 420\}$ Hz) with nominal load.

when the load step change is higher than the load step used in V_{dc2} design (40%). In this case, LPA saturates in the transient because the load step applied (100%) causes an undershoot greater than the designed V_{dc2} (25 V), distorting the ACPS output voltage waveform. Moreover, experimental waveform components $v_{\mathrm{ref,rms}} = \{220, 220/3, 220/5, 220/7\}$ V at $\{60, 180, 300, 420\}$ Hz are shown in Fig. 14(d) and demonstrate the good waveform quality of the output voltage.

The whole system efficiency (taking into account the main and correction amplifiers) can be seen in Fig. 15(a) for the entire load power range and with resistive load. The proposed HPA achieved a maximum efficiency of 92.5% at nominal resistive load. Basically, the efficiency improvement can be attributed to the absence of an additional power stage to implement the isolated voltage sources required in the conventional cascaded multilevel converter [6], [7].

The THD of the voltage waveforms synthesized by the MMC ($\mathrm{v_{ab}}$) and by the entire ACPS ($\mathrm{v_o}$) for the entire load range can be seen in Fig. 15(b). It is possible to note that the THD of the ACPS output voltage (around 0.25%) is not affected by the distortion of the main amplifier, which increases for higher power levels.

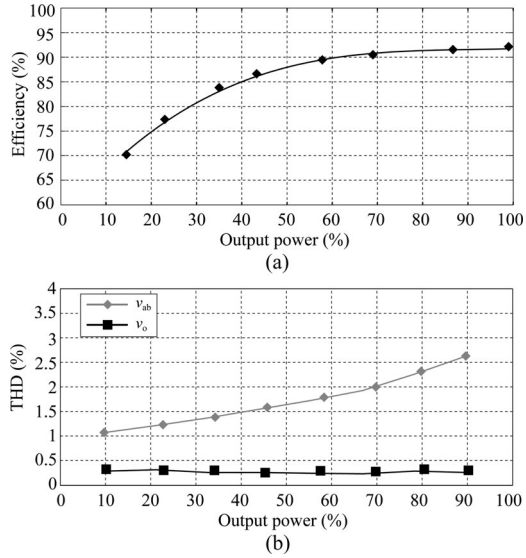

Fig. 15. Experimental results for a sinusoidal waveform reference ($v_{\mathrm{ref,rms}} = 220$ V at 60 Hz) and resistive load. (a) Efficiency. (b) THD of the ACPS output voltage.

VI. Conclusion

This paper proposed a hybrid topology for ACPS application composed of an MMC, operating as main amplifier, and an LPA, operating as correction amplifier, associated in series. By combining these different technologies it is possible to achieve modularity, high fidelity, high bandwidth (due to the use of an LPA as correction amplifier and the MMC as main amplifier) as well as high efficiency.

This topology uses a single dc power source to supply the MMC dc bus voltage without the need of transformers in the input power supply, but increases the complexity of the control system when compared to other topologies. Results included in this paper demonstrate that the proposed ACPS has good steady-state and transient performances, which assure high efficiency as well as satisfactory output voltage distortion (THD). Therefore, authors believe that this topology can be a candidate for high-performance ACPS applications.

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