Control of Parallel-Connected Modular Multilevel Converters

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***Abstract*—The modular multilevel converter (MMC) is an emerging and highly attractive multilevel converter topology for high-voltage and high-power applications. This paper proposes the control method of parallel-connected modular multilevel converters (parallel-MMCs), which assumes that the multiple MMCs are directly connected at both ac and dc sides to effectively enhance the power rating as expected. Two key problems were first solved for the parallel-MMCs under the normal operation conditions: voltage balancing of submodules and mitigation of circulating currents, where the novel transformed third-order harmonic resonant controller in the synchronous reference frame was employed to mitigate the dominant second-order and fourth-order circulating currents and a sixth-order harmonic resonant controller is used to attenuate the zero-sequence sixth-order circulating current existed in all phase currents per MMC. Considering the high risk of switches fault in the parallel-MMCs, the fault-tolerant operation schemes were then proposed in this paper to address the major concerns of open-circuit and short-circuit switch fault in a submodule, respectively. Carefully controlling the healthy submodules and the corresponding phase arms, the parallel-MMCs can successfully maintain their balanced capacitor voltages and mitigate the circulating currents with the qualified output waveform obtained. In addition, the parallel configuration of MMCs provides the unique solution for the short-circuit switch fault operation which was seldom discussed in the published literature works with respect to the MMC fault-tolerant operation schemes. MATLAB simulations and the constructed experimental prototype have verified the performance of the proposed control strategy.**

***Index Terms*—Circulating current, fault-tolerant operation, modular multilevel converter (MMC), parallel operation, pulse width modulation (PWM) compensation.**

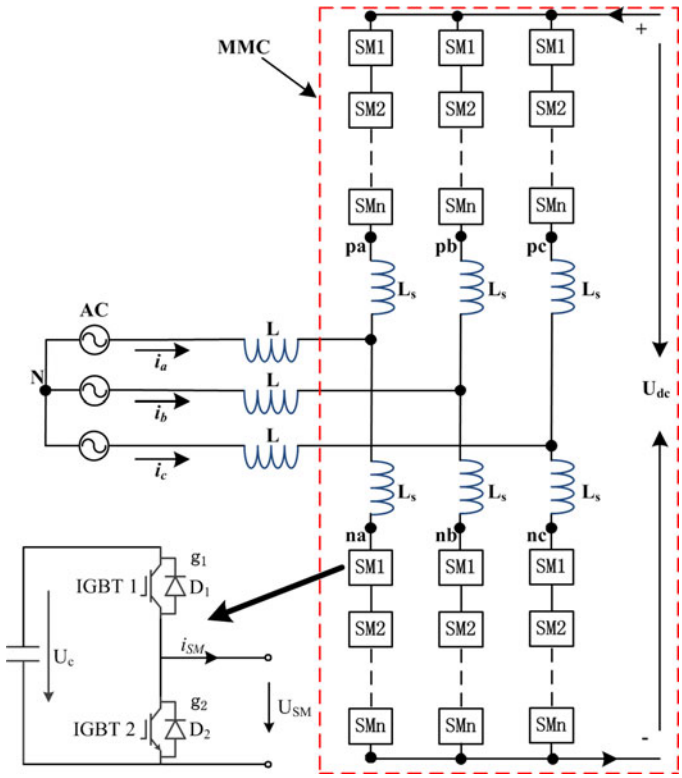

Fig. 1. Topology of the MMC.

I. Introduction

THE modular multilevel converter (MMC), which has been originally presented in [1] and [2], is suitable for the applications of high-voltage dc (HVDC) power transmission [3]–[5], adjustable speed motor drives [6], reactive power compensation [7], etc., mainly due to its inherent advantages of the modular structure and the low output voltage/current harmonics. Inside the MMC, every half-bridge converter is considered as a submodule (SM) as shown in Fig. 1, which can be simply cascaded to increase the dc-link voltage to a desired value. However, as the power increases or in other words when the MMC has to handle the high current, a single MMC is increasingly viewed as inappropriate, restricted mainly by the present semiconductor manufacturing technology without any immediate solution. One intuitive solution is to assume the compact integrated parallel-connected semiconductor switches in each SM, which however need a complicated gate driver to guarantee the simultaneous turning ON/OFF of parallel switches. Besides, assuming a single module with more than two switches connected in parallel would be impractical since the uneven loss distribution, which cannot be simply solved by the gate driver [8], would cause operational failure especially under the high-power high-current application conditions. Otherwise, an overdesigned heat dissipation system should be employed, which unfortunately will increase the system cost significantly. Another solution is to assume the parallel-connected setups to equally divide the

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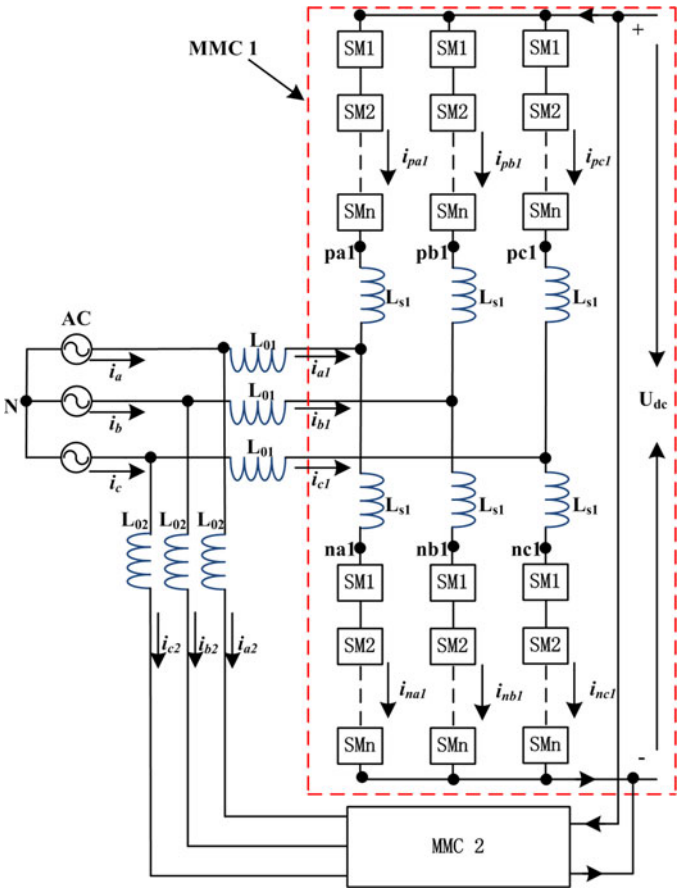

Fig. 2. Topology of the parallel-MMCs.

processed current into each setup, where the dc-link and the ac output terminals are directly connected together. The latter has been widely implemented in two-level converters [9]–[11]. Assuming that the parallel-connected MMCs (parallel-MMCs) will not only effectively increase the power rating as normally expected, but also significantly enhance the operational reliability by both reducing the thermal design burden and providing the unique solutions for semiconductor fault-tolerant operation. However, the parallel configuration of the MMC has been less reported.

In order to successfully implement the parallel-MMCs, two keys issues should be carefully addressed. One is the mitigation of internal and external circulating currents introduced in each phase and between the parallel-MMCs, respectively. Another is the switch fault-tolerant operation scheme without using the expensive redundant hardware to enhance the operational reliability, which is deemed as necessary in a complex multilevel power conversion system. Putting two MMCs in the parallel operation as shown in Fig. 2 would face the situation of cross coupling between the parallel-MMCs because when two MMCs are connected to the same dc bus and ac source/load, the extra zero-sequence circulating current (ZSCC) will result in the unexpected current distortion and the unbalanced load sharing, which would consequently result in the operational failure. Traditionally, in order to avoid this problem, transformers are used in an ac source/load side to isolate the direct current flow. However, the transformer is costly and bulky. As reported in [12]–[15], the parallel-connected converter can assume a specific control method to attenuate the ZSCC. However, when this method is assumed in the parallel-MMCs, both MMCs should first maintain their dc capacitor voltages of all SMs to be equal. When the voltages of all SMs are balanced, the dc-link voltage can be treated as a constant value when assuming a proper modulation method, thus the parallel-MMCs can be simplified as the two-level converters to attenuate the external ZSCC. Besides, the internal circulating currents should be minimized to reduce the losses. Many papers have reported the internal circulating current control methods [16]–[21], which in principle, control the second-order harmonic current flowing through the phase arms or in addition control the higher order fourth-, sixth-, and eighth-harmonic currents as the added control targets to smooth the internal circulating current, where the well-known resonant controllers are assumed to attenuate each order harmonics. Zhang *et al.* [22] assumed the repetitive controller to attenuate the circulating current. In order to reduce the calculation burden, this paper proposes a transformed third-order harmonic resonant controller in the synchronous reference frame to attenuate both dominant second- and fourth-order circulating harmonics per phase and additionally assumes a generalized sixth-order resonant controller to control the zero-sequence sixth-order circulating harmonic current in all phases per MMC.

The high risk of semiconductor switching failure induced by the open-circuit or short-circuit fault in parallel-MMCs cannot be ignored, whose most direct solution is to install a redundant phase-leg connected to the output terminals of normal phase-legs using the triacs the same as that assumed in the low-level power conversion system. Such hardware redundant configuration is expensive and seldom adopted in a high-voltage multilevel converter. The alternative solutions by adjusting the redundant pulse width modulation (PWM) signals in multilevel converters were presented in literature works to compensate the output performance [23]–[26]. The unique configuration of the MMC, however, is not suitable for the onefold PWM compensation scheme under the switch fault-tolerant operation conditions since the dc capacitor in a failure SM has to be inserted in the arm current flowing loop in most of the switching failure cases resulting in the dangerous overvoltage operation. Therefore, before assuming the PWM compensation scheme, the faulty SM should be bypassed first by using an additional bypass switch connected between the output terminals per SM as suggested in [27]. Using the bypass switch can only effectively solve the switch open-circuit failure problem, leaving the case of upper semiconductors (IGBT1 or D1 in Fig. 1) short-circuit failure per SM unsolved. But thanks to the parallel configuration, the parallel-MMCs can ride through all open-circuit and short-circuit semiconductor failure operation conditions using the proposed PWM compensation scheme and the revised control method in this paper without any additional assisted hardware; meanwhile, the proposed control scheme can effectively attenuate all circulating currents as well without sacrificing the output performance.

The rest of this paper is organized as follow. In Section II, the circuit configuration of the proposed parallel-MMCs is briefly

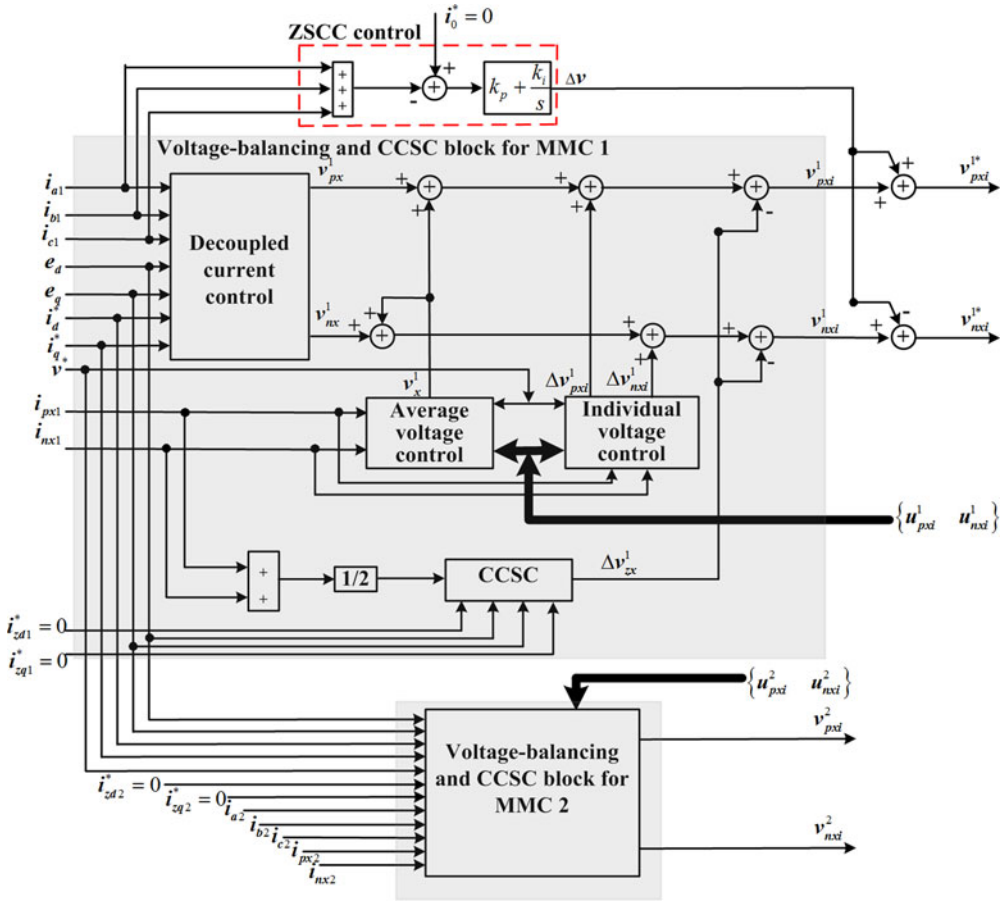

Fig. 3. General illustration of the control method of parallel-MMCs.

introduced and a control method is presented to analyze how to maintain the voltage balancing of all SM in both MMCs. In Section III, a control strategy is presented to attenuate the internal circulating currents using the proposed reduced-order resonant controllers. In Section IV, the control method to attenuate the external circulating current is presented. In Section V, the PWM compensation strategy and the corresponding control method are addressed to ride through the semiconductor failure operation conditions. Finally, MATLAB simulations and the constructed experimental prototype verified the performance of the proposed parallel-MMCs.

II. Illustration of the Parallel-MMC and its Voltage Balancing Control Method

Fig. 2 shows the circuit topology of the presented parallel-connected MMCs. The configuration of both MMCs is identical, where each MMC consists of six converter arms, which are constructed by a cascaded connection of SMs with a buffer inductor connected in series. As shown in Fig. 1, a half-bridge converter and a dc capacitor constitute the SM, where the terminal between two switches (IGBT1 and IGBT2) and the negative dc-rail terminal will connect to the adjacent SMs to form the aforementioned cascaded connection of single converter arm. And one phase leg consists of two arms, which are named as the positive arm and the negative arm, respectively. The buffer inductors L_s limit the circulating currents among six phase-legs in the parallel-MMCs.

The general control diagram of parallel-MMCs for grid-tied applications is illustrated in Fig. 3, where the general control function is realized by the voltage-balancing control blocks and circulating current suppression control (CCSC) blocks for MMC 1 and MMC 2 and the external ZSCC control block. The decoupled current control block is assumed to generate the fundamental control reference in the grid-tied applications, which may vary depending on the application cases. A general three-phase PLL is assumed to obtain the phase angle, which is not drawn in Fig. 3. In what follows, we will illustrate the capacitors voltage balancing control method in detail, whose control principle is suitable for the parallel-MMCs operated under both the normal operation condition and the switch fault-tolerant operation conditions.

In general, the voltage-balancing control method of the MMC can be divided into the following two specific control blocks [28]–[31]:

1) individual voltage control;
2) average voltage control.

A. Individual Voltage Control

Fig. 4(a) shows the control diagram of individual voltage control per SM, where u^j_{pxi} and u^j_{nxi} $(i = 1, 2, \ldots n, x = a, b,$

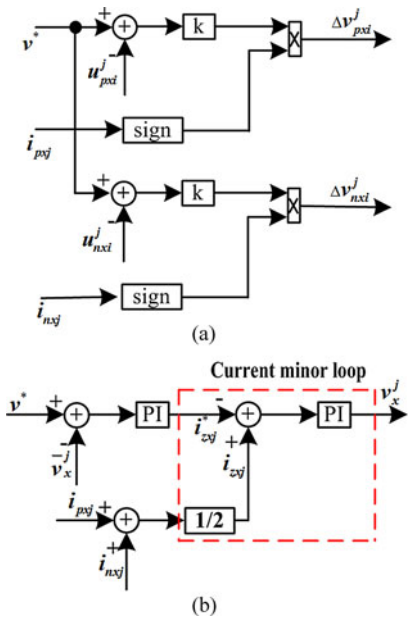

Fig. 4. Block diagrams of (a) individual voltage control and (b) average voltage control.

or $c, j = 1$ or 2 refers to the first and second MMC, respectively, p and n represent the upper and lower arms, respectively) are the measured SM dc voltages. The error between the dc voltage reference v^* and the measured dc voltage will be amplified by a proportional gain k. Besides, the arm current polarity of i_{pxj} and i_{nxj} will be added to the control signal to properly fine tune the switching states. In detail, (1) shows the tuning direction according to the arm current

$$\begin{cases} \Delta v_{pxi}^{j} = \begin{cases} k(v^* - u_{pxi}^{j}) & (i_{pxj} \geq 0) \\ -k(v^* - u_{pxi}^{j}) & (i_{pxj} \leq 0) \end{cases} \\ \Delta v_{nxi}^{j} = \begin{cases} k(v^* - u_{nxi}^{j}) & (i_{nxj} \geq 0) \\ -k(v^* - u_{nxi}^{j}) & (i_{nxj} \leq 0) \end{cases} \end{cases}. \quad (1)$$

B. Average Voltage Control

The principle of average voltage control is to control the averaged phase voltage by regulating the circulating current, whose control diagram is illustrated in Fig. 4(b), where $\bar{v}_x^j$ and i_{zxj} are the averaged dc voltage and circulating current per phase calculated as follows:

$$\begin{cases} \bar{v}_x^j = \dfrac{1}{2n}\left(\displaystyle\sum_{i=1}^{n} u_{pxi}^{j} + \sum_{i=1}^{n} u_{nxi}^{j}\right) \\ i_{zxd} = \dfrac{1}{2}(i_{pxj} + i_{nxj}) \end{cases}. \quad (2)$$

After a fine-tuned PI controller, the error between the averaged dc voltage and the dc voltage reference will be amplified as the dc-loop current reference between the positive arm and the negative arm per phase. Doing so, the measured circulating current per phase can follow this generated reference to tune the averaged dc voltage $\bar{v}_x^j$ through the second PI controller. For example, when $v^* \geq \bar{v}_x^j$, i_{zxj}^* will increase. Then, the function of the current minor control loop would force the actual circulating current i_{zxj} to closely follow i_{zxj}^*. As a result, the feedback control of i_{zxj} enables $\bar{v}_x^j$ to follow its reference v^*

III. Internal CCSC

As a result of the SM capacitor voltage variation, the three parallel connected phase legs as shown in Fig. 1 may have different summed voltages. Consequently, this leads to the circulating currents among the three-phase units. The circulating currents will flow through the six-phase arms and distort the sinusoidal arm currents introducing the additional converter losses; therefore, the circulating current will threaten the safe operation of the power devices and capacitors. In addition, this current will influence the SM voltages and the output voltages [28] as illustrated in Section II. The internal circulating currents analysis has been reported in the technical literature works. The authors in [16] and [17] analyzed the mechanism of three-phase circulating currents in the MMC and discussed the relationship between the amplitudes of the circulating currents and the parameters of the arm inductors. Although increasing the arm inductance can reduce the circulating currents, it is not able to completely eliminate the circulating currents and it is not practical due to the large inductor size and the high cost. An effective control method to eliminate the circulating currents was proposed in [16] and [17]. However, this method just suppressed the second-order harmonic current that appeared in the circulating currents. According to the circulating currents analysis in [32], in addition to the low-frequency component, the dc and high-frequency components also appear in the circulating currents. It has also been pointed out that the circulating currents only contain the even-order harmonics without the odd order harmonics. Especially, the second-, fourth-, and sixth-order harmonics dominate the circulating currents. She *et al*. [21] employed many resonant controllers to suppress the second-, fourth-, and sixth-order circulating harmonics of the three-phase MMC and Zhang *et al.* [22] assumed the repetitive controller to attenuate the circulating current harmonics per phase. This paper proposes a novel CCSC method to suppress the three-phase second-, fourth-, and sixth-order circulating current harmonics by only using three resonant controllers with the precise circulating current harmonics tuning capability and the significant reduction of calculation burden as well.

For tuning multiple harmonics, although the resonant controllers placed in the stationary reference frame can be used, they would result in more terms for summation. Therefore, as an alternative, the resonant controllers in the synchronous reference frame would be more effective, since each represents two equivalent resonant terms in the stationary reference frame for compensating two harmonics simultaneously as stated in [33]. According to the circulating currents analysis in [32], the second-order current harmonic is a negative-sequence current, the fourth-order current harmonic is a positive-sequence current, and the sixth-order harmonic is a zero sequence current. Thus, the three-phase second- and fourth-order current

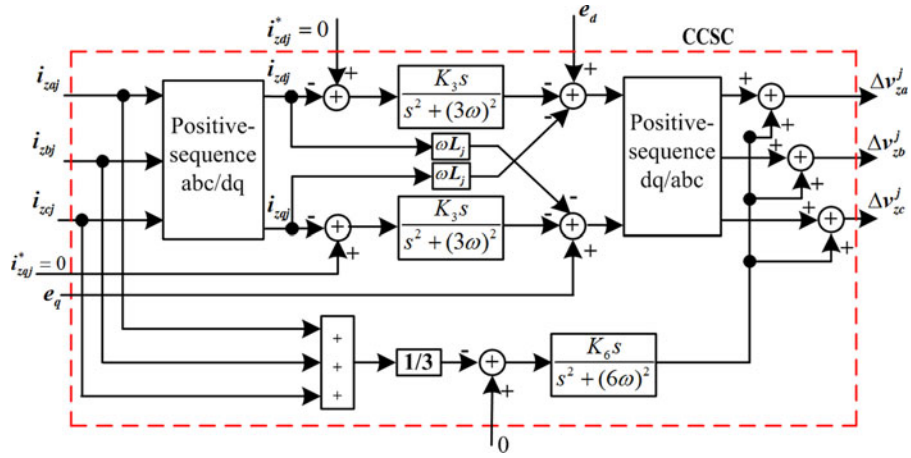

Fig. 5. Block diagram of internal CCSC.

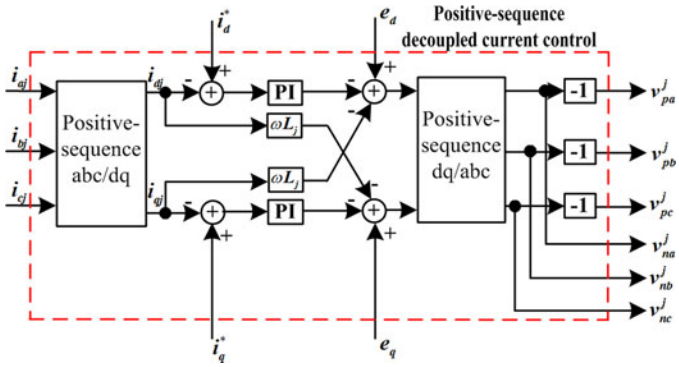

Fig. 6. Illustration of the positive-sequence decoupled current control block.

harmonics can be tuned simultaneously by only using two third-order resonant controllers to, respectively, tune the transformed *dq* components under the synchronous reference frame as shown in Fig. 5. In order to suppress the sixth-order zero-sequence current harmonic, an additional resonant controller is assumed to suppress the summed three-phase current in Fig. 5. The assumed resonant controllers can be, respectively, written as

$$\begin{cases} G(s) = \dfrac{K_3 s}{s^2 + (3\omega_0)^2} \\ G(s) = \dfrac{K_6 s}{s^2 + (6\omega_0)^2} \end{cases} \tag{3}$$

where K_3, K_6, and ω_0 represent the integral gains and the fundamental frequency, respectively.

The summed control signal per SM in the positive-arm and the negative-arm can be written as

$$\begin{cases} v_{pxi}^j = v_{px}^j + v_x^j + \Delta v_{pxi}^j - \Delta v_{zx}^j \\ v_{nxi}^j = v_{nx}^j + v_x^j + \Delta v_{nxi}^j - \Delta v_{zx}^j \end{cases} \tag{4}$$

where v_{px}^j and v_{nx}^j ($x = a, b$, or $c, j = 1$ or 2) are the primary control commands derived from the current control block in Fig. 3, whose detailed control diagram is drawn in Fig. 6, where the three-phase control signals v_{px}^j and v_{nx}^j will be assigned to control six arms per MMC to track the current reference.

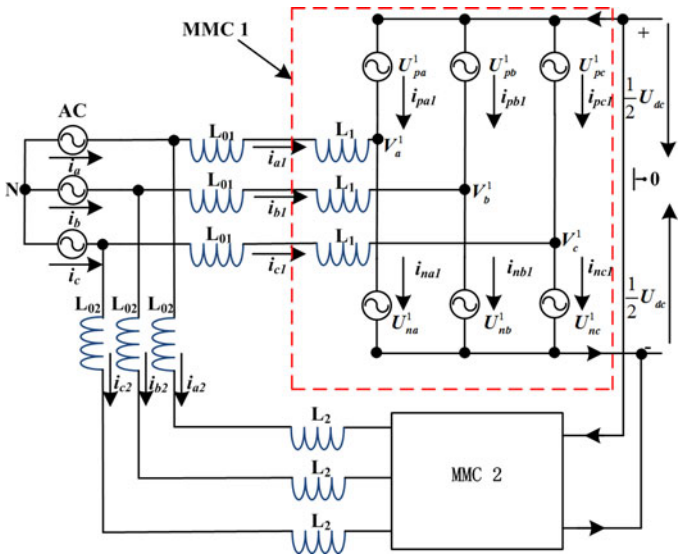

Fig. 7. Equivalent simplified circuit model of parallel-MMCs.

IV. Analysis and Control of External ZSCCs in Parallel-MMCs

The SM can be treated as a controlled voltage source when building the average model of parallel-MMCs. According to the analysis in [16], $px1$ and $nx1$ ($x = a, b$, or c) are the virtual equipotential points in Fig. 2. Therefore, both buffer inductors per phase can be treated as the parallel connected inductors in Fig. 7, where it is easy to obtain $L_1 = L_{S1}/2$, $L_2 = L_{S2}/2$. The sum of capacitor voltages in positive arm and negative arm per phase are equivalent to the controlled voltage U_{px}^j and U_{nx}^j ($x = a, b$, or c and $j = 1$ or 2)

$$\begin{cases} u_{px}^j = \displaystyle\sum_{i=1}^{n} S_{pxi}^j U_c \\ u_{nx}^j = \displaystyle\sum_{i=1}^{n} S_{nxi}^j U_c \end{cases} . \tag{5}$$

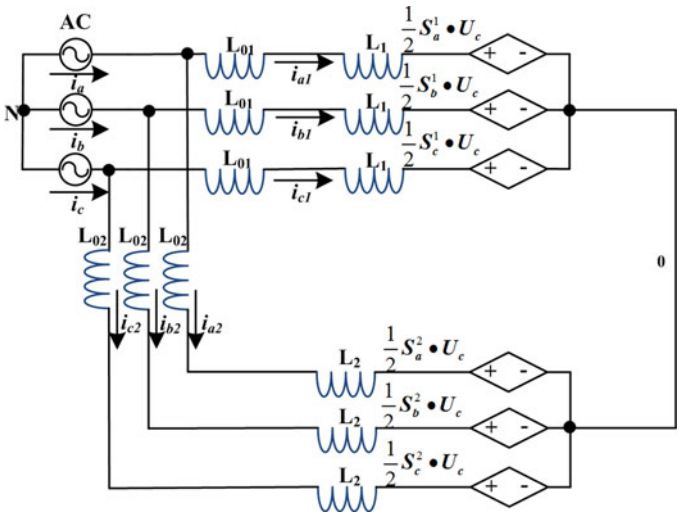

Fig. 8. Equivalent average model of parallel-MMCs.

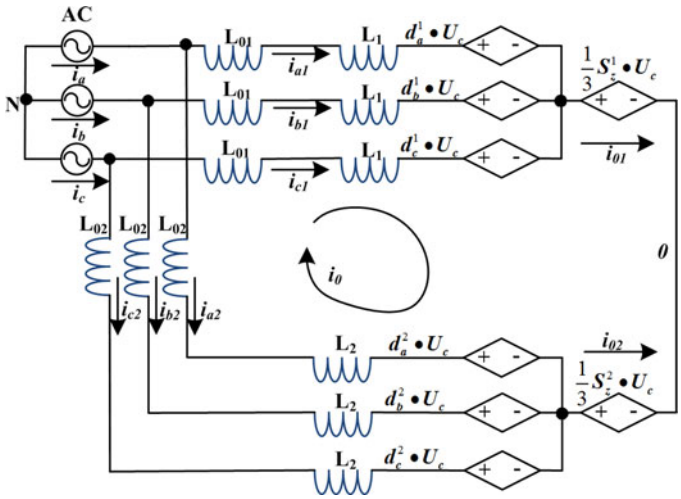

Fig. 9. Average model of parallel-MMCs with zero-sequence components added.

Assuming that the equivalent switching frequency is much larger than the output voltage fundamental frequency, the parallel-MMCs can be further equivalent to a controlled voltage source viewed from its ac side, therefore, the equivalent average model of parallel-MMCs can be drawn as Fig. 8.

The zero-sequence duty-cycle S_z^j can be defined as

$$S_z^j = \frac{1}{2}S_a^j + \frac{1}{2}S_b^j + \frac{1}{2}S_c^j \tag{6}$$

and $\frac{1}{2}S_a^j, \frac{1}{2}S_b^j, \frac{1}{2}S_c^j$ can be further expressed as

$$\begin{cases} \frac{1}{2}S_a^j = d_a^j + \frac{1}{3}S_z^j \\ \frac{1}{2}S_b^j = d_b^j + \frac{1}{3}S_z^j \\ \frac{1}{2}S_c^j = d_c^j + \frac{1}{3}S_z^j \end{cases} \tag{7}$$

where

$$d_a^j = \frac{1}{2}S_a^j - \frac{1}{3}S_z^j, d_a^j = \frac{1}{2}S_b^j - \frac{1}{3}S_z^j, d_c^j = \frac{1}{2}S_c^j - \frac{1}{3}S_z^j.$$

As a result, the average model of parallel-MMCs with the zero-sequence components added is drawn in Fig. 9, where the ZSCC flowing in MMC 1 and MMC 2 are denoted by i_{01} and i_{02}, respectively. Hence, the ZSCC i_0 can be defined as

$$\begin{aligned} i_0 &= i_{01} = i_{a1} + i_{b1} + i_{c1} = -i_{02} \\ &= -(i_{a2} + i_{b2} + i_{c2}). \end{aligned} \tag{8}$$

With the prerequisite of balanced SM voltages, the ZSCC i_0 can be calculated by summing the three-phase currents of a single MMC as expressed in (8). Therefore, it is reasonable to suppress the external ZSCC only in one MMC to achieve the full elimination of ZSCC between the parallel-MMCs as that reported for controlling the parallel-connected two-level converters. A simple PI controller is assumed to control the ZSCC to be zero as shown in Fig. 3, where the generated modulation signals will be added to v_{pxi}^1 and v_{nxi}^1 to produce the final modulation signals for MMC 1.

V. Fault-Tolerant Operation of Parallel-MMCs

In view of the high amount of power semiconductors in the parallel-MMCs, any failure can cause large downtime and tremendous losses for the consumers. Therefore, it is important to develop the fault-tolerant operation schemes to enhance the reliability. This paper proposes the novel PWM compensation schemes for the fault-tolerant operation of parallel-MMCs without using an additional backup hardware. Only single-switch fault in one SM is considered in this paper, whose failure conditions can be broadly classified as the open-circuit fault and short-circuit fault. Carefully analyzing the switching states per SM in Fig. 1, it is noted that the open-circuit fault of IGBT 1 and the short-circuit fault of IGBT 2 are identical for the fault-tolerant operation and similarly the short-circuit fault of IGBT 1 and the open-circuit fault of IGBT 2 are identical either in terms of their complementary switching sequence. Therefore, the fault-tolerant operation of parallel-MMCs only needs to consider two cases: open-circuit fault and short-circuit fault of IGBT 1.

A. PWM Compensation Schemes for the Open-Circuit Fault-Tolerant Operation of IGBT 1

Once the IGBT 1 suffers the open-circuit fault, the whole SM is recommended to only output state $\{0\}$ by keeping IGBT 2 ON in order to maintain the continuous arm current being equivalent to the bypass function of SMs. In this case, the corresponding phase arm will lose one voltage level. In order to reduce the circulating current induced by the absence of one SM, it is suggested that the corresponding opposite phase arm downgrade its switching level from $N+1$ to N either. And the healthy SM capacitor voltages in the faulty phase-leg should be slightly increased to $NU_c/(N-1)$ so that the summed phase voltage is still equal to NU_c the same as that of other two healthy

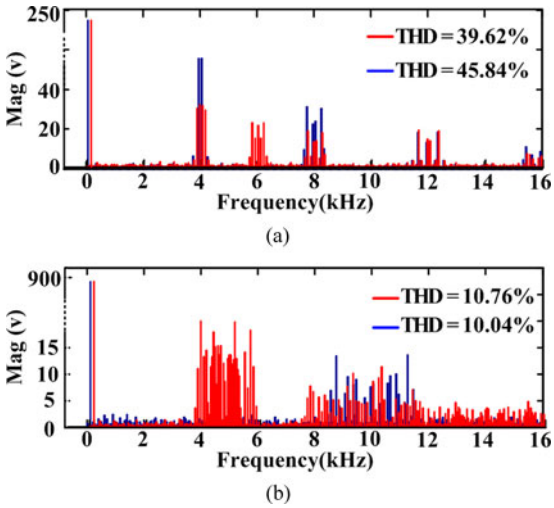

Fig. 10. Harmonics spectrum and THD of line-voltages between phase A and B for the cases of (a) two SMs per arm in phase A and three SMs per arm in phase B (red) and two SMs per arm in phase A and B (blue) with switching frequency of 2000 Hz and (b) nine SMs per arm in phase A and ten SMs per arm in phase B (red) and nine SMs per arm in phase A and B (blue) with switching frequency of 500 Hz.

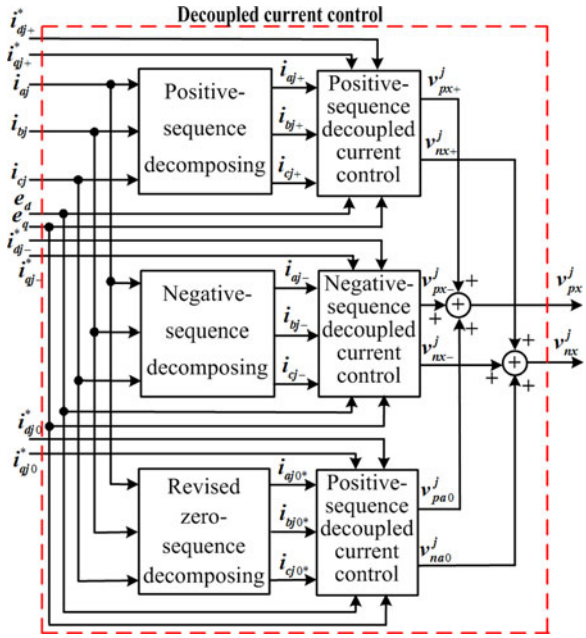

Fig. 11. Illustration of positive-, negative-, and zero-sequence currents decoupled control block.

phase-legs. Doing so, the revised switching states in the faulty phase-leg would not induce any additional circulating current in theory. The switching level reduction in the faulty phase-leg can increase the output harmonics induced by the unbalanced output line voltages. Reducing the switching level of other five healthy phase-legs with or without increasing their SM capacitor voltages can keep the balanced output line voltage as an alternative. Fig. 10 compares the line voltage THD and harmonic spectrum of the aforementioned two PWM compensation methods. It is revealed that the output quality of the former method for only reducing the switching level of faulty phase-leg could have a better output quality compared to the latter method when the number of SM is less. Comparatively, when the number of SM increases, the latter method could demonstrate the better output quality as shown in Fig. 10(b).

Besides, the aforementioned two fault-tolerant operation schemes could demonstrate the different merits and demerits for the different applications. For the cases with the invariant dc-link voltage, e.g., the rear-end inversion part of HVDC, the fault-tolerant operation scheme with the switching level downgrade of only faulty leg is superior since it would minimize the dc-link inrush current during the transit process. For the cases, where the dc-link voltage is allowed to reduce accordingly, e.g., the reactive power compensation system with the redundant SMs, it is recommended to downgrade the switching level of all six phase-legs in parallel-MMCs without inducing the high inrush current and meanwhile keeping the superior output performance.

B. Revised Control Scheme for the Short-Circuit Fault-Tolerant Operation of IGBT 1

Unlike the H-bridge SM, the half-bridge SM does not have the redundant switching states to bypass the faulty switch. When the IGBT 1 suffers the short-circuit failure, the corresponding SM must keep its output state $\{1\}$ unchanged, which would unavoidably insert the dc capacitor into the load current flowing loop resulting in the damageable overvoltage breakdown. Therefore, when such short-circuit failure happens, the corresponding whole phase arm should be shut down to protect the equipment. Traditionally, the single three-phase MMC cannot continue its normal operation since one phase-leg is out of operation. But fortunately, the parallel-MMCs provide the redundant phase-leg to ride-through the short-circuit failure condition with the careful consideration of tradeoff between the current rating and the output power.

As a consequence, the parallel-MMCs will continue its operation by only using five phase-legs. In order to maintain the symmetrical three-phase output currents, the corresponding phase-leg in the healthy MMC can generate double output current with the output current of other four legs unchanged to produce the same output power as that before the switch failure. For example, assuming that the total three-phase output currents are i_a, i_b, and i_c, respectively, and an SM of phase A in MMC 1 suffers the IGBT 1 short-circuit failure condition, the phase A in MMC 2 would produce the output current of i_a, while the other four healthy phases would generate $\frac{1}{2}i_b, \frac{1}{2}i_c, \frac{1}{2}i_b$, and $\frac{1}{2}i_c$, respectively, as usual to make sure that the total three-phase currents are symmetrical as expected. In this case, the desired output currents per MMC are unbalanced. Therefore, the traditional decoupled positive-sequence current control method for the grid-tied applications illustrated in Fig. 6 cannot be solely employed to control the output currents since the unbalanced three-phase currents per MMC can be decomposed into the positive-sequence, negative-sequence, and zero-sequence components. A combined closed-loop current controller is shown in Fig. 11, where the positive-sequence, negative-sequence,

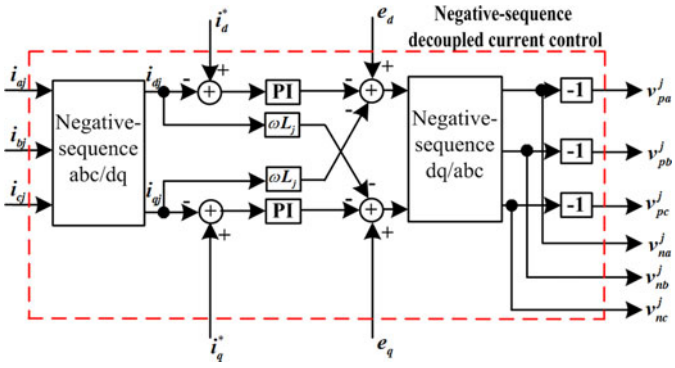

Fig. 12. Illustration of negative-sequence decoupled current control block.

and zero-sequence components i_{xj+}, i_{xj-}, and i_{xj0} ($x = a, b$ or $c, j = 1$ or 2) are derived using (9). In order to use the positive-sequence decoupled current control method to control the desired zero-sequence output current, (10) further revises the zero-sequence components. Doing so, the zero-sequence current can be controlled using the similar positive-sequence decoupled current control block as shown in Fig. 11. Besides, the negative-sequence current can be controlled using the negative-sequence decoupled current control block as shown in Fig. 12

$$\begin{cases} \begin{bmatrix} i_{aj+} \\ i_{bj+} \\ i_{cj+} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & a & a^2 \\ a^2 & 1 & a \\ a & a^2 & 1 \end{bmatrix} \begin{bmatrix} i_{aj} \\ i_{bj} \\ i_{cj} \end{bmatrix} \\ \begin{bmatrix} i_{aj-} \\ i_{bj-} \\ i_{cj-} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & a^2 & a \\ a & 1 & a^2 \\ a^2 & a & 1 \end{bmatrix} \begin{bmatrix} i_{aj} \\ i_{bj} \\ i_{cj} \end{bmatrix} \\ \begin{bmatrix} i_{aj0} \\ i_{bj0} \\ i_{cj0} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_{aj} \\ i_{bj} \\ i_{cj} \end{bmatrix} \\ a = e^{j2\pi/3} \end{cases} \tag{9}$$

$$\begin{aligned} \begin{bmatrix} i_{aj0^*} \\ i_{bj0^*} \\ i_{cj0^*} \end{bmatrix} &= \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ a^2 & a^2 & a^2 \\ a & a & a \end{bmatrix} \begin{bmatrix} i_{aj} \\ i_{bj} \\ i_{cj} \end{bmatrix} \\ &= \frac{1}{3} \left\{ \begin{bmatrix} 1 & 1 & 1 \\ -\frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} \\ -\frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} \end{bmatrix} \right. \\ &\quad \left. -j \begin{bmatrix} 0 & 0 & 0 \\ \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ -\frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \right\} \begin{bmatrix} i_{aj} \\ i_{bj} \\ i_{cj} \end{bmatrix}. \end{aligned} \tag{10}$$

In addition to the above primary control for the fundamental components, the control method of internal circulating currents should be revised either since the three-phase circulating currents of both MMCs are now unbalanced resulting in the large low-frequency ripple in the transformed *dq* components in Fig. 5. The solution is to assume the remaining two-phase internal circulating currents in the faulty MMC to rebuild the three-phase circulating currents as inputs and similarly rebuild the three-phase circulating currents for the healthy MMC using the unchanged two-phase circulating currents by assuming the ac components of three-phase circulating currents being symmetrical in Fig. 5. Doing so, the well-tuned resonant controllers in the synchronous reference frame can still work well to suppress the internal circulating currents. It is noted that the external ZSCC control is not applicable here since the average models of parallel-MMCs derived in Figs. 8 and 9 are not applicable either due to the absence of one phase in parallel-MMCs. In principle, the revised control method for the IGBT 1 short-circuit fault-tolerant operation will only regulate five-phase currents by including the additional negative- and zero-sequence decoupled current controller, removing the external ZSCC controller, and leaving the internal circulating current control block almost unchanged.

C. Diagnostic Methods for the IGBT Faults and the Reconfigured Control Logic

Diagnostic methods for the IGBT faults have been presented in many published literature works. Park's vector approach as an effective fault diagnostic tool for voltage source inverter was first proposed in [34]. The localization of the faulty switch can also be identified by the analysis of the current space-vector trajectory diameter [35]. A novel fast-diagnostic method for open-circuit faults without sensors is proposed to improve the reliability of the power electronic system in [36]. Estima and Cardoso [37] present a new diagnostic method that allows the real-time detection and localization of single-power switch open-circuit faults in VSI-fed PWM motor drives. Besides, the fault detection methods in multilevel converters [38] include the frequency analysis method [39], [40], neural networks method [41], and load voltages and currents time behavior methods [42]–[44]. The fault detection interval may vary from few switching periods to few milliseconds as indicated in [44] and [45]. Regardless of the specific fault detection principle, the inherent current limit characteristics of the MMC can indeed help reduce the transient damage. The next step is to reconfigure the switching sequences and control function in order to minimize the performance degradation as illustrated in Section V-A and V-B. Since the gate driver can directly detect the IGBT short-circuit fault and clamp the switching commands of opposite IGBT in a half-bridge module, the reconfigured control function for IGBT 1 short-circuit fault could be immediately implemented upon the controller receiving the feedback fault signal. For another case, where IGBT 1 suffers the open-circuit fault, the complicated switching logic reconfiguration should be implemented as illustrated below.

For a practical MMC, multiple FPGAs are assumed for communication and switching signal generation. The internal communication usually assumes fibre-optical, whose

communication delay can be ignored. Since the switching signals are generated in separate FPGAs, the direct replacement of whole switching signals is not practical for the IGBT 1 open-circuit fault-tolerant operation. Therefore, an alternative method is to adjust the local switching sequences according to the identified faulty module location. Assuming the carrier phase-shifted modulation method [46] as an example, where the switching sequences per module is generated by the comparison between a specific triangular carrier and a modulation reference, each phase would equip with $2n$ triangular carriers. The $2n$ carriers can be labeled as C1, C2, C3,. . .,Cn for the n modules of upper arm and $C1^*, C2^*, C3^*, \ldots, Cn^*$ for the n modules of lower arm, respectively. The phase shift between adjacent carriers is $2\pi/n$ and the phase shift between Ci and C$i^*(i = 1, 2, 3 \ldots n)$ is π. Assuming that the initial phase angle of C1 is 0, the subsequent initial phase angles of Ci and Ci^* are $(i-1)2\pi/n$ and $\pi + (i-1)2\pi/n$, respectively. When IGBT 1 of SMm $(1 \le m \le n)$ suffers the open-circuit failure, both SMm and SMm^* in the same phase should be bypassed by keeping the corresponding IGBT 2 ON as analyzed in Section V-A. Therefore, the phase shifts of remaining $2(n-1)$ triangular carriers should be revised accordingly as illustrated in (11), where α_i represents the phase angle of Ci

$$\begin{cases} \alpha i = \begin{cases} \dfrac{(i-1)*2\pi}{n-1} (1 \le i < m) \\ \dfrac{(i-2)*2\pi}{n-1} (m < i \le n) \end{cases} \\ \alpha i^* = \begin{cases} \dfrac{(i-1)*2\pi + (n-1)\pi}{n-1} (1 \le i < m) \\ \dfrac{(i-2)*2\pi + (n-1)\pi}{n-1} (m < i \le n) \end{cases} \end{cases}. \quad (11)$$

In addition, the averaged dc voltage v_x^{-j} of the faulty phase should be recalculated as

$$v_x^{-j} = \frac{1}{2(n-1)} \left(\sum_{i=1}^{m-1} u_{pxi}^j + \sum_{i=m+1}^{n} u_{pxi}^j + \sum_{i=1}^{m-1} u_{nxi}^j + \sum_{i=m+1}^{n} u_{nxi}^j \right) \quad (1 \le m \le n). \quad (12)$$

The individual voltage reference v^* of the faulty phase should be replaced by $nU_c/(n-1)$ either. Doing so, the controller can easily reconfigure the switching logic after labeling all SMs to ensure the smooth transient process.

VI. Simulation Results

To verify the theoretical findings presented in this paper, the simulation model of parallel-MMCs with three SMs per phase arm was built in MATLAB/Simulink. The carrier phase-shifted modulation method [46] was assumed. To simulate the different power consumption among all SMs, an equivalent resistor was connected to the capacitor per SM in parallel with the value of 500, 700, and 800 Ω in the positive arm, and 400, 500, and 700 Ω in the negative arm, respectively. The circuit parameters are listed in Table I, where the output filter inductances are different. The d- and q-axis current references i_d^* and i_q^* in Fig. 6 are set to be 30 and 30 A, respectively, under both the normal and switch fault operation conditions.

TABLE I
Circuit Parameters

DC bus voltage	U_{dc}	600V
Sub-module capacitor voltage	U_C	200V
Sub-module capacitor	C	3300uf
Fundamental frequency	f	50Hz
Carrier frequency	f_C	5kHz
Output filter inductances	L_{01}	2mH
	L_{02}	5mH
Buffer inductances	L_{s1}	2mH
	L_{s2}	2mH
Output phase voltage (RMS)	U_s	110V

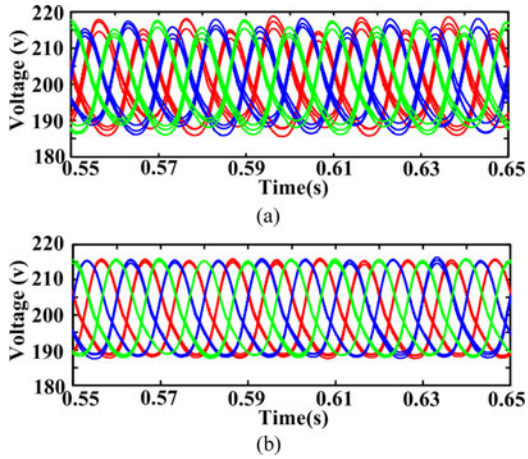

Fig. 13. Capacitor voltages of (a) MMC 1 and (b) MMC 2.

A. Simulation Results Under Normal Operation Conditions

To verify the voltage-balancing control method under the normal operation conditions, the simulated capacitor voltages of the positive arm and negative arm are shown in Fig. 13. It is obvious that the voltage balancing control method works well and all capacitor voltages are balanced around 200 V as expected. A little bit unbalanced voltage (around 3 V) will appear in the capacitors of MMC 1 since the external ZSCC control signal is added in the control loop of MMC 1. But, the small unbalanced voltage is still within the acceptable range.

Fig. 14 shows the simulated internal circulating currents and their spectrum in MMC 1 without and with the proposed CCSC method added under the normal operation conditions. It is noted that the internal circulating currents without using the proposed CCSC method contain the dominant low-frequency second-, fourth-, and sixth-order current harmonics as shown in Fig. 14(a) and (b). By using the proposed CCSC method, the low-frequency harmonics are significantly suppressed as shown in Fig. 14(c) and (d). It can also be seen that the positive-arm and negative-arm currents have become near sinusoidal by employing the proposed CCSC method as shown in Fig. 15.

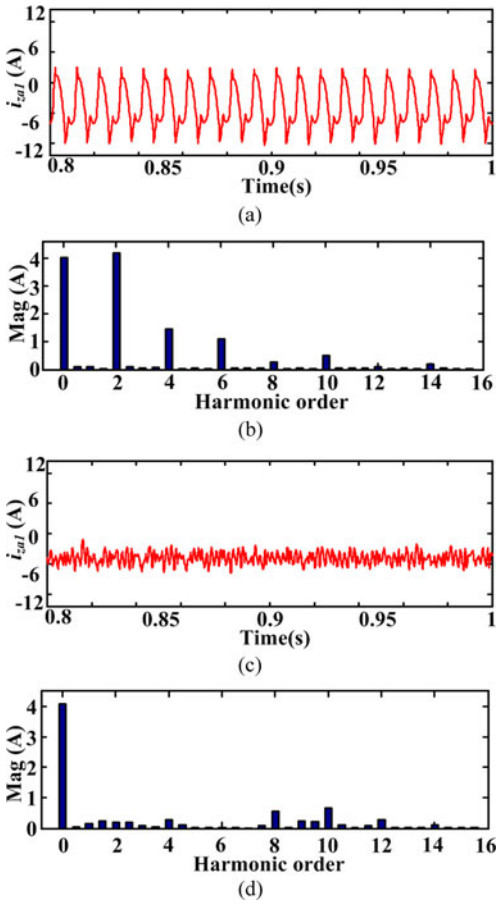

Fig. 14. Simulated internal circulating currents and their spectrums: (a) and (b) without, and (c) and (d) with the proposed CCSC method.

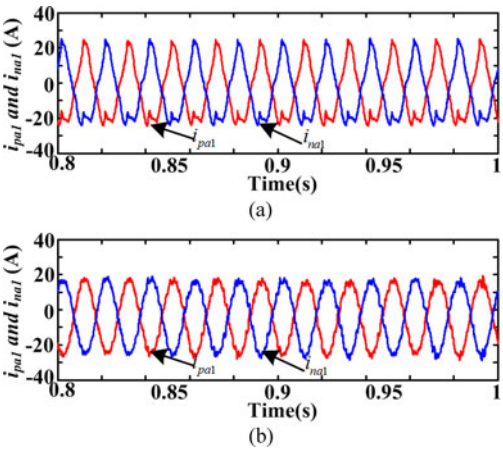

Fig. 15. Simulated waveforms of positive-arm and negative-arm currents of phase-A in MMC 1 (a) without and (b) with the proposed CCSC method.

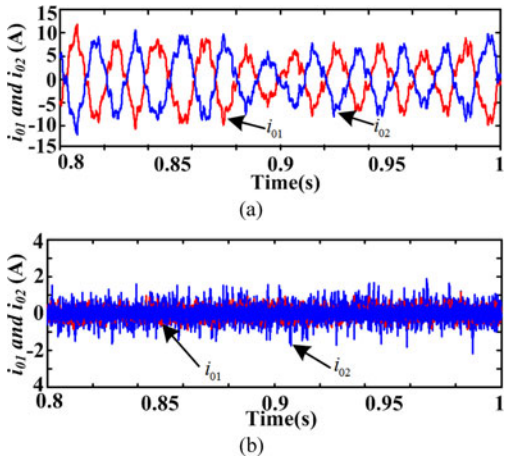

Fig. 16. Simulated external zero-sequence circulating currents (a) without and (b) with ZSCC control added.

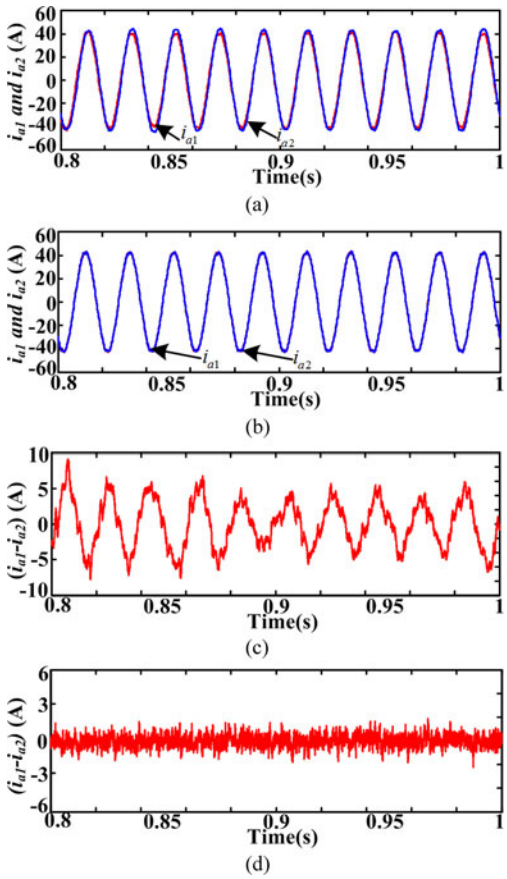

Fig. 17. Simulated phase currents i_{a1} and i_{a2}: (a) without and (b) with ZSCC control added and their difference under the conditions, (c) without and (d) with ZSCC control added.

In order to verify the performance of the ZSCC control method in the parallel-MMCs, Fig. 16(a) shows the simulated ZSCC without using the ZSCC control method, where the ZSCCs i_{01} and i_{02} are apparently large. In comparison, Fig. 16(b) shows the simulated results with ZSCC control added, where the ZSCCs are almost eliminated. In addition, Fig. 17 shows the phase A currents i_{a1} and i_{a2} of MMC1 and MMC2 and their difference under the operation conditions without and with the ZSCC control method added, respectively. Obviously, using the ZSCC control method can significantly reduce the phase current difference between MMC1 and MMC2.

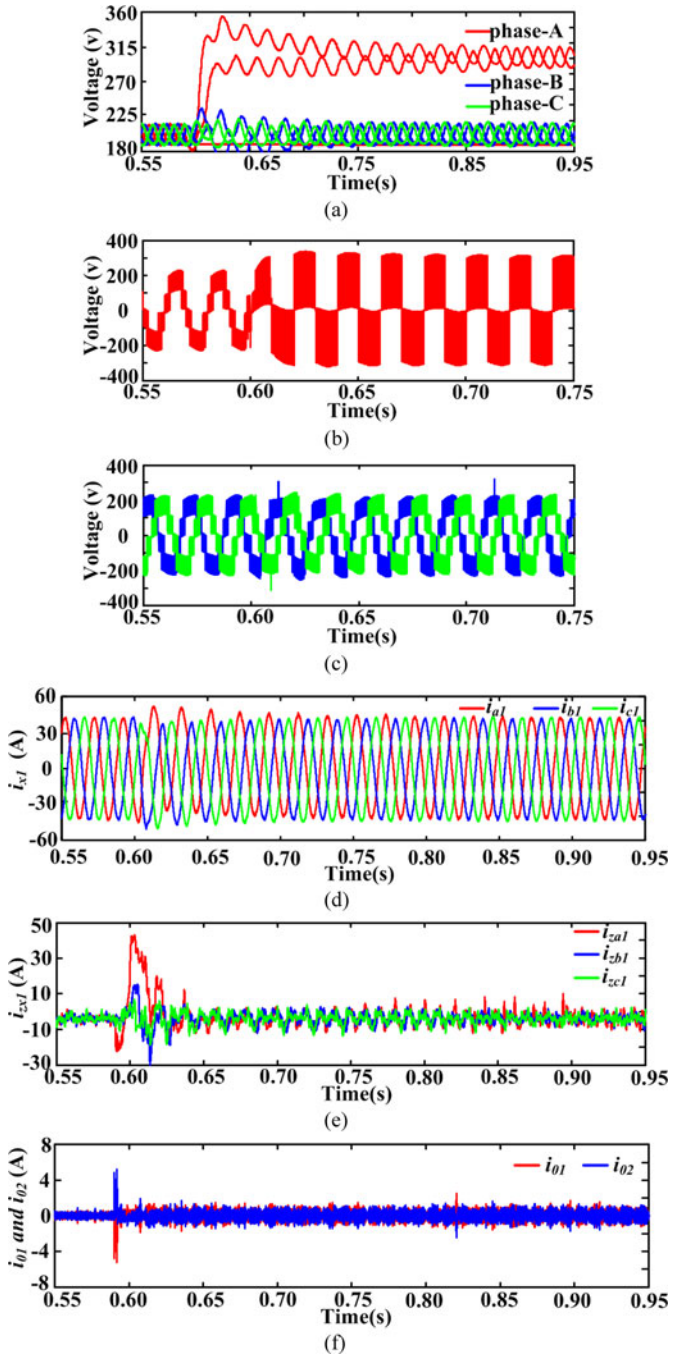

Fig. 18. Simulated waveforms of MMC 1 under IGBT 1 open-circuit fault condition: (a) capacitor voltages, (b) the output voltage of phase A, (c) the output voltages of phase B and C, (d) the three-phase output currents, (e) internal circulating currents of MMC 1, and (f) external circulating currents.

B. Simulation Results Under Fault-Tolerant Operation Conditions

Fig. 18 shows the simulated results of parallel-MMCs under the fault-tolerant operation condition when IGBT 1 in phase A of MMC 1 suffers the open-circuit failure at 0.59 s and the switching sequence is reconfigured at 0.6 s by fully considering the time delay induced by the fault detection algorithm and communications. It is noted that the healthy SM capacitor voltages in the faulty phase-leg are now charged to 300 V and others still remain 200 V as shown in Fig. 18(a). Fig. 18(b) and (c) shows that the phase A of MMC 1 produce a reduced level phase voltage while the phase voltages of phase B and C remain unchanged. Fig. 18(d) shows the three-phase output currents of MMC 1, which are quickly attenuated to be balanced after the switch failure. Fig. 18(e) and (f) shows the internal circulating currents of MMC 1 and the external circulating currents, respectively. It is noted that all circulating currents can be successfully suppressed again after the switch failure. Due to the inherent current limit characteristics, the fault detection and communication delays will not induce severe transient performance downgrade.

Fig. 19 shows the simulated results of parallel-MMCs under the fault-tolerant operation condition when IGBT 1 in phase A of MMC 1 suffers the short-circuit failure at 0.59 s. Similarly, the added time delay is 10 ms for reconfiguring the control function. As presented in Section V-B, the faulty phase-leg should be shut down to avoid the overvoltage damage. Therefore, the phase A current in MMC 1 is now reduced to zero and as a consequence the phase A current in MMC 2 continuously increases to reach its double value leaving other four phase currents unchanged as shown in Fig. 19(a) and (b). Therefore, the total output current can keep unchanged as expected as shown in Fig. 19(c). The current difference between two MMCs is shown in Fig. 19(d), where the zero current difference in phase B and C verifies that the external ZSCC control block can be removed when the parallel-MMCs switches to the five-leg operation conditions. The SM capacitor voltages of MMC 1 and MMC 2 are shown in Fig. 19(e) and (f), respectively. Note that only the capacitor voltages in phase A of MMC 2 are increased because a larger phase current flows through the corresponding SMs. The internal circulating currents of MMC 1 and MMC 2 are shown in Fig. 19(g) and (h), respectively. It is found that only the internal circulating currents of phase A in MMC 2 have obviously increased since its corresponding SM capacitor voltages are varying in a wider range as shown in Fig. 19(f).

VII. Experimental Verifications

To further verify the presented findings, an experimental prototype was constructed with two SMs per phase arm to power an inductive load with $L = 1$ mH and $R = 16\ \Omega$. The total dc supply voltage is 200 V, the buffer inductor is 2 mH, the dc capacitance per SM is 550 μF, and the switching frequency is 5 kHz. Due to the constraint of available components in the lab, only single MMC was constructed to verify the proposed circulating current suppression method and the voltage balancing control method. Fig. 20 shows the photograph of experimental prototype, where phase A, B, C, input dc source, and output load are clearly marked.

Fig. 21(a) shows the captured output current, arm currents, and circulating current under the open-loop control condition, where the circulating current contains the dominant second-, fourth-, and sixth-current harmonics as illustrated in the drawn spectrum of Fig. 21(b). Fig. 22 shows the measured capacitor voltages under the proposed closed-loop control method, where all SM capacitor voltages of phase A are captured. It is noted

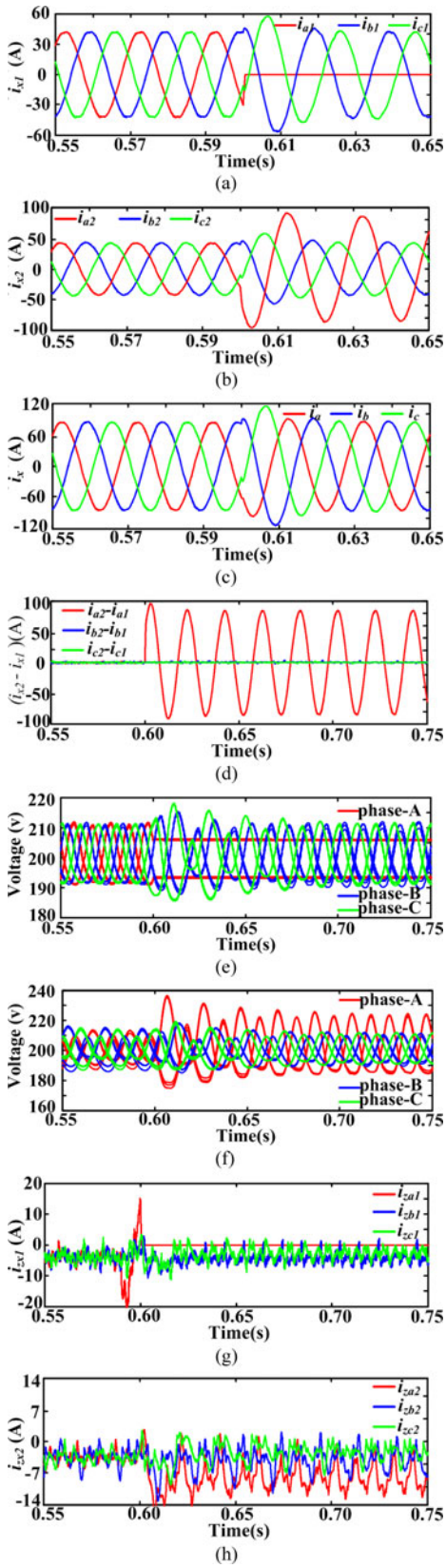

Fig. 19. Simulated waveforms under IGBT 1 of phase A in MMC 1 short-circuit fault condition: (a) the output three-phase currents of MMC 1, (b) the output three-phase currents of MMC 2, (c) the total output three-phase currents, (d) the current difference between two MMCs, (e) capacitors voltages in MMC 1, (f) capacitors voltages in MMC 2, (g) the circulating currents in MMC 1, and (h) the circulating currents in MMC 2.

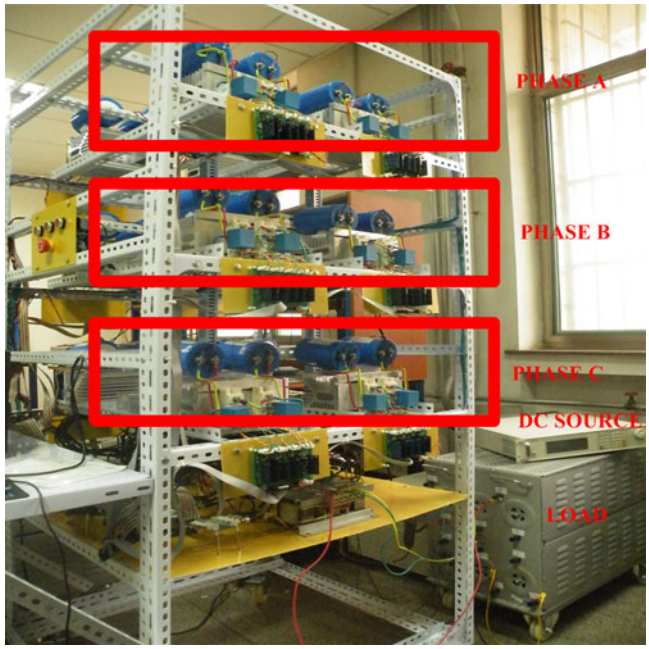

Fig. 20. Photograph of the experimental prototype.

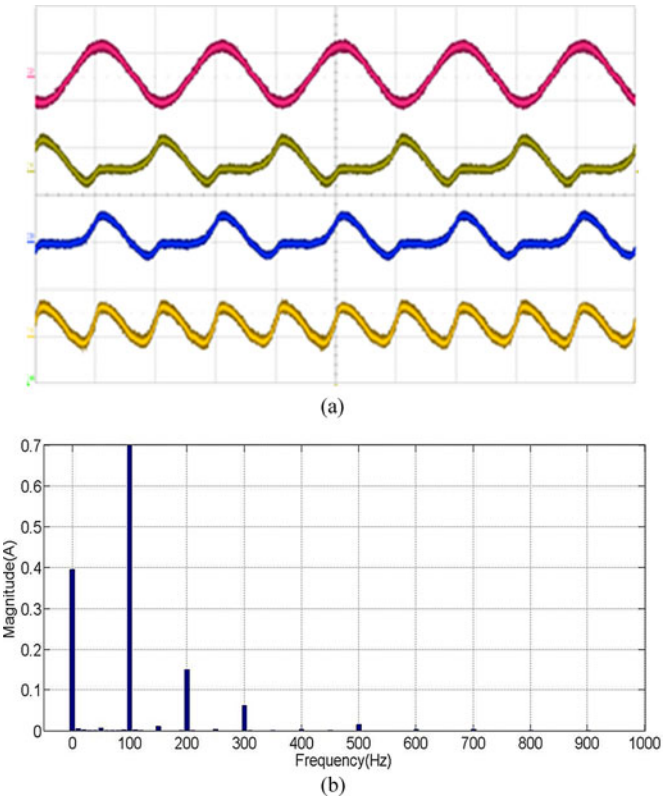

Fig. 21. Experimental results of (a) (from top to bottom) output current (5 A/div), negative arm current (5 A/div), positive arm current (5 A/div), and circulating current (5 A/div), and (b) spectrum of the circulating current.

that the capacitor voltages are around 100 V and well consistent. Fig. 23(a) shows the measured capacitor voltages of two SMs, the output current, the circulating current, and the arm currents under the proposed CCSC condition. And Fig. 23(b) shows the drawn spectrum of the circulating current. Comparatively, the

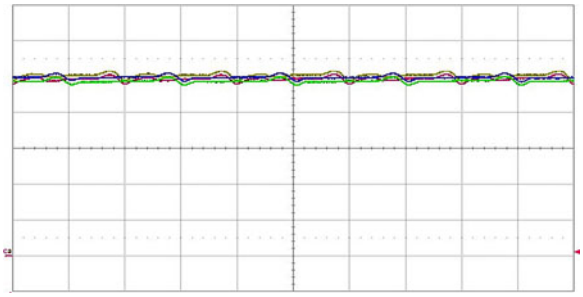

Fig. 22. Measured capacitor voltages of phase A in MMC1, 20 V/div.

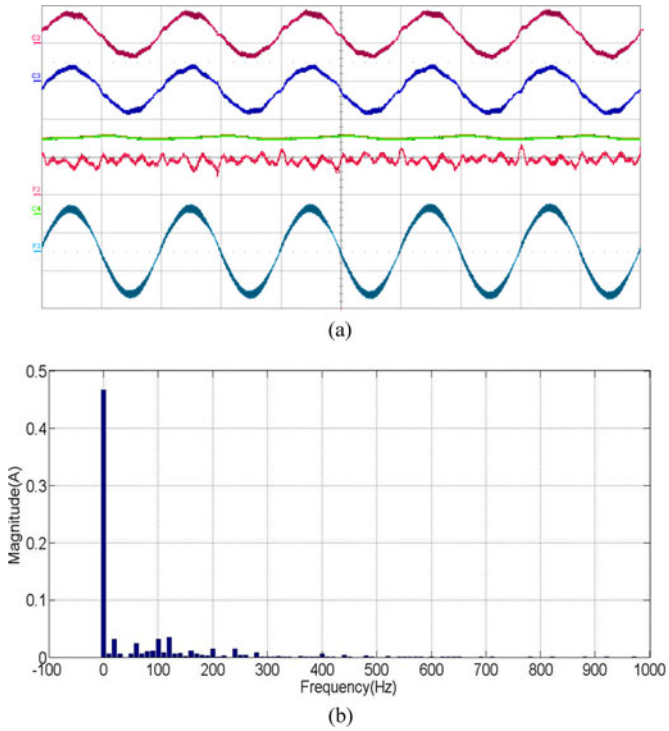

Fig. 23. Experimental results of (a) (from top to bottom) measured positive arm current (2 A/div), negative arm current (2 A/div), capacitor voltages of two SMs (50 V/div), circulating current (1 A/div), and output current (2 A/div), and (b) spectrum of the circulating current.

low-order circulating current harmonics have been suppressed significantly and distributed more evenly.

VIII. Conclusion

This paper presents the control methods of parallel-connected MMCs under both normal and switch fault-tolerant operation conditions. In order to reduce the calculation burden meanwhile increase the control accuracy of the internal circulating current suppression method; the resonant controllers are assumed in the synchronous reference frame to suppress the dominant second and fourth-order circulating current harmonics, and a sixth-order resonant controller is employed to suppress the zero-sequence internal circulating current. In addition, when the capacitor voltages are balanced as expected by using the voltage balancing control method, the external ZSCC can then be precisely controlled by treating the MMC as a simple two-level converter. This paper also proposes the fault-tolerant operation schemes as the switch in an SM suffers the open- or short-circuit failure. In principle, the fault-tolerant operation schemes will not influence the output quality by either adjusting the corresponding PWM schemes or the closed-loop control method. MATLAB simulations and the constructed experimental prototype verified the performance of proposed control method.

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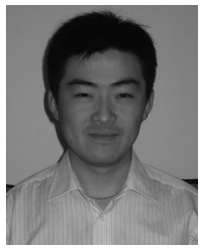

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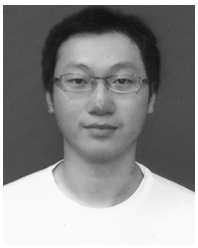

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