Characteristic Investigation and Control of a Modular Multilevel Converter-Based HVDC System Under Single-Line-to-Ground Fault Conditions

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***Abstract*—This paper presents the analysis and control of a multilevel modular converter (MMC)-based HVDC transmission system under three possible single-line-to-ground fault conditions, with special focus on the investigation of their different fault characteristics. Considering positive-, negative-, and zero-sequence components in both arm voltages and currents, the generalized instantaneous power of a phase unit is derived theoretically according to the equivalent circuit model of the MMC under unbalanced conditions. Based on this model, a novel double-line frequency dc-voltage ripple suppression control is proposed. This controller, together with the negative- and zero-sequence current control, could enhance the overall fault-tolerant capability of the HVDC system without additional cost. To further improve the fault-tolerant capability, the operation performance of the HVDC system with and without single-phase switching is discussed and compared in detail. Simulation results from a three-phase MMC-HVDC system generated with MATLAB/Simulink are provided to support the theoretical analysis and proposed control schemes.**

***Index Terms*—High-voltage direct-current (HVDC), modular multilevel converter (MMC), single-line-to-ground (SLG) fault.**

I. Introduction

RECENTLY, voltage source converter-based high-voltage direct-current (VSC-HVDC) transmission systems have drawn much interest to transmit power from far away locations, like offshore wind farms, to main ac power grids [1]–[3]. Compared to the line commutated converter-based HVDC, VSC-HVDC has the merits of black start capability, independent active as well as reactive power control, and power supply for weak ac grids. Meanwhile, the modular multilevel converter (MMC), featuring modular design, high efficiency, low distortion of the output voltage, compact size, etc., is regarded as a preferable choice and has already been implemented in some HVDC transmission projects (e.g., "TransBay Cable" Project) [4]–[8]. To take full advantage of an MMC and extend its application in HVDC transmission systems, the ability to deal with severe unbalanced conditions, especially under single-line-to-ground (SLG) fault, becomes a key requirement.

Several research efforts have focused on the operation and control of an MMC under unbalanced conditions [9]–[16]. Thanks to the distributed location of dc capacitors, the MMC has more degrees of freedom than two-level converters, which enables flexible control and uninterruptable performance with unbalanced input voltages [9], [10]. Proportional-integral-resonant-based controllers are proposed in [11] to mitigate the double-line frequency circulating current and the dc line current ripple under unbalanced conditions. Considering the impact of asymmetrical arm resistances, Zhou *et al.* [12] present proportional-resonant (PR)-based controllers for zero-sequence circulating current suppression. However, an ac active power ripple instead of an unbalanced ac side current is regulated for better control performance, which may cause malfunction of the protective devices. The operation of an MMC-based HVDC (MMC-HVDC) with converter-side SLG fault and dc line to ground fault is presented in [13]. With nongrounded or large resistance-grounded dc buses, no or low zero-sequence current is generated, and thus, the performance degradation is negligible. Nevertheless, this conclusion no longer applies to an HVDC system with a long dc cable and/or solid-grounded dc buses. By adopting the dual-current control scheme proposed in [14], a mathematical model for an MMC-HVDC system is derived in [15]. The zero-sequence current is well suppressed for transformerless HVDC applications with the designed controllers. However, as described in this paper, the double-line frequency dc-voltage ripple cannot be eliminated by instantaneous active and reactive power ripple control. To address this problem, a novel dc voltage ripple suppressing control is proposed in [16] using arm voltages feed-forward control. Nevertheless, unnecessary hardware and cost are introduced because of the six-arm voltage measurements that are needed. To take full advantage of an MMC, a control scheme of regulating differential currents of an MMC is proposed in [17] based on Lagrange-based optimization

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in "abc" coordinates. Either constant capacitive energy sum or with constant (pure dc) differential current per phase can be achieved to prevent ac power oscillation from propagating into the dc side under unbalanced conditions. However, this control scheme is quite complex with many average values calculation, and the differential current reference is related to control output variables, such as $v_{\rm dc}$ and $v_{\rm diff}$, which may lead to degraded steady state as well as dynamic response.

In addition, some related work has been done in two- and three-level converters. Adam *et al.*[18] present a recovery strategy for VSC-HVDC transmission systems by which the commonly applied dc chopper can be eliminated and the system resiliency can be improved during ac faults. A control scheme is proposed in [19]–[21] to suppress the possible dc-link voltage fluctuations under unbalanced conditions, while [22] decomposes the current vectors and controls them separately in terms of positive- and negative-sequence components to deal with unbalanced conditions in VSCs. For accurate decoupling between the positive- and negative-sequence controllers, a new control strategy for a VSC transmission system is presented in [23] under unbalanced network conditions. Moreover, in order to achieve smooth dc voltage in VSCs under unbalanced operation conditions, multifrequency PR controllers in $\alpha\beta$ frames are adopted in [24], considering both supply voltage and input impedance unbalance. A unified model representing the dynamic behavior of the three-level neutral point diode-clamped VSCs is built in [25], and control strategies are introduced to either balance the ac line currents or to mitigate the double-line frequency active and reactive power ripple.

However, to the authors' best knowledge, fault characteristics and necessary fault-isolated operation after the SLG fault occurs have not been investigated yet. Besides, the existing literature mainly focuses on the controller design when a fault occurs in the primary side of the Y/Δ transformer, i.e., the zero-sequence current is completely blocked by the delta connection of the transformer in the converter side, and thus, only positive- and negative-sequence currents need to be regulated, leading to a limited fault-tolerant capability. Furthering current works, this paper derives the phase unit instantaneous power under unbalanced conditions considering positive-, negative-, and zero-sequence components in both arm voltages and currents, which provides a straightforward insight into the origin of the dc-voltage ripple and the circulating current. In addition, to take full advantage of an MMC, a quasi-PR control is designed to suppress the second-order dc voltage ripple during the SLG fault without additional hardware costs. This controller, together with negative- and/or zero-sequence current control, enables the HVDC system to achieve the low dc-voltage ripple as well as balanced ac line currents at both converter stations on each end of the HVDC line. To verify the effectiveness of the designed controllers, the system performance with three possible SLG fault conditions has been investigated and compared in detail (specifically, SLG fault occurs in the (1) primary side, (2) secondary side of Y/Δ transformer, and (3) transformerless applications). Finally, the technical feasibility of single pole switching (SPS) is evaluated to maintain the system operation with acceptable performance degradation during an SLG fault.

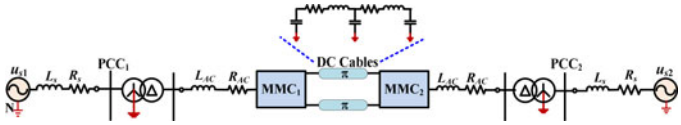

Fig. 1. Single-line diagram of an MMC-HVDC transmission system.

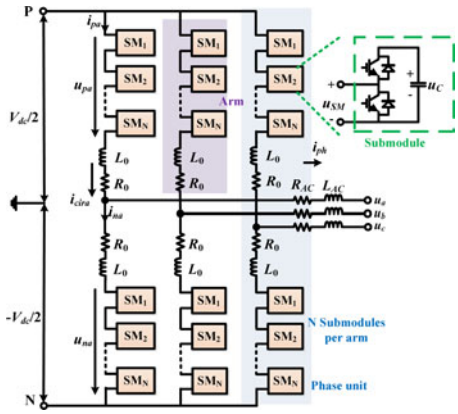

Fig. 2. Circuit configuration of an MMC.

This paper is structured as follows: Section II briefly introduces the configuration of an MMC-HVDC transmission system. A general phase unit instantaneous power is derived under SLG fault conditions in Section III, indicating the origin of the double-line frequency dc-voltage ripple and the circulating current. Section IV describes the proposed control architecture and its implementation, and in Section V, extensive simulation is carried out to analyze the fault characteristics under different SLG conditions, and also to verify the theoretical consideration as well as the designed control scheme. A summary of the fault-tolerant operation and its characteristic under each case is presented in Section VI, and Section VII provides the conclusion for this paper.

II. System Configuration

Fig. 1 illustrates the single-line diagram of an MMC-HVDC transmission system, where u_{s1} and u_{s2} represent ac grid voltages, L_s and R_s represent the grid impedance, $L_{\rm AC}$ and $R_{\rm AC}$ are ac reactor and its equivalent parasitic resistance. For isolation and voltage conversion, the ac terminal of each MMC is connected to the grid u_{s1} or u_{s2} through a three-phase Y/Δ transformer. The two MMCs are connected through dc cables and a two-section π type cable model is employed in this study. As a crucial factor, grounding points are located at dc cables through capacitors, each neutral point of AC grids, and Y connection of transformers.

The configuration of an MMC is shown in Fig. 2. Each phase leg of the MMC consists of one upper and one lower arm connected in series between the dc terminals. *N* series-connected sub-modules (SMs) and one arm inductor L_0 form an arm. Each SM contains an IGBT half-bridge as a switching element and a dc storage capacitor.

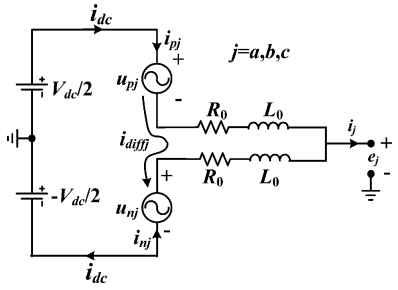

Fig. 3. Single-phase equivalent circuit of the MMC.

Fig. 3 illustrates the single-phase equivalent circuit of an MMC [26], where e_j and i_j represent the phase voltage and line current of phase *j*, respectively, u_{pj} and u_{nj} are the voltages produced by the SMs in the upper and lower arm, respectively; i_{pj} and i_{nj} denote the corresponding arm currents, and $i_{\mathrm{diff}\,j}$ is the circulating current in phase *j*.

III. Analysis of the Phase Unit Instantaneous Power Under Unbalanced Conditions

According to the single-phase equivalent circuit shown in Fig. 3, an MMC can be characterized by the following equations:

$$\begin{aligned} u_{pj} &= \frac{V_{\mathrm{dc}}}{2} - e_j - u_{\mathrm{diff}\,j} \\ u_{nj} &= \frac{V_{\mathrm{dc}}}{2} + e_j - u_{\mathrm{diff}\,j} \\ u_{\mathrm{diff}\,j} &= L_0 \frac{di_{\mathrm{diff}\,j}}{dt} + R_0 i_{\mathrm{diff}\,j} \quad (j = a, b, c) \end{aligned} \tag{1}$$

where e_j stands for the voltage reference produced by the controllers in phase *j*, a fundamental frequency voltage under balanced conditions. According to [27], u_{diff} mainly consists of a negative-sequence double-line frequency component.

During an SLG fault, with dc-voltage ripple suppression and current controllers, the voltage reference could contain positive-, negative-, and/or zero-sequence components. Taking phase A as an example, (1) can be rewritten as

$$\begin{aligned} u_{pa} &= \frac{V_{\mathrm{dc}}}{2} - U^+ \sin(\omega_f t + \alpha_+) - U^- \sin(\omega_f t + \alpha_-) \\ &\quad - U^0 \sin(\omega_f t + \alpha_0) - U^-_{\mathrm{diff}} \sin(2\omega_f t + \beta_-) \\ &= \frac{V_{\mathrm{dc}}}{2} \begin{bmatrix} 1 - k^+ \sin(\omega_f t + \alpha_+) - k^- \sin(\omega_f t + \alpha_-) \\ -k^0 \sin(\omega_f t + \alpha_0) - l^- \sin(2\omega_f t + \beta_-) \end{bmatrix} \\ u_{na} &= \frac{V_{\mathrm{dc}}}{2} + U^+ \sin(\omega_f t + \alpha_+) + U^- \sin(\omega_f t + \alpha_-) \\ &\quad + U^0 \sin(\omega_f t + \alpha_0) - U^-_{\mathrm{diff}} \sin(2\omega_f t + \beta_-) \\ &= \frac{V_{\mathrm{dc}}}{2} \begin{bmatrix} 1 + k^+ \sin(\omega_f t + \alpha_+) + k^- \sin(\omega_f t + \alpha_-) \\ +k^0 \sin(\omega_f t + \alpha_0) - l^- \sin(2\omega_f t + \beta_-) \end{bmatrix} \end{aligned} \tag{2}$$

where U^+, U^-, and U^0 are the amplitudes of the positive-, negative-, and zero-sequence voltage references, respectively, α_+, α_-, and α_0 are the corresponding initial phase angles, $\omega_f = 2\pi \cdot 60$ rad/s, U_{diff} represents the amplitude of the voltage reference produced by the circulating current control, and β_- denotes its initial phase angle; k^+, k^-, and k^0 are the positive-, negative-, and zero-sequence voltage modulation index, as shown in (3). Similarly, l^- represents the ratio of the voltage reference used for circulating current suppression to the dc voltage given by (4)

$$k^+ = \frac{U^+}{V_{\mathrm{dc}}/2} k^- = \frac{U^-}{V_{\mathrm{dc}}/2} k^0 = \frac{U^0}{V_{\mathrm{dc}}/2} \tag{3}$$

$$l^- = \frac{U^-_{\mathrm{diff}}}{V_{\mathrm{dc}}/2}. \tag{4}$$

Assuming that the circulating current is eliminated, while the negative- and/or zero-sequence currents are not completely compensated because of limited control bandwidth, converter power capacity constraints, conflicts among controllers, or computation errors, etc., the upper and lower arm currents can be decomposed as

$$\begin{aligned} i_{pa} &= \frac{I_{\mathrm{dc}}}{3} + \frac{I^+_{\mathrm{ac}}}{2} \sin(\omega_f t + \gamma_+) + \frac{I^-_{\mathrm{ac}}}{2} \sin(\omega_f t + \gamma_-) \\ &\quad + \frac{I^0_{\mathrm{ac}}}{2} \sin(\omega_f t + \gamma_0) \\ &= \frac{I_{\mathrm{dc}}}{3} [1 + m^+ \sin(\omega_f t + \gamma_+) + m^- \sin(\omega_f t + \gamma_-) \\ &\quad + m^0 \sin(\omega_f t + \gamma_0)] \\ i_{na} &= \frac{I_{\mathrm{dc}}}{3} - \frac{I^+_{\mathrm{ac}}}{2} \sin(\omega_f t + \gamma_+) - \frac{I^-_{\mathrm{ac}}}{2} \sin(\omega_f t + \gamma_-) \\ &\quad - \frac{I^0_{\mathrm{ac}}}{2} \sin(\omega_f t + \gamma_0) \\ &= \frac{I_{\mathrm{dc}}}{3} [1 - m^+ \sin(\omega_f t + \gamma_+) - m^- \sin(\omega_f t + \gamma_-) \\ &\quad - m^0 \sin(\omega_f t + \gamma_0)] \end{aligned} \tag{5}$$

where I^+_{ac}, I^-_{ac}, and I^0_{ac} are the amplitudes of the positive-, negative-, and zero-sequence phase current, respectively, and m^+, m^-, and m^0 stand for the associated current modulation index, respectively; γ_+, γ_-, and γ_0 are the corresponding initial phase angles.

According to (1), (2), and (5), the per unit instantaneous power in phase A is calculated as (6). Similarly, the instantaneous power in phases B and C is derived as (7) and (8)

$$\begin{aligned} p_a &= u_{pa} i_{pa} + u_{na} i_{na} \\ &= \frac{V_{\mathrm{dc}} I_{\mathrm{dc}}}{6} [2 - k^+ m^+ \cos(\alpha_+ - \gamma_+) - k^- m^- \\ &\quad \times \cos(\alpha_- - \gamma_-) - k^0 m^0 \cos(\alpha_0 - \gamma_0) \\ &\quad - k^- m^+ \cos(\alpha_- - \gamma_+) - k^0 m^- \cos(\alpha_0 - \gamma_-) - k^+ m^0 \\ &\quad \times \cos(\alpha_+ - \gamma_0) \\ &\quad - k^0 m^+ \cos(\alpha_0 - \gamma_+) - k^+ m^- \cos(\alpha_+ - \gamma_-) - k^- m^0 \end{aligned}$$

$$\times \cos(\alpha_- - \gamma_0)$$
$$+k^- m^+ \cos(2\omega_f t + \alpha_- + \gamma_+)$$
$$+k^+ m^- \cos(2\omega_f t + \alpha_+ + \gamma_-) + k^0 m^0 \cos(2\omega_f t + \alpha_0 + \gamma_0)$$
$$+k^0 m^+ \cos(2\omega_f t + \alpha_0 + \gamma_+) + k^- m^- \cos(2\omega_f t + \alpha_- + \gamma_-)$$
$$+ k^+ m^0 \cos(2\omega_f t + \alpha_+ + \gamma_0)$$
$$+k^+ m^+ \cos(2\omega_f t + \alpha_+ + \gamma_+) + k^0 m^- \cos(2\omega_f t + \alpha_0 + \gamma_-)$$
$$+ k^- m^0 \cos(2\omega_f t + \alpha_- + \gamma_0) - 2l^- \sin(2\omega_f t + \beta_-)] \quad (6)$$

$$p_b = u_{pb} i_{pb} + u_{nb} i_{nb}$$
$$= \frac{V_{\mathrm{dc}} I_{\mathrm{dc}}}{6} [2 - k^+ m^+ \cos(\alpha_+ - \gamma_+)$$
$$- k^- m^- \cos(\alpha_- - \gamma_-) - k^0 m^0 \cos(\alpha_0 - \gamma_0)$$
$$- k^- m^+ \cos(\alpha_- - \gamma_+ - 120^\circ) - k^0 m^-$$
$$\times \cos(\alpha_0 - \gamma_- - 120^\circ) - k^+ m^0 \cos(\alpha_+ - \gamma_0 - 120^\circ)$$
$$- k^0 m^+ \cos(\alpha_0 - \gamma_+ + 120^\circ) - k^+ m^-$$
$$\times \cos(\alpha_+ - \gamma_- + 120^\circ) - k^- m^0 \cos(\alpha_- - \gamma_0 + 120^\circ)$$
$$+ k^- m^+ \cos(2\omega_f t + \alpha_- + \gamma_+)$$
$$+k^+ m^- \cos(2\omega_f t + \alpha_+ + \gamma_-) + k^0 m^0 \cos(2\omega_f t + \alpha_0 + \gamma_0)$$
$$+ k^0 m^+ \cos(2\omega_f t + \alpha_0 + \gamma_+ - 120^\circ) + k^- m^-$$
$$\cos(2\omega_f t + \alpha_- + \gamma_- - 120^\circ)$$
$$+ k^+ m^0 \cos(2\omega_f t + \alpha_+ + \gamma_0 - 120^\circ)$$
$$+ k^+ m^+ \cos(2\omega_f t + \alpha_+ + \gamma_+ + 120^\circ) + k^0 m^-$$
$$\times \cos(2\omega_f t + \alpha_0 + \gamma_- + 120^\circ)$$
$$+ k^- m^0 \cos(2\omega_f t + \alpha_- + \gamma_0 + 120^\circ)$$
$$- 2l^- \sin(2\omega_f t + \beta_- + 120^\circ)] \quad (7)$$

$$p_c = u_{pc} i_{pc} + u_{nc} i_{nc}$$
$$= \frac{V_{\mathrm{dc}} I_{\mathrm{dc}}}{6} [2 - k^+ m^+ \cos(\alpha_+ - \gamma_+) - k^- m^-$$
$$\times \cos(\alpha_- - \gamma_-) - k^0 m^0 \cos(\alpha_0 - \gamma_0)$$
$$- k^- m^+ \cos(\alpha_- - \gamma_+ + 120^\circ) - k^0 m^-$$
$$\times \cos(\alpha_0 - \gamma_- + 120^\circ) - k^+ m^0 \cos(\alpha_+ - \gamma_0 + 120^\circ)$$
$$- k^0 m^+ \cos(\alpha_0 - \gamma_+ - 120^\circ) - k^+ m^-$$
$$\times \cos(\alpha_+ - \gamma_- - 120^\circ) - k^- m^0 \cos(\alpha_- - \gamma_0 - 120^\circ)$$
$$+ k^- m^+ \cos(2\omega_f t + \alpha_- + \gamma_+) + k^+ m^-$$
$$\times \cos(2\omega_f t + \alpha_+ + \gamma_-) + k^0 m^0 \cos(2\omega_f t + \alpha_0 + \gamma_0)$$
$$+ k^0 m^+ \cos(2\omega_f t + \alpha_0 + \gamma_+ + 120^\circ) + k^- m^-$$
$$\times \cos(2\omega_f t + \alpha_- + \gamma_- + 120^\circ)$$
$$- k^+ m^0 \cos(2\omega_f t + \alpha_+ + \gamma_0 + 120^\circ)$$
$$+ k^+ m^+ \cos(2\omega_f t + \alpha_+ + \gamma_+ - 120^\circ) + k^0 m^-$$
$$\times \cos(2\omega_f t + \alpha_0 + \gamma_- - 120^\circ)$$
$$+ k^- m^0 \cos(2\omega_f t + \alpha_- + \gamma_0 - 120^\circ)$$
$$- 2l^- \sin(2\omega_f t + \beta_- - 120^\circ)]. \quad (8)$$

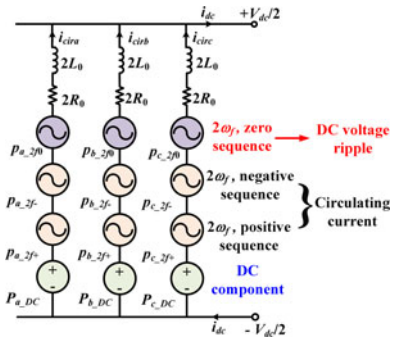

Fig. 4. Three-phase equivalent circuit of an MMC under unbalanced conditions.

As described in (6)–(8), the instantaneous power of each phase unit is composed of dc components (first three rows), zero-sequence (the fourth row), positive-sequence (the fifth and sixth rows), and negative-sequence (the last two rows) double-line frequency ac components.

For better understanding, the three-phase equivalent circuit of the instantaneous power in an MMC under SLG fault is summarized in Fig. 4 based on the above equations. Among the instantaneous power components, the dc item P_{j_DC} $(j = a, b, c)$ helps to maintain the dc voltage, while the three-phase currents generated by positive- and negative-sequence ac components ($P_{j\_2f^-}$ and $P_{j\_2f^+}$) counteract each other, thus flowing among phase units and forming both positive- as well as negative-sequence circulating currents. However, the zero-sequence ac components P_{j_2f0} have to flow into the dc bus since they cannot cancel with each other among the three phases, resulting in the double-line frequency ripple in the dc-bus voltage.

In (6)–(8), under balanced conditions, k^-, k^0, m^-, and m^0 equal to zero, while under unbalanced conditions, even if negative- and zero-sequence currents are eliminated (i.e. m^-, and m^0 equal to zero), the negative-sequence voltage reference k^- would not be zero. Therefore, the dc-voltage ripple is unavoidable, and its magnitude will increase with the higher negative-sequence voltage and positive-sequence current. Similarly, except for the negative-sequence circulating current that exists under all conditions, the positive-sequence circulating current will also be generated because of nonzero voltage reference m^0 used for zero-sequence current regulation under certain conditions.

This phase unit second-order power derivation aims at providing the existence and components of the second-order power in the dc side, if no circulating current control is applied, and is unable to give a quantified magnitude of the second dc voltage and the current ripple.

IV. Control Scheme Under an SLG Fault

In this paper, MMC_1 in Fig. 1 controls the dc voltage and the reactive power, while MMC_2 is assigned to regulate the

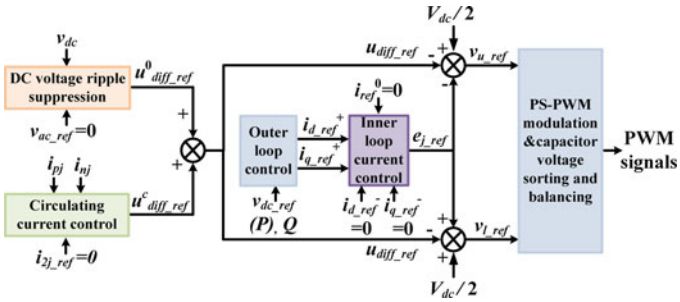

Fig. 5. Control scheme of an MMC under unbalanced condition.

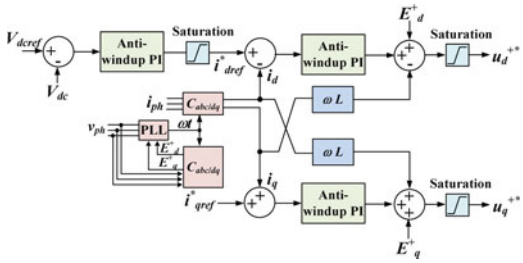

Fig. 6. Diagram of positive-sequence current control.

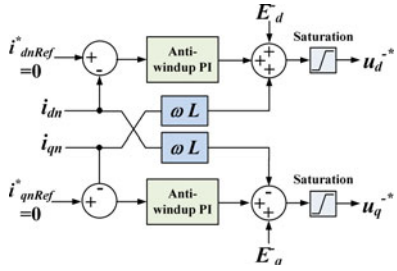

Fig. 7. Diagram of negative-sequence current suppression.

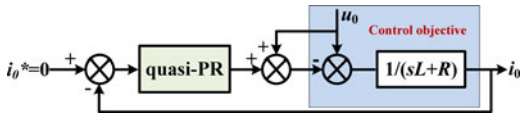

Fig. 8. Control diagram of the zero-sequence current.

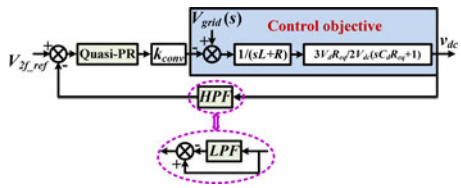

Fig. 9. Control diagram for the dc-voltage ripple suppression.

active and reactive power generation. Although the multiresonant frequency-adaptive synchronization method proposed in [28] can be applied to detect the fundamental frequency positive- and negative-sequence components under highly unbalanced and distorted grid conditions; a common phase-locked loop (PLL) structure is adopted for the studied system to simplify the control scheme and unify the problem.

Fig. 5 shows the overall control diagram under unbalanced conditions. According to the functionality assignment, the outer loop references are the dc voltage and the reactive power in the rectifier station (MMC_1), while those for the inverter station (MMC_2) are active and reactive power. The sum of the references generated by positive-, negative-, and zero-sequence current regulation forms the phase voltage command e_{j_ref}. The output of the dc-voltage ripple suppression controller, i.e., $u^0_{\mathrm{diff\_ref}}$ in $u_{\mathrm{diff\_ref}}$, is subtracted from both the upper and lower arms' voltage references, which is similar to the implementation of circulating current control. As indicated from (1), the dc-voltage ripple suppression controller will not affect the normal phase voltage generation (e_j). Hence, both the unbalanced current and the dc-voltage ripple can be eliminated at the same time, enabling desirable performance of MMC-HVDC under SLG faults.

With properly designed control parameters, it is unnecessary to deactivate the negative- and/or zero-sequence current regulation, as well as the double-line frequency dc-voltage ripple suppression control immediately when the fault is cleared, which reduces the requirement for fast fault detection.

$(N+1)$-level phase shift pulse width modulation is adopted in this study for its high equivalent switching frequency and relatively simple implementation. To balance capacitor voltages among SMs and enable small arm inductances, the capacitor voltage balancing method and circulating current suppression techniques in [29] are employed.

The detailed positive-sequence current controller is illustrated in Fig. 6. To achieve accurate synchronization with the grid voltage, the positive-sequence voltage is extracted with methods proposed in [30] and used as the input of a PLL. In addition, the converter-side phase current in *dq* coordinates (I_d and I_q) are directly used for power and/or voltage control. Compared to the single-positive-sequence current control used in dual-current control, the negative-sequence voltage reference is generated instantaneously when an SLG fault occurs, which is beneficial for system stability and fast compensation of grid voltage variation by avoiding any delay introduced by the current extractor, fault detection, or controllers activation.

Fig. 7 shows the control diagram of the negative-sequence current compensation. The same method in [30] is used for negative-sequence current extraction. By setting the reference i^*_{dnref} and i^*_{qnref} to be zero, the negative-sequence current can be eliminated using a PI controller in *dq* coordinates. For zero-sequence current elimination under certain circumstances, a quasi-PR controller is employed, as shown in Fig. 8.

A quasi-PR-based feedback control is proposed in this paper to mitigate the double-line frequency dc-voltage ripple. Fig. 9 shows the control diagram of the dc-ripple suppression, where k_{conv} represents the gain of converters, *L* is the effective ac side inductance ($L_{\mathrm{AC}} + L_0/2$), *R* stands for the equivalent inductor series resistance, R_{eq} denotes the equivalent dc impedance; the second-order dc voltage ripple reference v_{2f_ref} is set to zero. A second high-pass filter (HPF) is employed to eliminate any dc

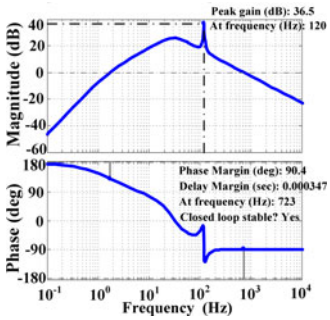

Fig. 10. Open-loop bode plot of dc-voltage ripple control.

component. In a practical implementation, it can be realized that $v_{\rm dc}$ subtracts its low-frequency components for easier software or hardware implementation (represented as the dashed circles in Fig. 9). Since only the dc voltage is detected, no extra cost is introduced for the control implementation.

The transfer functions of the PR controller and the HPF are given as

$$H_{\rm HPF}(s) = \frac{k_0 s^2}{s^2 + \xi\omega_n s + \omega_n^2}$$
$$H_{\rm PR}(s) = k_p + \frac{2k_r\omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \tag{9}$$

where k_0 is a gain constant, ξ is a damping ratio, ω_n is the natural frequency of the HPF, k_p, k_r represent controller gains, ω_c is the cutoff frequency, and ω_0 is the angular frequency of the control target.

Based on Fig. 9 and (9), the open-loop transfer function from $v_{\rm dc}$ to $v_{2f_{\rm ref}}$ can be derived as

$$G(s) = \frac{3V_{\rm rms}R_{\rm eq}k_0k_{\rm conv}s^2[k_ps^2 + 2\omega_c(k_p+k_r)s + k_p\omega_0^2]}{\sqrt{2}V_{\rm dc}(sC_dR_{\rm eq}+1)(sL+R)(s^2+2\omega_c s+\omega_0^2)(s^2+\xi\omega_n s+\omega_n^2)}. \tag{10}$$

Finally, the main control parameters are selected as: $k_p = 1.5$, $k_r = 50$, $\omega_c = 10$ rad/s, $\omega_0 = 2\pi \times 120 = 753.6$ rad/s, $\xi = 1.2$, $k_0 = 0.2$, and $\omega_n = 2\pi \times 30 = 188$ rad/s. The corresponding open-loop bode plot is illustrated in Fig. 10, with the magnitude as high as 36.5 dB at the second harmonic frequency. Moreover, the cutoff frequency is set to be around one-tenth (723 Hz) of the equivalent switching frequency 7.2 kHz (4×1.8-kHz carrier frequency), enabling sufficient mitigation of the switching ripple.

V. Case Study

A. System Parameters

A three-phase MMC-HVDC transmission system with the controllers designed in Section IV is established in MATLAB/Simulink, and the system parameters are summarized in Table I.

Considering that the control performance under unbalanced conditions is not affected by the number of SMs N, ($N = 4$) cells per arm is used in this paper to achieve acceptable simulation time. Moreover, the current references of all converters are limited to $I_{\rm dref\_max} = 1.36I_{\rm drated}$ (222 A, $I_{\rm dmax} = 1.1I_{\rm drated}$, $I_{\rm qmax} = 0.8I_{\rm drated}$, where $I_{\rm drated}$ is the converter-side rated d-axis current in $\rm MMC_2$.

TABLE I
MAIN CIRCUIT PARAMETERS OF MMC-HVDC

Parameters	Values
DC-Link voltage $V_{\rm dc}$	5 kV
AC system voltage u_{s1}, u_{s2}	10 kV
Voltage frequency	60 Hz
Transformer ratio	10 kV/2.5 kV
Transformer leakage inductance	0.01 mH
No. of SMs in each arm N	4
SM capacitance	4000 μF
AC-side inductance $L_{\rm AC1}$, $L_{\rm AC2}$	9.55 mH
Arm inductance L_0	11.27 mH
Carrier frequency	1.8 kHz
Rectifier side reactive power reference	0 Var
Inverter-side active power reference	0.5 MW
Inverter-side reactive power reference	0.25 MVar
DC cable length	50 km
Resistance per unit length	13.9 mΩ/km
Inductance per unit length	159 μH/km
Capacitance per unit length	0.231 μF/km

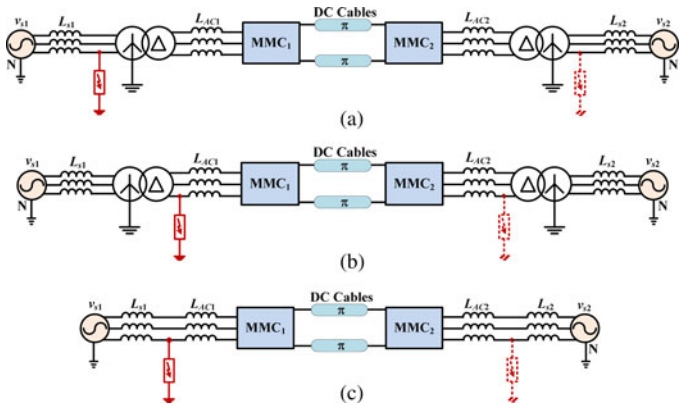

Fig. 11. Different SLG fault locations. (a) SLG fault occurring in the primary side of Y/Δ transformer (case 1). (b) SLG fault occurring in the secondary side of Y/Δ transformer (case 2). (c) SLG fault occurring in a transformerless application (case 3).

B. Studied Fault Cases

In practice, an SLG fault may occur in different locations due to insulation damage or poor connection. In this paper, the fault conditions are categorized into the following three cases.

Case 1 (SLG Fault Occurs in the Primary Side of the Y/Δ Transformer): Fig. 11(a) shows the system schematic with SLG fault occurring in phase C. The solid line fault represents an SLG fault in the rectifier side, while the dashed line stands for an SLG fault in the inverter side. With delta connection in the secondary side, no zero-sequence current will flow into the converter side. During an SLG fault period, the negative-sequence voltage in the primary side will be introduced to the secondary side of the interfacing Y/Δ transformer, and results

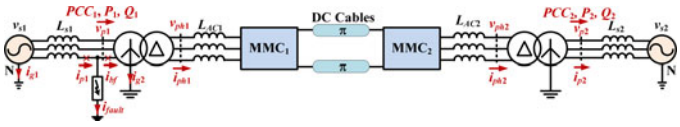

Fig. 12. Rectifier side SLG fault in case 1.

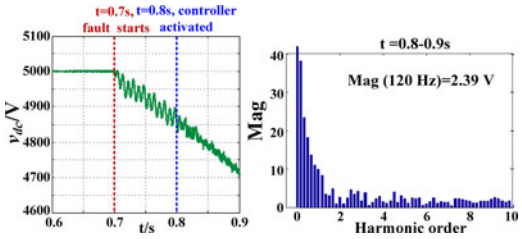

Fig. 13. DC voltage and its spectrum with an SLG fault in case 1 (MMC_1 side).

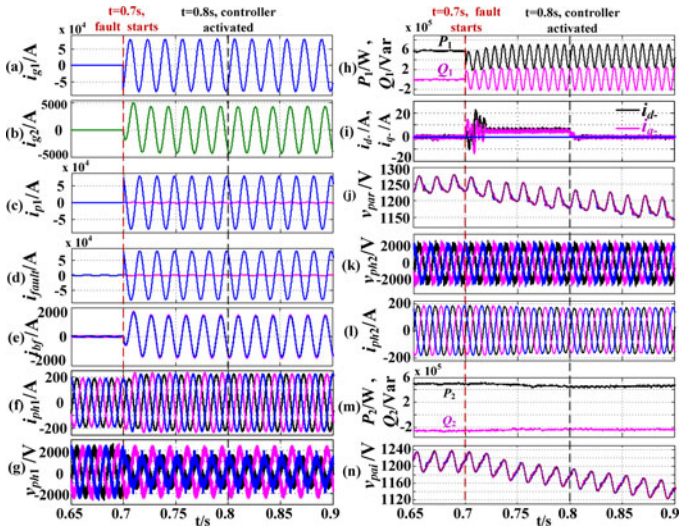

Fig. 14. Simulation waveforms of the studied system under an SLG fault in case 1 (MMC_1 side). $\mathbf{MMC}_1$ **side:** (a) ac grid ground current, (b) transformer primary side ground current, (c) phase currents before the fault point, (d) fault current, (e) phase currents after the fault point, (f) phase current in the delta side of the Y/Δ transformer, (g) phase voltage in the delta side of the Y/Δ transformer, (h) active and reactive power, (i) negative-sequence current components, and (j) upper arm SM capacitor voltages in phase A; $\mathbf{MMC}_2$ **side:** (k) phase voltage in the delta side of the Y/Δ transformer, (l) phase current in the delta side of the Y/Δ transformer, (m) active and reactive power, and (n) upper arm SM capacitor voltages in phase A.

in the negative-sequence current in the converter side if there is no negative-sequence control for the converters.

Case 2 (SLG Fault Occurs in the Secondary Side of the Y/Δ Transformer): Fig. 11(b) illustrates the system schematic in case 2, and the SLG fault occurs in phase C. Similarly, with delta-connected winding in the converter side, the grid utility can be free from the zero-sequence current caused by faults.

Case 3 (SLG Fault Occurs in a Transformerless System): The system schematic of a transformerless-HVDC with an SLG fault occurring in phase C is given in Fig. 11(c) by removing both Y/Δ transformers in Fig. 11(a). Different from the above two cases, the zero sequence current will not be blocked any more, thus flowing into the ac grids at each converter station and forming ground currents.

C. Fault-Tolerant Operation With Designed Controllers in Case 1

An SLG fault occurs in phase C at 0.7 s, and the negative- and/or zero-sequence current control together with dc voltage ripple suppression is activated at 0.8 s. Without a ground loop between the secondary sides of the Y/Δ transformer in two converter stations, the SVM scheme is adopted for high dc-voltage utilization.

1) SLG Fault Occurs in the Rectifier Side: As a clear description, the circuit diagram is redrawn in Fig. 12 with crucial voltages and currents labeled. The corresponding simulation waveforms at MMC_1 and MMC_2 are illustrated in Figs. 13 and 14, respectively.

Due to the preset current limitation, power balance between the generation of rectifier and absorption of the inverter is broken, and consequently, the dc voltage drops gradually during the SLG fault. This voltage drop, however, will not finally stop until another power balance is achieved because of overmodulation in the inverter station (the dc voltage can be maintained if the maximum phase current is limited to $1.5I_{\mathrm{rated}}$ or larger). A double-line frequency ripple with a magnitude of 24.31 V is observed in the dc voltage, resulting in the dc capacitor overstress as well as possible power distortion in the inverter side. When the dc voltage ripple suppression control is activated at 0.8 s, the double-line frequency dc voltage ripple is reduced to 2.39 V in two fundamental cycles (see Fig. 13), in spite of a slightly larger high-frequency ripple caused by additional switching actions. In addition, low-frequency harmonics within the control bandwidth are also partially mitigated, contributing to high-output power quality.

As shown in Fig. 14, the ac grid u_{s1} and MMC_1 keep feeding the fault, and produce significant ground currents i_{g1} [see Fig. 14(a)] and i_{g2} [see Fig. 14(b)]. The ground current, in the form of the zero-sequence current, flows through i_{p1} and i_{bf} and forces the three-phase current i_{bf} to overlap [see Fig. 14(e)]. Furthermore, C phase current in i_{p1} becomes much larger than the other two healthy phases [see Fig. 14 (c)]. To meet the power demands from the inverter, the converter-side phase current i_{ph1} in the rectifier increases from 181 A to its maximum allowed value 222 A [see Fig. 14(f)].

As mentioned previously, the negative-sequence voltage is created by the converter when the fault occurs [see Fig. 14(g)], which partially reduces the negative-sequence current. When the designed control starts at 0.8 s, the negative-sequence voltage generated by the converter is regulated to be exactly the same as that in the grid side. Consequently, the *dq*-axis negative-sequence currents are eliminated in about 0.1 s [see Fig. 14(i)]. Fig. 14(h) illustrates the active and reactive power in the rectifier side, represented as P_1 and Q_1, respectively. Besides the large double-line frequency ripple, the active power absorbed by MMC_1 is 1/3 lower because of the voltage drop at PCC_1.

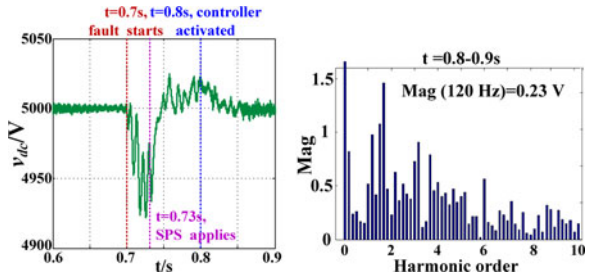

Fig. 15. DC voltage with SPS in case 1 (MMC_1 side).

As shown in Fig. 14(j), although SMs' capacitor voltages are well balanced, their mean value gradually decreases from 1250 V due to the dc voltage drop. In addition, the capacitor voltage ripple increases by 10 V because of larger charging and discharging phase currents.

In the inverter station, phase voltage v_{ph2} is not affected, while the magnitude of phase current i_{ph2} decreases from 163.3 A to 150.2 A due to the reduced power generation in the rectifier side (Fig. 14(k) and (l)). For the same reason, the active power output of MMC_2 drops from 0.5 MW to around 0.46 MW, and the reactive power is reduced from 0.25 MVar to around 0.23 MVar, as shown in Fig. 14(m). With 150-V voltage drop in the dc cables, the average value of SMs' capacitor voltages in MMC_2 becomes 1212.5 V in the steady state [see Fig. 14(n)]. Like Fig. 14(j), although the capacitor voltages keep decreasing, they are well balanced with the smaller ripple.

The feasibility of SPS presented in [31] and [32] is also investigated in this paper for continuous load power supply and system protection under permanent SLG fault conditions. The faulted phase (phase C) instead of all three phases is cut from both sides, as illustrated by the red crossings in Fig. 12. Limited by the negative impact of the unbalanced phase current, the system with SPS can only survive a temporary SLG fault. Otherwise, all three phases will be tripped after a certain time (normally 0.5 s) [33].

Figs. 15 and 16 give the dc voltage and the ac waveforms in MMC_1 and MMC_2 stations, respectively, with SPS started at $t = 0.7$ s. A reasonable assumption is made here that it takes 30 ms to open a single pole breaker. After a transient process, the dc voltage finally recovers to its rated value at $t = 0.85$ s, and the double-line frequency ripple decreases from 8.81 to 0.23 V after the designed controllers are activated (see Fig. 15). Compared with the case without SPS, the dc voltage ripple is much smaller thanks to the lower positive- and negative-sequence current.

However, as shown in Fig. 16(a) and (b), there is still a ground current within the loop between the ac grid u_{s1} and transformer grounds. This ground current would necessarily create a zero-sequence current in the two healthy phases [see Fig. 16(c) and (e)], but its magnitude is reduced to 140 A, and will not cause any damage in a short time period. A 1-MΩ grounding snubber resistance is chosen to get the i_{fault} smaller than 20 mA [see Fig. 16(d)].

Fig. 16(f) and (g) gives the delta side phase current and voltage, respectively. Without the faulted phase, both the current and

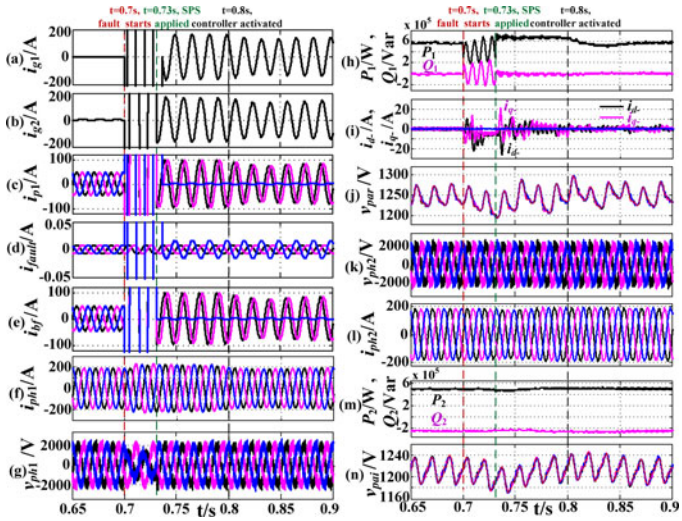

Fig. 16. Simulation waveforms of the studied system under an SLG fault with SPS in case 1 ($\mathbf{MMC}_1$ side). $\mathbf{MMC}_1$ **side:** (a) ac grid ground current, (b) transformer primary side ground current, (c) phase currents before the fault point, (d) fault current, (e) phase currents after the fault point, (f) phase current in the delta side of the Y/Δ transformer, (g) phase voltage in the delta side of the Y/Δ transformer, (h) active and reactive power, (i) negative-sequence current components, and (j) upper arm SM capacitor voltages in phase A; $\mathbf{MMC}_2$ **side:** (k) phase voltage in the delta side of the Y/Δ transformer, (l) phase current in the delta side of the Y/Δ transformer, (m) active and reactive power, and (n) upper arm SM capacitor voltages in phase A.

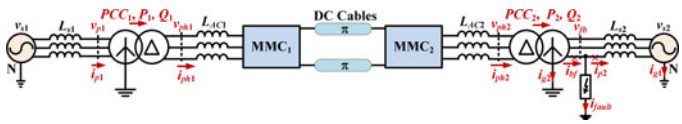

Fig. 17. Inverter-side SLG fault in case 1($\mathbf{MMC}_2$ side).

voltage become balanced, and the amplitude of i_{ph1} goes back to its rated value after the dc voltage recovers. The active and reactive power in the rectifier side is given in Fig. 16(h). Disconnection of SLG fault not only eliminates the large double-line frequency power ripples, but also enables rated power generation at PCC_1 after $t = 0.85$ s. In addition, in spite of a temporary overshoot and oscillation, SPS reduces the negative-sequence current [see Fig. 16(i)]. As illustrated by Fig. 16(j)–(n), due to the fault isolation, capacitor voltages of SMs in the MMC_1 and MMC_2 stations, together with the inverter-side phase current, are regulated to their rated values after a transient process. Furthermore, the active and reactive power generated by MMC_2 tracks its reference in less than two fundamental cycles when the fault is cleared.

2) SLG Fault Occurs in the Inverter Side: Fig. 17 shows the circuit diagram with an SLG fault in the grid side of $\mathbf{MMC}_2$. Fig. 18 shows the dc voltages and their spectrum in the rectifier and inverter stations.

As can be observed, the power loss in the inverter side leads to an abrupt dc voltage increase when the SLG fault occurs, but thanks to the unaffected rectifier control, the dc voltage goes back to its rated value after 0.1 s. Furthermore, the double-line ripple in the inverter-side dc-side voltage is reduced from 24.93

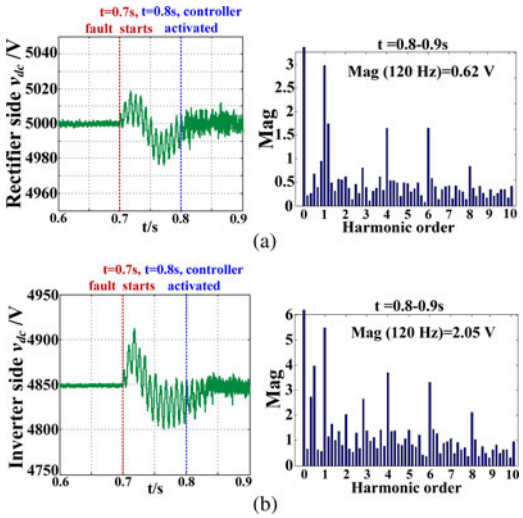

Fig. 18. DC voltage and its spectrum with an SLG fault in case 1 ($\mathbf{MMC}_2$ side). (a) MMC_1 side dc voltage and its spectrum (b) $\mathbf{MMC}_2$ side dc voltage and its spectrum.

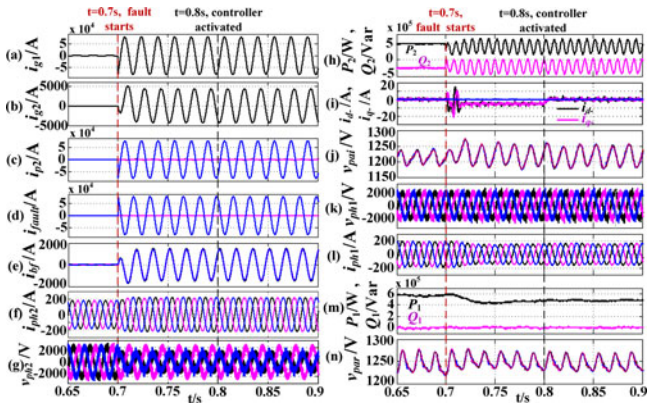

Fig. 19. Simulation waveforms of the studied system under an SLG fault in case 1 ($\mathbf{MMC}_2$ side). $\mathbf{MMC}_2$ **side:** (a) ac grid ground current, (b) transformer primary side ground current, (c) phase currents after the fault point, (d) fault current, (e) phase currents before the fault point, (f) phase current in the delta side of the Y/Δ transformer, (g) phase voltage in the delta side of the Y/Δ transformer, (h) active and reactive power, (i) negative-sequence current components, and (j) upper arm SM capacitor voltages in phase A; $\mathbf{MMC}_1$ **side:** (k) phase voltage in the delta side of the Y/Δ transformer, (l) phase current in the delta side of the Y/Δ transformer, (m) active and reactive power, and (n) upper arm SM capacitor voltages in phase A.

to 2.05 V when the dc voltage suppression control is activated. In addition, the second-order ripple in the rectifier side dc voltage drops from 8.5 to 0.62 V. It is interesting that the dc voltage ripple is attenuated greatly by the dc cables, and if controllers with high bandwidth are adopted, the output voltage distortion in the healthy converter station can be quite small, thus the constant active power control may not be necessary in some applications.

Fig. 19 illustrates the corresponding ac side waveforms. With the same grounding connection, $\mathbf{MMC}_2$ suffers the same current distribution ($i_{g1}, i_{g2}, i_{p2},$ and i_{bf}) in the primary side as that in Fig. 14.

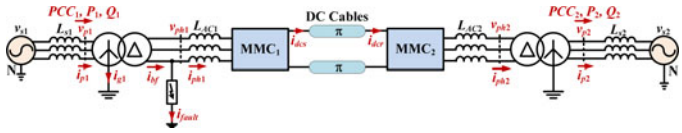

Fig. 20. Rectifier side SLG fault in case 2.

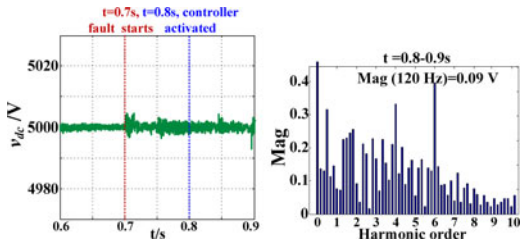

Fig. 21. DC voltage and its spectrum with SLG fault in case 2 (MMC_1 side).

To track the power references, the magnitude of the delta side current in $\mathbf{MMC}_2$ (i_{ph2}) increases to its maximum value of 222 A. Since the phase current is still not high enough to compensate the power loss caused by the SLG fault, both active and reactive power generation (P_2 and Q_2) at PCC2 decrease. Meanwhile, power absorption (P_1 and Q_1) from the ac grid v_{s1} is reduced until a new power balance is achieved to maintain the dc voltage, thus the rectifier side phase current i_{ph1} decreases proportionally.

As shown in Fig. 19(i), the negative-sequence component in i_{ph2} is effectively minimized by the negative-sequence current controller. With a stable dc voltage, SMs' capacitor voltages in both MMC_1 and MMC_2 are well balanced and regulated around their rated values. Moreover, the capacitor voltage ripple in MMC_2 increases because of higher i_{ph2}, while that in MMC_1 decreases due to lower i_{ph1}. To protect the system from large fault current, the SLG fault should be isolated by opening the faulted phase from both sides, as represented by red crossings in Fig. 17. Without the faulted phase, all currents and voltages, except those in the primary side of Y/Δ transformer in MMC_2, present the same performance as normal conditions. Due to the space limitation, the detailed waveforms are not repeated here.

D. Fault-Tolerant Operation With Designed Controllers in Case 2

The circuit diagram with SLG fault in the secondary side of Y/Δ transformer at MMC_1 station is given in Fig. 20. SPWM instead of SVM scheme is employed in this simulation because of the neutral point displacement during the fault.

With the normal primary side voltage v_{p1}, the magnitude of the phase voltage in the converter side v_{ph1} is clamped to its line-to-line voltage, which enables constant v_d and v_q under the *dq* coordinates. Since the SLG fault in this case mainly introduces a zero-sequence component in the converter-side phase current i_{ph1}, the normal dc voltage control is unaffected by the SLG fault, as demonstrated in Fig. 21.

Because of the small negative-sequence current, a double-line frequency ripple with a magnitude of only 0.41 V is observed in

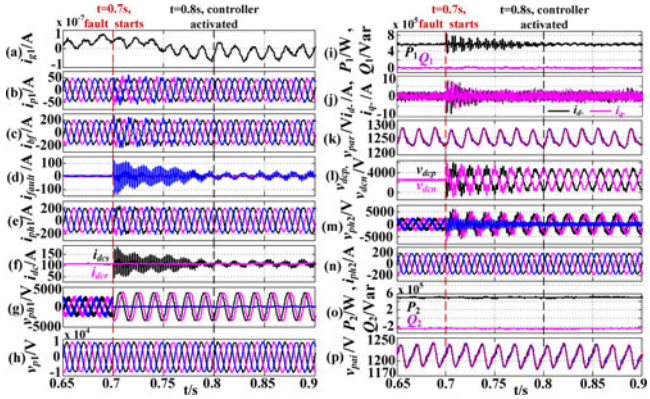

Fig. 22. Simulation waveforms of the studied system under an SLG fault in case 2 (MMC_1 side). $\mathbf{MMC}_1$ **side:** (a) ac grid ground current, (b) phase current in the Y side of the Y/Δ transformer, (c) phase currents before the fault point, (d) fault current, (e) phase current in the delta side of the Y/Δ transformer, (f) dc bus currents in the sending and receiving end, (g) phase voltage in the delta side of the Y/Δ transformer, (h) phase voltage in the Y side of the Y/Δ transformer, (i) active and reactive power, (j) negative-sequence current components, (k) upper arm SM capacitor voltages in phase A; and (l) dc buses to ground voltage, $\mathbf{MMC}_2$ **side:** (k) phase voltage in the delta side of the Y/Δ transformer, (l) phase current in the delta side of the Y/Δ transformer, (m) active and reactive power, and (n) upper arm SM capacitor voltages in phase A.

the dc voltage. When the dc voltage ripple suppression control is activated at 0.8 s, the dc-voltage ripple is further reduced to 0.09 V in less than two fundamental cycles.

As shown in Fig. 22(a)–(c), without a zero-sequence current path, no ground current flows into the primary side ($i_{g1} = 0$) and only positive- as well as negative-sequence currents appear in i_{bf} and i_p. The waveforms of dc currents in the sending end i_{dcs} (rectifier side) and receiving end i_{dcr} (inverter side) are presented in Fig. 22(f). A detailed comparison among these two currents and ground current i_{fault} reveals that i_{fault} is forced to flow into the ground through the capacitance of the dc cables. Moreover, the oscillation in i_{fault}, caused by resonance among inductors and distributed capacitors, is gradually damped down [see Fig. 22(d)].

Fig. 22(g) and (h) gives the converter- and grid-side phase voltage in the rectifier station, respectively. As mentioned previously, during an SLG fault, the grid-side phase voltage v_{p1} keeps balanced, while the magnitude of the converter-side phase voltage v_{ph1} in the other two healthy phases equals to the value of the line-to-line voltage in this case. After the oscillation in i_{fault} damps down and the controllers start to operate at 0.8 s, the positive-sequence component in the converter-side phase current i_{ph1} stays at 181 A, and the negative- and zero-sequence components are reduced to around 0.5 and 6 A, respectively.

In order to eliminate the zero-sequence current, a zero-sequence voltage with its magnitude equal to the positive sequence one needs to be generated by the converters. However, this will affect the positive-sequence power regulation and lead to potential system instability. To deal with this issue, the zero-sequence voltage feedforward control is not applied and the output of zero-sequence current control should be limited properly in this case. According to (6)–(8), an additional second-order dc-voltage ripple will be generated by these zero-sequence current

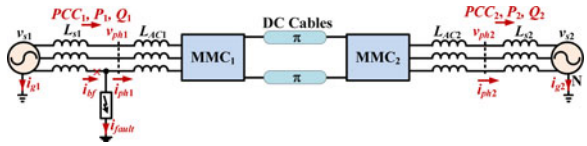

Fig. 23. Rectifier side SLG fault in case 3.

and output voltage. However, compared to case 1, the product of them is much smaller than that formed by the negative-sequence voltage and the positive-sequence current, thus contributing to a lower dc-voltage ripple.

Although the average value maintains, the active power P_1 in the rectifier side still has some double-line frequency ripple caused by the zero-sequence voltage and current, but the magnitude of this ripple is low enough to be neglected after 0.85 s [see Fig. 22(j)]. On the other hand, as shown in Fig. 22(k), the negative-sequence current is well suppressed by the negative-sequence current control activated at $t = 0.8$ s.

Different from the previous cases, the SLG fault has no obvious impact on capacitor voltages in both rectifier and inverter sides due to the stable dc voltage and phase currents [see Fig. 22(k) and (p)]. However, the positive and negative dc bus to ground voltage becomes sinusoidal [see Fig. 22(l)]. That is why the converter-side phase voltage in the inverter station has the same shape as that in the rectifier station [see Fig. 22(m)]. In spite of the phase voltage variation caused by the floating ground potential, the line-to-line voltage is the same as that under normal conditions, which enables rated active and reactive power generation in the inverter side (P_2 and Q_2) as long as the phase current i_{ph2} remains balanced and well regulated.

Since the fault current is relatively small and performance degradation is also low, no SPS is adopted in this case. Due to the symmetrical fault characteristics and space limitation, waveforms with SLG fault in the inverter station are not duplicated.

It should be mentioned that different from the dc fault, the positive and negative dc buses are connected to ground through stray capacitors, and the stray capacitance of the dc cable is normally hundreds of nF/km. Thus, the inrush current caused by its stored energy discharging during the transient fault period is limited. Moreover, the stray capacitance dominates the short-circuit loop impedance, which may contribute to a small short-circuit current in the steady state.

The above analysis, however, is valid only when the stored energy of the dc-cable capacitance is low. If a long dc cable is used, and/or additional dc capacitors are adopted for dc side grounding, a significant fault current may be created by the secondary SLG fault, making the continuous operation of MMC impossible. Furthermore, in ultrahigh dc-voltage applications, even though the stray capacitance is small, its stored energy may also be high enough to produce a destructive fault current and force the system to completely stop during the fault.

E. Fault-Tolerant Operation With Designed Controllers in Case 3

Fig. 23 shows the circuit diagram with an SLG fault occurring in a transformerless application, and the corresponding

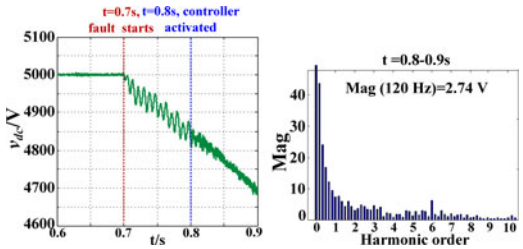

Fig. 24. DC voltage and its spectrum with SLG fault in case 3 (MMC_1 side).

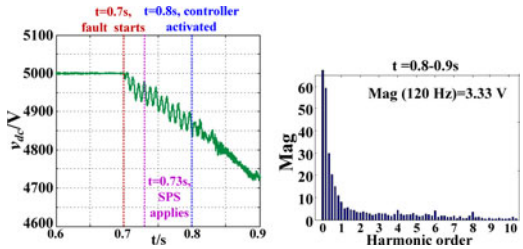

Fig. 26. DC voltage with SPS in case 3 (MMC_1 side).

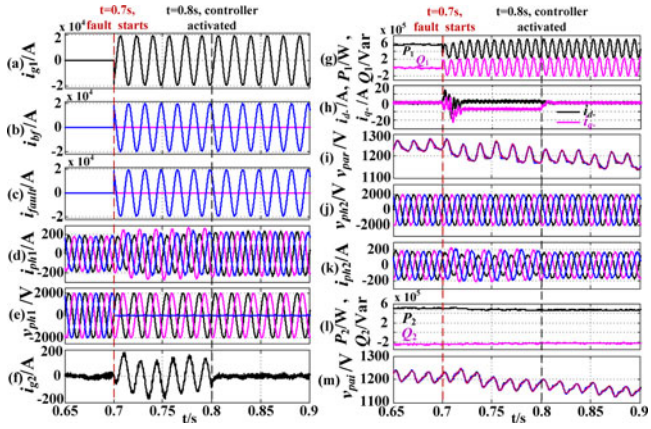

Fig. 25. Simulation waveforms of the studied system under SLG fault in case 3 ($\mathbf{MMC}_1$ side). $\mathbf{MMC}_1$ **side:** (a) ac grid ground current, (b) grid-side phase currents, (c) fault current, (d) converter-side phase currents, (e) converter-side phase voltage, (g) active and reactive power, (h) *d*- and *q*-axis negative-sequence current, and (j) upper arm SM capacitor voltages in phase A; $\mathbf{MMC}_2$ **side:** (f) ac grid ground current (j) converter-side phase voltage, (k) converter-side phase current, (m) active and reactive power, and (n) upper arm SM capacitor voltages in phase A.

simulation waveforms at MMC_1 and MMC_2 are presented in Figs. 24 and 25, respectively.

Being grounded in both ac grids, the SPWM scheme is applied to avoid the ground current caused by the common mode voltage generated by the SVM scheme. Additionally, the line-to-line voltage of the ac grid v_{s1} is adjusted from 10 to 2.5 kV to match the converter-side voltage in the previous cases.

The dc voltage drops gradually because of the phase current limitation. The magnitude of double-line frequency ripple in the dc voltage decreases from 23.36 to 2.74 V (see Fig. 24) in about one fundamental cycle when the designed control is activated.

Being solid grounded, the ac grid u_{s1} produces a significant ground current i_{g1}, which mainly flows in the loop between the ground of u_{s1} and the SLG fault. As shown in Fig. 25(a)–(c), the faulted phase (phase C) currents in i_{p1} and i_{bf} are close to i_{g1}, while the other two healthy phase currents are clamped by the converter-side phase current i_{ph1}. To track the dc voltage reference, the magnitude of i_{ph1} grows from 181 to 222 A, and the apparent unbalanced components in i_{ph} disappear after the designed control works at $t = 0.8$ s [see Fig. 25 (d)].

Before 0.8 s, the ground current i_{g2} flowing into the neutral point of the ac grid v_{s2} in the $\mathbf{MMC}_2$ side is nonzero. This indicates that a zero-sequence current is transferred from $\mathbf{MMC}_1$ to $\mathbf{MMC}_2$, which is different from the previous cases [see Fig. 25(f)].

Due to the voltage drop at PCC1, active power generation of the rectifier reduces to $2P_{\mathrm{rated}}/3$ and large double-line frequency ripple is observed in both active and reactive power [see Fig. 25(g)]. The negative-sequence currents i_d^- and i_q^- drop to zero in less than one cycle after $t = 0.8$ s [see Fig. 25(h)]. In the inverter station, the converter-side phase current i_{ph2} becomes balanced ($i_{g2} \approx 0$) with negative- and zero-sequence current control operating at 0.8 s. Compared to case 1, with no voltage clamp provided by the Y/Δ transformer, the faulted phase voltage drops to zero, resulting in a more asymmetrical phase current. On the other hand, the converter-side phase current instead of its positive-sequence component is directly used for power and/or voltage control, which helps to mitigate the negative-sequence current instantaneously when the fault happens. Thus, i_d^- and i_q^- in this case are still less than 10 A.

Moreover, as a result of lower power generation in the rectifier side, the magnitude of i_{ph2} decreases from 163.3 to 150.2 A [see Fig. 25(k)]. This in turn induces a lower power generation at PCC2 [see Fig. 25(l)]. The capacitor voltages of SMs in both stations gradually decrease below their rated values, and their ripples proportionally vary with the magnitude of the corresponding phase currents [see Fig. 25(i) and (m)]. Different from case 2, the zero-sequence component of v_{ph1} in this case is low enough to be fully compensated by the converters.

SPS is also applied for system protection and continuous load energy supply. Considering the operating principle of a circuit breaker, SPS should be only activated when fault currents are larger than the preset tripping values, e.g., $I_{\mathrm{dref}}\_\mathrm{max}$ in this paper. Therefore, only the grid-side faulted phase is tripped to block the large ground current, as represented by the red cross mark in Fig. 23. Furthermore, if the converter-side faulted phase is also tripped, the controllers cannot work well since it is impossible to achieve balanced phase current with only two phases.

The associated dc voltage and the ac waveforms adopting SPS are presented in Figs. 26 and 27, respectively. With a fault connected in the converter side, the dc voltage keeps dropping, even after the SPS operates at $t = 0.73$ s. The double-line frequency dc-voltage ripple decreases from 23.43 to 3.33 V when the proposed control is activated.

The grounding current i_{g1} only consists of the zero-sequence current contained in i_{bf}, and phase C current flows into the fault point and forms i_{fault}. As the grounding current i_{g2} is eliminated after 0.8 s, the amplitude of i_{g1} decreases from 260 to 222 A.

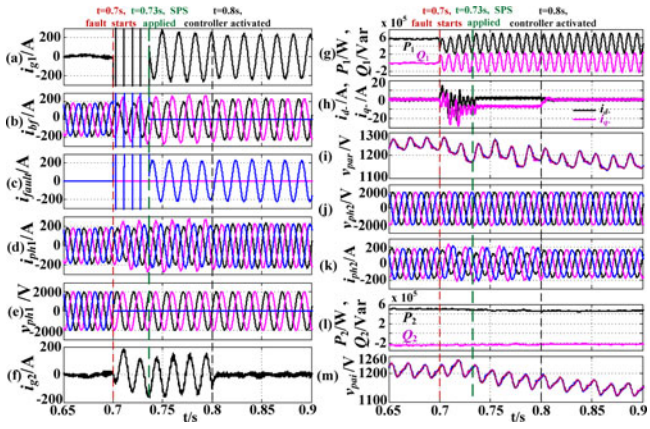

Fig. 27. Simulation waveforms of the studied system under SLG fault with SPS in case 3 (MMC_1 side). MMC_1 **side:** (a) ac grid ground current, (b) grid-side phase currents, (c) fault current, (d) converter-side phase currents, (e) converter-side phase voltage, (g) active and reactive power, (h) negative-sequence current components, and (j) upper arm SM capacitor voltages in phase A; MMC_2 **side:** (f) ac grid ground current (j) converter-side phase voltage, (k) converter-side phase current, (m) active and reactive power, and (n) upper arm SM capacitor voltages in phase A.

The system performance after the fault point, including the converter-side phase voltage and current, active /reactive power generation, capacitor voltages of SMs, etc., is the same as that without SPS. Moreover, the symmetrical operation performance can be obtained with an SLG fault in the inverter side except for successful dc voltage regulation. Hence, no description or waveforms are repeated.

IV. Discussion

Up to this point, the fault-tolerant operation of the MMC-HVDC system under three SLG fault conditions with and without SPS has been investigated. The purpose of this section is to summarize its characteristics under each case and their potential issues.

Case 1 (SLG Fault Occurs in the Primary Side of the Y/Δ Transformer): The dc voltage and capacitor voltages of SMs can be well regulated with the SLG fault occurring in the inverter side. In contrast, if it occurs in the rectifier side, additional control strategies and/or communication between two converter stations is required to maintain the dc voltage. In both situations, the designed controllers help to mitigate the dc-voltage ripple and negative-sequence current effectively. Furthermore, the active and reactive power transferred by the HVDC system is determined by the current limitation (power rating) of the converter stations and/or overload capability of the dc cables. Rated power generation is impossible if the maximum current is less than $3I_{\mathrm{rated}}/2$, and vice versa.

On the other hand, if SPS is adopted, the desirable performance including rated output power capability, stable dc voltage, and balanced phase currents in the converter sides, etc., can be obtained under SLG fault conditions. The only issue is that the unbalanced grid-side current in the faulted station is inevitable if the faulted phase is cut from both sides.

Case 2 (SLG Fault Occurs in the Secondary Side of the Y/Δ Transformer): In this case, despite oscillations which are slowly damped down, the rated output power and balanced capacitor voltages can be achieved at both converter stations as long as the dc side is grounded through high impedances. Although the ground potential floating leads to abnormal dc bus to ground voltage and converter-side phase voltage in the other station, the voltage difference between the two dc buses and line-to-line voltage stays the same. In addition, by using the implemented control scheme, the low negative-sequence current in the faulted station can be easily eliminated, while the compensation of zero-sequence current is still quite difficult with limited output power capacity.

Case 3 (SLG Fault Occurs in a Transformerless System): In order to ensure normal operation of controllers, the faulted phase with SLG fault is only cut from the grid side. Therefore, other than SPS, additional high-speed communication between the two stations is required to stop the dc voltage from dropping during an SLG fault. A possible solution is exchanging the operation modes of the two converters, i.e., MMC_1 controls the active and reactive power, while MMC_2 regulates the dc voltage during the fault period. Furthermore, load shedding, as a compromised but effective way, can also be used here. With the power reference of the inverter reduced to $(2I_{\mathrm{dref\_max}}/3I_{\mathrm{drated}}) \times P_{\mathrm{rated}}$, the stable dc voltage can be achieved with the phase current magnitude of $I_{\mathrm{dref\_max}}$, and the rated phase current can be obtained with power reference of 2/3 P_{rated}.

Different from cases 1 and 2, the zero-sequence current caused by an SLG fault in one station will be transferred to the other station and cause the grounding current to flow into the neutral point of both ac grids. Fortunately, the zero- as well as the negative-sequence current can be fully suppressed by the designed controllers.

In order to achieve small grounding current and low performance degradation in cases 2 and 3, large dc-side grounding impedances can be used. However, personnel safety, fault detection, and protection are a concern in such systems.

Although the current magnitude may vary case by case due to different grounding types, transformer connections, dc-voltage regulation schemes, and cable overload capability, etc., the fault characteristics and operating principle should be the same as that analyzed above. The two converter stations could compensate the negative- and/or zero-sequence currents separately, while to avoid conflicts between controllers in the two converter stations, only the one suffering an SLG fault is designed to suppress the double-line frequency dc-voltage ripple. Furthermore, the proposed controller and the operation principle will be more effective and important in higher power applications with larger dc voltage ripple and negative/zero-sequence currents.

VII. Conclusion

In order to improve the overall reliability of the MMC-HVDC transmission system, the technical feasibility of maintaining its operation performance with/without SPS under the SLG fault is investigated in this paper. The fault characteristics and

controllers' design are discussed. Simulation results with the proposed controllers are presented under different fault cases. The key points included in this paper could be summarized as follows:

1) Considering positive-, negative-, and zero-sequence components in both arm voltage and current, the phase unit instantaneous power under unbalanced condition has been derived to provide a straightforward insight into the origin of the dc voltage ripple and the circulating current. The zero-sequence instantaneous power forms the double-line frequency dc-voltage ripple, while the negative- and zero-sequence power leads to the circulating current under unbalanced conditions.
2) The proposed quasi-PR dc-voltage ripple suppression control, together with negative- and/or zero-sequence current control, enables the HVDC system to achieve the low dc-voltage ripple as well as balanced ac line currents at both converter stations under different SLG faults. Moreover, only the dc voltage is required to be measured, and thus, no extra hardware is introduced for the controller implementation.
3) The fault characteristics of an HVDC system in three possible fault cases, including the dc voltage, ground currents, converter-side phase currents, and power output capability, etc., are analyzed and compared to illustrate the demand of protective devices and a generalized controller.
4) The fault-tolerant operation performance of the HVDC system with/without SPS are discussed and compared in detail to illustrate the merits of SPS.

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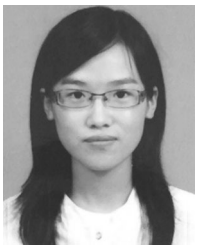

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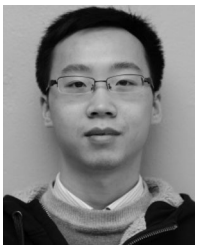

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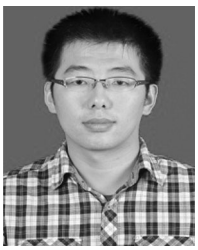

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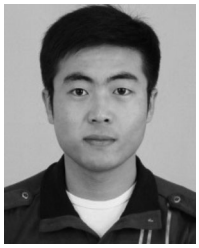

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