# Analysis and Control of Modular Multilevel Converters With Integrated Battery Energy Storage

Michail Vasiladiotis, *Student Member, IEEE*, and Alfred Rufer, *Fellow, IEEE*

***Abstract*—Multilevel converters and battery energy storage systems are key components in present and future medium voltage networks, where an important integration of renewable energy sources takes place. The modular multilevel converter offers the capability of embedding such energy storage elements in a split manner, given the existence of several submodules operating at significantly lower voltages. This paper analyzes such a converter structure under different operating modes. In order to eliminate the low-frequency components of the submodule output currents, the latter are interfaced to the batteries by means of nonisolated dc/dc converters. Control algorithms are developed for the balancing of the battery state of charges and the respective gain limitations are established. Unbalanced grid conditions are also taken into account through the theory of symmetrical components and solutions are proposed. Finally, the development of a down-scaled prototype is described and experimental results are presented.**

***Index Terms*—Active power control, battery energy storage system (BESS), integrated split storage, modular multilevel converter, prototype, state of charge (SoC) balancing, symmetrical components.**

## I. Introduction

THE need of ancillary services, such as load leveling and power buffering, poses a necessity for energy storage system utilization in modern large-scale power systems. Among them, electrochemical technologies such as supercapacitors and batteries are key components offering straightforward solutions. From a power electronics perspective, multilevel converters present significant advantages in the medium voltage and high power range over conventional topologies, attracting therefore the interest of both the academic and industrial worlds. Among them, the most promising concept regards the modular multilevel converter (MMC), which implies the series connection of identical power submodules within a converter branch [1]. The branches can be then configured in several ways, achieving different conversion structures such as ac/dc [1], [2], ac/ac [3]–[5] or even isolated dc/dc [6].

The MMC has been extensively studied during the recent years. A wide range of applications have been considered including HVDC systems [7]–[10], medium-voltage electric drives [11], [12], as well as direct and indirect grid interfaces [13], [14]. The topology-specific features, such as the existence of continuous branch currents, the capacitive nature of the phase legs, the low-output frequency operation in dc/ac drives as well as the submodule capacitor voltage balancing are also implying more advanced modeling, modulation, and control system developments [15]–[24].

An emerging topic regards the use of the MMC family as battery energy storage units. Contrary to utilizing only one central battery on the medium voltage level, aspects such as redundancy and straightforward battery management system (BMS) designs can be fulfilled through a split accumulation concept. The integration of batteries into the submodules of a cascaded H-bridge (CHB) converter has been already studied considerably [25]–[29]. Some works have been also discussing the use of an MMC as an ac/dc structure with embedded storage, with the focus laid on system design [30]–[33]. However, [32] and [33] do not take advantage of the common dc link, which is typically used to feed an external load as shown by [30]. On the other hand [31], proposes the utilization of a single large dc-link battery, which does not benefit from the lower submodule voltage levels. In the authors' view, the MMC-BESS is not to be considered as a strict alternative to the application-specific CHB-based storage unit, but rather as an ac/dc conversion structure with additional energy storage capability.

Several topology-specific issues arise in such an MMC-based storage unit, which need to be overcome. Initially, the submodule implementation using half-bridges implies strong low-frequency currents at their outputs. In order to prevent the latter from flowing into the batteries, passive or active interfaces can be utilized [29]–[31]. The control of the MMC-BESS then becomes different than in typical operation, given the need for handling all possible system power flows. In addition and in several modern battery technologies, a flat curve of state of charge (SoC) is observed as a function of their voltage in a wide regime. This implies the need for a balancing algorithm targeting directly at the SoCs and no longer at the battery voltages [26], [27]. Finally, the operation of such a converter under unbalanced grid conditions poses challenges, since each converter branch is affected in an independent manner unlike conventional three-phase topologies.

This study makes a thorough analysis of the different operating modes that can be encountered in such a three-phase MMC-based BESS featuring a common dc link. As the batteries are interfaced to the converter submodules through nonisolated dc/dc converters, the control problem can be split in two subproblems, voltage and power control. The submodule capacitor voltage control is handled by the dc/dc converters, offering the flexibility to directly manipulate the active power components for a SoC balancing of the batteries. The SoCs are modeled by

Manuscript received October 11, 2013; revised December 16, 2013; accepted January 17, 2014. Date of publication January 28, 2014; date of current version August 26, 2014. Recommended for publication by Associate Editor M. A. Perez.

The authors are with the Laboratory of Industrial Electronics, École Polytechnique Fédérale de Lausanne, 1015 Lausanne, Switzerland (e-mail: michail.vasiladiotis@epfl.ch; alfred.rufer@epfl.ch).

Digital Object Identifier 10.1109/TPEL.2014.2303297

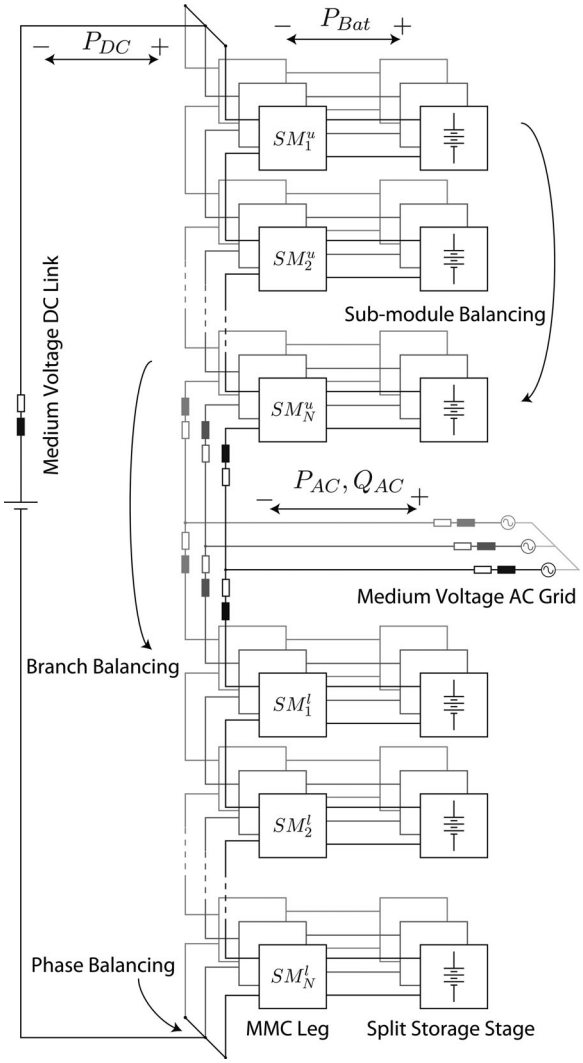


Fig. 1. MMC with integrated battery energy storage elements.

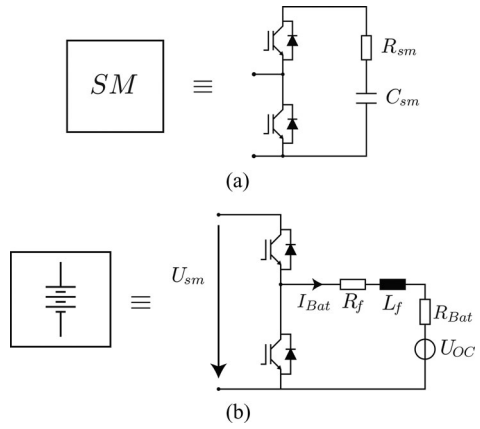


Fig. 2. Implementation of the (a) MMC submodule and (b) the split storage stage based on the indirect active interface (IAI).

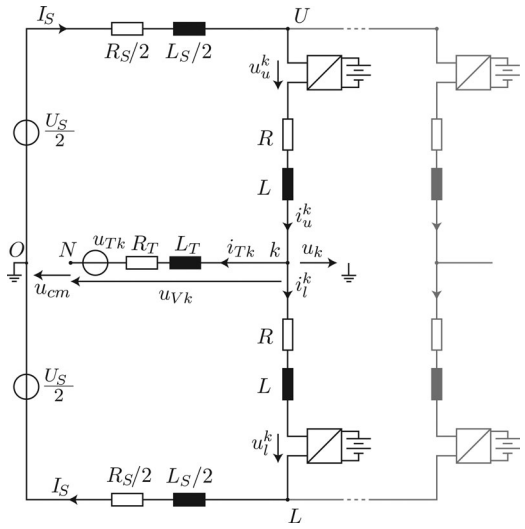


Fig. 3. Multiphase MMC.

first-order transfer functions in all possible unbalance directions, namely submodule, branch, and phase. The limitations of the proportional regulator gains are also derived analytically. Moreover, the operation of such a storage unit under grid asymmetries is investigated and solutions are offered.

This paper is organized as follows. Section II describes the possible operating modes of an MMC with the integrated BESS. In addition, the submodule capacitor voltage problem is treated. Section III explores the degrees of freedom (DOF) for handling active power components independently within the converter in all possible unbalance directions. Section IV discusses the SoC-balancing concept. Finally, Section V describes the development of a laboratory prototype and presents experimental results, leading to Section VI, which concludes the work.

## II. MMCs with the Integrated BESS

### A. Topology Description and Modeling Basics

The three-phase MMC with the integrated BESS is illustrated in Fig. 1. It comprises three parallel-connected phase legs. Each leg consists of two branches, where the midpoint is connected to the ac side handling an amount of active as well as reactive powers, respectively. Each submodule is equipped with a storage element, which serves as an active power port, contrary to a typical MMC case where the average active power in the submodules should be equal to zero. In addition, the phase legs are connected to a common dc link, which can be considered as an additional active power flow port in the studied system. In a typical MMC case, the submodule is implemented by means of a half-bridge, as depicted in Fig. 2(a). This implies that each branch cannot provide negative voltages.

In Fig. 3, a simplified scheme of one converter leg defining all necessary magnitudes is presented. Throughout the remainder of the paper, the following subscripts/superscripts are utilized: $k \in \{a, b, c\}$ referring to the studied phase, $j \in \{u, l\}$ to the upper/lower branches of the same phase leg, and $i \in \{1, 2, \ldots, N\}$ to the submodules of the respective branch.

The so-called circulating current flows through the phase leg and can comprise both dc and ac components. The latter is

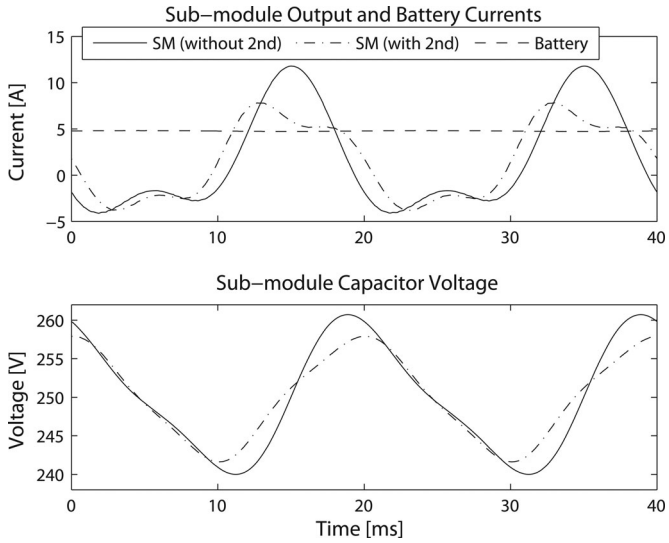


Fig. 4. Average submodule output and battery currents as well as submodule capacitor voltage with and without second-order harmonic injection in the circulating current for voltage ripple reduction.

defined in its general form as

$$i^k_{\rm circ} = \underbrace{I^k_{\rm circ0}}_{I_S/3} + \sum_{n=1}^{\infty} \hat{i}^k_{{\rm circ},n} \cos(n\omega t + \theta_n). \tag{1}$$

Assuming that the branch impedances are symmetrical and therefore the line current splits equally between the upper and lower branches of the same phase leg, the branch currents are defined as

$$i^k_u = \frac{i_{Tk}}{2} + i^k_{\rm circ}, i^k_l = -\frac{i_{Tk}}{2} + i^k_{\rm circ}. \tag{2}$$

A second-harmonic component can be imposed on the circulating current, in order to reduce the maximum energy variation in the submodule capacitors and therefore the capacitive storage requirements [13], [34], [35]. Even in such a case, though, there is still a significant submodule output current variation which should be prevented from flowing into the battery. For this reason, another half-bridge with a filtering inductor serves as the indirect active interface (IAI) between the submodule capacitor and the battery. The latter is shown in Fig. 2(b) together with the battery, which is modeled as a controllable voltage source ($U_{\rm OC}$) in series with an equivalent resistance ($R_{\rm bat}$). The advantage of such a power decoupling is illustrated in Fig. 4. The average submodule output current is depicted together with the respective average battery current, both for the case of pure dc circulating current as well as second-order harmonic injection. The battery current is the same for both cases, even though the harmonic content of the submodule output current is different. The battery current ripple will be limited to the switching harmonics generated by the buck converter, which are now related to the switching frequency, the filter inductance $L_f$, as well as the battery/submodule voltage ratio.

### B. Submodule Capacitor Voltage Balancing

Factors such as losses, practical variations between the submodule capacitances, as well as different battery power demands can lead to divergence from the desired submodule capacitor voltages. Therefore, an individual control of these voltages should take place. The IAI between the submodules and the BESS offers an additional DOF toward such a direction. A typical cascaded outer voltage/inner current loop can be used for voltage balancing from the battery side, similar to the CHB converter-based photovoltaic unit of [36] and the supercapacitive MMC-based traction system of [37]. This section deals with the dimensioning of the control system for the IAI, whose block diagram is given in Fig. 5.

According to the notations of Fig. 2, the respective transfer functions for the current and voltage are given respectively as

$$G^U_S(s) = \frac{1}{sC_{\rm sm}}, \quad G^I_S(s) = \frac{1}{sL_f + R_f}. \tag{3}$$

The inner loop controls the average value of the battery current with the regulator $G^I_R(s)$ given by

$$G^I_R(s) = \frac{1 + sT_{nI}}{sT_{iI}}. \tag{4}$$

The battery voltage is added to the output of the regulator for disturbance rejection purposes. The converter and control hardware nonlinearities and delays are modeled by small time constants according to the pseudocontinuous approach with the associated transfer function $G_{pE}(s)$ [38] as

$$G_{pE}(s) = \frac{1}{1 + sT_{pE}}. \tag{5}$$

The external loop controls the submodule capacitor voltage $U^{kji}_{\rm sm}$ to its reference value $U^*_{\rm sm}$ through a PI controller

$$G^U_R(s) = \frac{1 + sT_{nU}}{sT_{iU}}. \tag{6}$$

A precalculated feed-forward current component $I^{kji}_{ff} = P^{kji*}_{\rm Bat}/U^{kji}_{\rm Bat}$ is added to the output of the regulator for faster response. The latter is based on the power demand of the battery, which is a result of the higher level control functions. In this way, the contribution of the voltage regulator will correspond to a small amount of active power injection in order to compensate for the losses that would cause deviations of the capacitor voltage from its desired value. Since only the average value of the capacitor voltage can be controlled, a low-pass filter has to be added on the voltage measurement of $U^{kji}_{\rm sm}$ in order to reject the low-order harmonic frequency oscillations

$$G^U_f(s) = \frac{1}{1 + sT_f}. \tag{7}$$

The inner current loop is designed according to the magnitude optimum criterion. Therefore, the regulator constants are given as

$$T_{nI} = \frac{L_f}{R_f}, \quad T_{iI} = \frac{2T_{pE}}{R_f}. \tag{8}$$

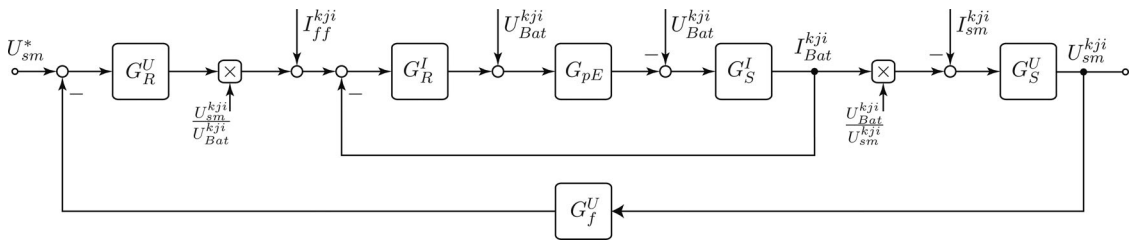


Fig. 5. Cascaded voltage/current control loop for each of the IAIs.

Subsequently, an equivalent transfer function is considered for the closed-loop current control with a time constant of $T_{\rm cl} = 2T_{pE}$, in order to design the external voltage loop. For the latter, the symmetric optimum criterion for systems with integral behavior is utilized. The gains are specified as

$$T_{nU} = 4(T_f + T_{\rm cl}), T_{iU} = \frac{8(T_f + T_{\rm cl})^2}{C_{\rm sm}}. \tag{9}$$

### C. Operation Modes

By exploring Fig. 1, the definition of power flows is at hand. The converter can exchange a specific amount of active and reactive power $P_{\rm AC}$ and $Q_{\rm AC}$ with the three-phase grid, respectively. A fraction of the active power $P_{\rm AC}$ is exchanged with the dc link $(P_{\rm DC})$ and the rest will be exchanged with the three-phase BESS $(P_{\rm Bat})$. Evidently, the following relation holds:

$$P_{\rm AC} = P_{\rm DC} - P_{\rm Bat}. \tag{10}$$

The sign of each power component reveals its direction, considering as positive the one defined by the respective signs of Fig. 1 or equivalently by the current arrows in Fig. 3. An explicit decoupled line and circulating current control implies the ability to regulate independently the average dc power from the ac one. By defining $\varepsilon$ as the ratio $P_{\rm DC}/P_{\rm AC}$, (10) can be written as

$$P_{\rm AC} = \varepsilon P_{\rm AC} - P_{\rm Bat} \Leftrightarrow P_{\rm Bat} = P_{\rm AC}(\varepsilon - 1). \tag{11}$$

Defining the quantities $P^k_{\rm AC}$, $P^k_{\rm DC}$, and $P^k_{\rm Bat}$, (11) is valid on a per-phase level, accordingly. The dc part of the circulating current $I^k_{\rm circ0}$ cannot be used to charge/discharge the batteries, as it is physically transferred to the dc link. The latter can be expressed by

$$I^k_{\rm circ0} = \frac{P^k_{\rm DC}}{U_S} = \frac{\varepsilon P^k_{\rm AC}}{U_S}. \tag{12}$$

The ac part of the branch current, however, multiplied with the branch voltage, transfers the continuous power at the output of the submodules. According to the aforementioned considerations, six different operation modes can be distinguished.

Rectifier operation ($P_{\rm AC} < 0$):

1) Mode I: $P_{\rm AC} = P_{\rm DC} \Rightarrow P_{\rm Bat} = 0$ (idle);
2) Mode II: $|P_{\rm AC}| > |P_{\rm DC}| \Rightarrow P_{\rm Bat} > 0$ (charging);
3) Mode III: $|P_{\rm AC}| < |P_{\rm DC}| \Rightarrow P_{\rm Bat} < 0$ (discharging);

Inverter operation ($P_{\rm AC} > 0$):

1) Mode IV: $|P_{\rm AC}| < |P_{\rm DC}| \Rightarrow P_{\rm Bat} > 0$ (charging);
2) Mode V: $|P_{\rm AC}| > |P_{\rm DC}| \Rightarrow P_{\rm Bat} < 0$ (discharging);
3) Mode VI: $P_{\rm AC} = P_{\rm DC} \Rightarrow P_{\rm Bat} = 0$ (idle).

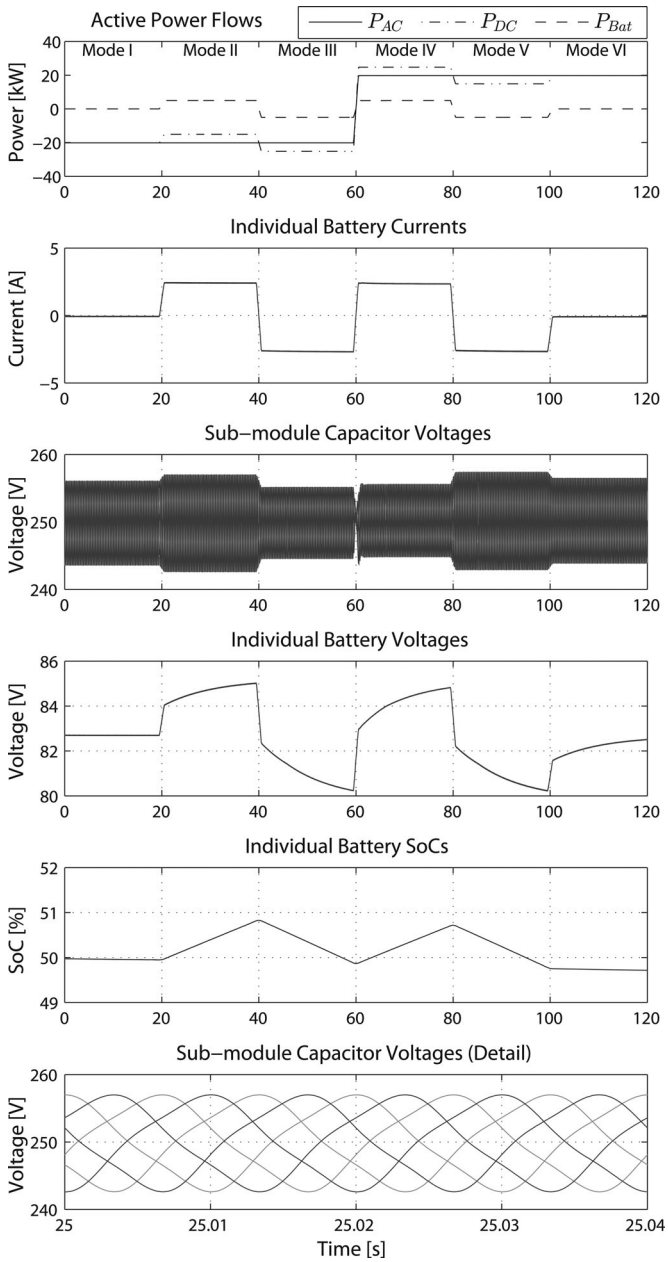


Fig. 6. Simulation results of an MMC-based storage unit for a hypothetical power profile, exploiting all possible operation modes.

In Modes I and VI, the storage system is not used at all, which corresponds to a typical MMC case. Fig. 6 shows the simulation results for the different operation modes of the MMC-based storage unit. The results correspond to a switching-averaged

TABLE I
MAIN SIMULATION SYSTEM PARAMETERS

| Quantity | Value | Comment |
|---|---|---|
| $S_n$ | 20 kVA | Nom. grid power |
| $\tilde{u}_T$ | 230 V | Grid rms phase voltage |
| $N$ | 4 | Sub-modules/branch |
| $U^{sm}_{bat,n}$ | 76.8 V | Nom. battery voltage |
| $Q^{sm}_{bat,n}$ | 1.5 Ah | Nom. battery capacity |
| $C_{sm}$ | 2.3 mF | Sub-module capacitance |
| $U_S$ | 800 V | DC-link voltage |
| $L, R$ | 2.3 mH, 0.2 Ω | Branch inductance/resistance |
| $L_T, R_T$ | 4 mH, 0.5 Ω | Grid inductance/resistance |

model, where all the closed-loop controllers are in action. The parameters are given in Table I. The integrated BESS behaves according to the load demand and the power flow direction. Therefore, it will charge or discharge, in order to meet the active power balance condition of (10). Moreover, it is clear that the average battery current contains a purely continuous component. In addition, the submodule voltage is not affected by the respective variations of the battery voltage. It is noted that the figures depicting the submodule and battery magnitudes consist of 24 waveforms each, which perfectly coincide due to their symmetric operation.

Up to now, an ideal condition of the balanced SoC operation and power consumption between the submodules, branches, and phases of the MMC was considered. However, different factors can lead to divergence of the battery SoCs. Throughout the next sections, the respective balancing control problems will be identified and solved by means of topology-specific DOF exploitation.

## III. INDIVIDUAL POWER CONTROL

### A. Submodule Power Control

The term individual submodule power control refers to the capability of absorbing or injecting different amounts of active power between the submodules of a converter branch. Fig. 7 shows an equivalent circuit of one converter branch. The submodule outputs have been decoupled from their respective inputs. On the ac side, the same current flows through the equivalent voltage sources, which are in series with the fictive split of the branch inductor $L$ and resistance $R$. This means that in order to change the amount of the absorbed or injected power flow by each dc side, the controlled AC submodule voltage has to be changed. This is done by a respective adaptation of the modulation reference for each submodule. A power ratio factor $\beta_{kji}$ is therefore introduced [39] as

$$\beta_{kji} = \frac{\overline{U}^{kji}_{\rm sm}\overline{I}^{kji}_{\rm sm}}{\sum_{i=1}^{N}\overline{U}^{kji}_{\rm sm}\overline{I}^{kji}_{\rm sm}} = \frac{P^{kji}_{sm}}{\sum_{i=1}^{N}P^{kji}_{\rm sm}} \quad \text{with} \quad \sum_{i=1}^{N}\beta_{kji} = 1. \tag{13}$$

The desired pulse width modulation-controlled branch voltage $u^k_j$ is a result of the high-level line and circulating current controllers. By multiplying the latter with its respective power ratio factor $\beta_{kji}$, the total branch active power can be distributed in a desired manner within the different submodules.

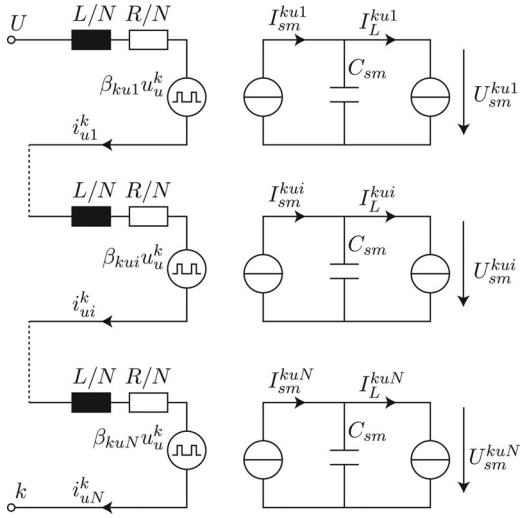


Fig. 7. Equivalent circuit for a decoupled power flow formulation, taking the upper ($u$) branch of the $k$th converter phase as an example.

### B. Phase Power Control

The case of phase power control implies the ability to handle different amounts of active power components from each converter phase without affecting the three-phase grid currents. Similar to a CHB converter with star configuration, the MMC offers the possibility of freely choosing the common-mode voltage $u_{\rm cm}$, which is shown in Fig. 3. Such an action enables the circulation of power within the converter phases, while keeping the total three-phase power transfer unaffected. Similar to its introduction by the authors in [40] and [41] for a STATCOM application and its use by the authors in [26] and [28] for a CHB-BESS, this paper tailors the concept for the MMC case. Grid unbalances are also taken into account for the derivation of the mathematical expressions.

The three-phase voltage and current quantities can be modeled by means of symmetrical components, where the superscripts $p$ and $n$ denote the positive and negative sequences, respectively. In order to achieve a constant power term associated with the common-mode voltage, the latter has to oscillate with the fundamental converter frequency. The $k$th converter phase voltage can be written as

$$u_k = \hat{u}^p_V \cos\left(\omega t + \phi^p_u - \frac{2\pi(m-1)}{3}\right) + \hat{u}^n_V \cos\left(\omega t + \phi^n_u + \frac{2\pi(m-1)}{3}\right) + \hat{u}_{\rm cm}\cos(\omega t + \phi_{\rm cm}) \tag{14}$$

where $m = 1, 2, 3$. The quantity $\phi^p_u$ can be set to zero, assuming that the control system is synchronized with the positive sequence voltage $u^p_V$. The $k$th phase current can also be expressed through the use of the symmetrical components as

$$i_{Tk} = \hat{i}^p_T \cos\left(\omega t + \phi^p_i - \frac{2\pi(m-1)}{3}\right)$$

$$+\hat{i}_T^n \cos\left(\omega t+\phi_i^n+\frac{2\pi(m-1)}{3}\right). \quad (15)$$

The product of the voltage with the current in each converter phase gives the associated phase power components. Only the constant and not the oscillating terms are of interest and are obtained for phases $a$ and $b$ as

$$\begin{aligned}P_{\rm ph}^a =& \underbrace{U_S I_{\rm circ0}^a}_{P_{\rm DC}^a} - \frac{\hat{u}_{\rm cm}\hat{i}_T^p}{2}\cos(\phi_{\rm cm}-\phi_i^p)\\ &- \frac{\hat{u}_{\rm cm}\hat{i}_T^n}{2}\cos(\phi_{\rm cm}-\phi_i^n) - \frac{\hat{u}_V^p\hat{i}_T^n}{2}\cos\phi_i^n\\ &- \frac{\hat{u}_V^n\hat{i}_T^p}{2}\cos(\phi_u^n-\phi_i^p)\\ &- \underbrace{\frac{\hat{u}_V^p\hat{i}_T^p}{2}\cos\phi_i^p - \frac{\hat{u}_V^n\hat{i}_V^n}{2}\cos(\phi_u^n-\phi_i^n)}_{\overline{P}_{\rm 3ph}} \quad (16)\end{aligned}$$

$$\begin{aligned}P_{\rm ph}^b =& \underbrace{U_S I_{\rm circ0}^b}_{P_{\rm DC}^b} - \frac{\hat{u}_{\rm cm}\hat{i}_T^p}{2}\cos\left(\phi_{\rm cm}-\phi_i^p-\frac{4\pi}{3}\right)\\ &- \frac{\hat{u}_{\rm cm}\hat{i}_T^n}{2}\cos\left(\phi_{\rm cm}-\phi_i^n-\frac{2\pi}{3}\right) - \frac{\hat{u}_V^p\hat{i}_T^n}{2}\cos\left(\phi_i^n-\frac{2\pi}{3}\right)\\ &- \frac{\hat{u}_V^n\hat{i}^p}{2}\cos\left(\phi_u^n-\phi_i^p-\frac{2\pi}{3}\right)\\ &- \underbrace{\frac{\hat{u}_V^p\hat{i}_T^p}{2}\cos\phi_i^p - \frac{\hat{u}_V^n\hat{i}_T^n}{2}\cos(\phi_u^n-\phi_i^n)}_{\overline{P}_{\rm 3ph}}. \quad (17)\end{aligned}$$

For the definition of $u_{\rm cm}$ the two expressions are adequate, since the third phase is not forming an independent equation:

$$\begin{cases}\underbrace{P_{\rm Bat}^a - P_{\rm ph}^{a*} - \alpha_1}_{\Delta P_{\rm ph}^a} = \hat{u}_{\rm cm}\alpha_2\cos\phi_{\rm cm} + \hat{u}_{\rm cm}\alpha_3\sin\phi_{\rm cm}\\ \underbrace{P_{\rm Bat}^b - P_{\rm ph}^{b*} - \beta_1}_{\Delta P_{\rm ph}^b} = \hat{u}_{\rm cm}\beta_2\cos\phi_{\rm cm} + \hat{u}_{\rm cm}\beta_3\sin\phi_{\rm cm}.\end{cases} \quad (18)$$

The coefficients $\alpha_{1-3}$ and $\beta_{1-3}$ are the functions of the phase voltage and current positive and negative sequence components are given as

$$\alpha_1 = \frac{\hat{u}_V^p\hat{i}_T^n}{2}\cos\phi_i^n + \frac{\hat{u}_V^n\hat{i}_T^p}{2}\cos(\phi_u^n-\phi_i^p)$$

$$\alpha_2 = \frac{\hat{i}_T^p}{2}\cos\phi_i^p + \frac{\hat{i}_T^n}{2}\cos\phi_i^n, \quad \alpha_3 = \frac{\hat{i}_T^p}{2}\sin\phi_i^p + \frac{\hat{i}_T^n}{2}\sin\phi_i^n$$

$$\beta_1 = \frac{\hat{u}_V^p\hat{i}_T^n}{2}\cos\left(\phi_i^n-\frac{2\pi}{3}\right) + \frac{\hat{u}_V^n\hat{i}_T^p}{2}\cos\left(\phi_u^n-\phi_i^p-\frac{2\pi}{3}\right)$$

$$\beta_2 = \frac{\hat{i}_T^p}{2}\cos\left(\phi_i^p+\frac{4\pi}{3}\right) + \frac{\hat{i}_T^n}{2}\cos\left(\phi_i^n+\frac{2\pi}{3}\right)$$

$$\beta_3 = \frac{\hat{i}_T^p}{2}\sin\left(\phi_i^p+\frac{4\pi}{3}\right) + \frac{\hat{i}_T^n}{2}\sin\left(\phi_i^n+\frac{2\pi}{3}\right).$$

The solution to the system is given similar to that in [40] by

$$\begin{aligned}\phi_{\rm cm} &= \arctan\left(\frac{\Delta P_{\rm ph}^a\beta_{2S} - \Delta P_{\rm ph}^b\alpha_{2S}}{\Delta P_{\rm ph}^b\alpha_{3S} - \Delta P_{\rm ph}^a\beta_{3S}}\right)\\ \hat{u}_{\rm cm} &= \frac{\Delta P_{\rm ph}^a}{\alpha_{2S}\cos\phi_{\rm cm} + \alpha_{3S}\sin\phi_{\rm cm}}. \quad (19)\end{aligned}$$

For a balanced three-phase system, where no negative sequence component exists and therefore $\alpha_1 = \beta_1 = 0$, the solution becomes

$$\begin{aligned}\phi_{\rm cm} &= \phi_i^p - \theta = \phi_i^p - \arctan\left[\frac{2\Delta P_{\rm ph}^b/\Delta P_{\rm ph}^a + 1}{\sqrt{3}}\right]\\ \hat{u}_{\rm cm} &= -\frac{2\Delta P_{\rm ph}^a}{\hat{i}^p\cos\theta}. \quad (20)\end{aligned}$$

### C. Branch Power Control

A third balancing direction exists in the MMC case. It regards the two branches within the same phase leg, which is also shown in Fig. 1. A power transfer between the two branches should take place, without however disturbing either the ac or the dc sides. Such an action is possible through the injection of a circulating current component with a fundamental frequency and the same angle with the phase voltage [18], [42]. The constant power difference between the two branches of the same $k$th phase leg will then become as follows:

$$\begin{aligned}\Delta P_{\rm br}^k &= -\hat{i}_{\rm bal}^k\hat{u}_V - \hat{i}_{\rm bal}^k\hat{u}_{\rm cm}\cos\phi_{\rm cm}\\ &= -\hat{i}_{\rm bal}^k\left(\hat{u}_V + \hat{u}_{\rm cm}\cos\phi_{\rm cm}\right). \quad (21)\end{aligned}$$

Therefore for a given amount of power difference $\Delta P_{\rm br}^k$ between the branches of the same phase leg, a circulating current amplitude is associated as

$$\hat{i}_{\rm bal}^k = -\frac{\Delta P_{\rm br}^k}{(\hat{u}_V + \hat{u}_{\rm cm}\cos\phi_{\rm cm})}. \quad (22)$$

This action implies that if different amounts of balancing powers are needed within the three phase legs, different ac circulating currents will be injected and therefore the dc-link current will no longer be a pure dc. This is something not acceptable when used for a SoC-balancing control, given the fact that the time that the injection lasts will be in the order of minutes, due to the high battery time constant. Therefore and according to [18], for each phase-leg circulating current injection, a respective injection in the other two phases should take place. The other two components will be orthogonal to the phase voltages, in order to deliver only reactive power to the legs. In addition, their amplitude should be chosen, so as to cancel out between the three phases and not cause any ac components to the dc link. The final branch balancing circulating currents can be therefore chosen

as

$$\begin{pmatrix} i^a_{\rm bal} \\ i^b_{\rm bal} \\ i^c_{\rm bal} \end{pmatrix} = \begin{pmatrix} \cos\omega t & -\frac{1}{\sqrt{3}}\sin\omega t & \frac{1}{\sqrt{3}}\sin\omega t \\ \frac{1}{\sqrt{3}}\sin\left(\omega t-\frac{2\pi}{3}\right) & \cos\left(\omega t-\frac{2\pi}{3}\right) & -\frac{1}{\sqrt{3}}\sin\left(\omega t-\frac{2\pi}{3}\right) \\ -\frac{1}{\sqrt{3}}\sin\left(\omega t+\frac{2\pi}{3}\right) & \frac{1}{\sqrt{3}}\sin\left(\omega t+\frac{2\pi}{3}\right) & \cos\left(\omega t+\frac{2\pi}{3}\right) \end{pmatrix} \begin{pmatrix} \hat{i}^a_{\rm bal} \\ \hat{i}^b_{\rm bal} \\ \hat{i}^c_{\rm bal} \end{pmatrix}. \quad (23)$$

### D. Operation Under Grid Unbalances

When a voltage unbalance occurs in the three-phase ac side and the currents are controlled to be perfectly symmetrical (negative sequence-free), each phase cannot provide the same amount of active power. In the MMC-BESS case, this would mean that the batteries can no longer be charged or discharged with the same rate, something that would cause an unbalance in the battery SoCs. In order to avoid this, a common-mode voltage injection can take place with the objective of keeping a constant power flow throughout the three converter phase legs. It is noted that a grid unbalance does not affect the power distribution between the branches of the same phase leg [44].

The simulation results for such a scenario are illustrated in Fig. 8. Initially, the system is operating in symmetrical conditions and each phase absorbs the same amount of active power. At $t = 20$ ms, a phase-to-ground fault takes place with a severity of 50% phase loss. The three-phase currents are controlled to be perfectly symmetrical through the use of two control loops in the rotating reference frame, in conjunction with a Decoupled Synchronous Reference Frame algorithm for symmetrical component identification and synchronization with the three-phase unbalanced network [43]. When no common-mode voltage component is used, the three phases obviously deliver different amounts of mean active powers. At $t = 70$ ms, the injection of $u_{\rm cm}$ takes place according to (19), making the three-phase delivered powers converge to the same value.

It is noted that such an action is preferable when the target is to avoid the SoC unbalance within the phases. However, the dc-link power in such a case remains unaffected and obviously reduced because of the network asymmetry. Alternatively, it can be chosen to use the BESS of a certain phase to cover a dc power demand, when the ac grid cannot support it during a faulty condition.

## IV. SoC Balancing

The concepts developed in the previous section can be utilized for achieving the balancing of the battery SoCs in a closed-loop manner. In order to achieve this, the explicit transfer functions relating the SoC with the amount of charging/discharging power need to be derived. The SoCs can be modeled as first-order systems with integral behavior. Assuming a submodule battery nominal capacity of $Q^{\rm sm}_{{\rm bat},n}$ and nominal voltage of $U^{\rm sm}_{{\rm bat},n}$, the respective transfer functions for the submodule, phase and branch directions are obtained as

$$\text{SoC}_{\rm sm} = \frac{i^{\rm sm}_{\rm bat}\cdot 100}{s\cdot Q^{\rm sm}_{{\rm bat},n}} = \frac{p^{\rm sm}_{\rm bat}\cdot 100}{s\cdot U^{\rm sm}_{{\rm bat},n} Q^{\rm sm}_{{\rm bat},n}} = \frac{p^{\rm sm}_{\rm bat}\cdot 100}{s\cdot E^{\rm sm}_{{\rm bat},n}} \quad (24)$$

$$\text{SoC}_{\rm ph} = \frac{p^{\rm ph}_{\rm bat}\cdot 100}{s\cdot E^{\rm ph}_{{\rm bat},n}} = \frac{p^{\rm ph}_{\rm bat}\cdot 100}{s\cdot 2NE^{\rm sm}_{{\rm bat},n}} \quad (25)$$

$$\text{SoC}_{\rm br} = \frac{p^{\rm br}_{\rm bat}\cdot 100}{s\cdot E^{\rm br}_{{\rm bat},n}} = \frac{p^{\rm br}_{\rm bat}\cdot 100}{s\cdot NE^{\rm sm}_{{\rm bat},n}}. \quad (26)$$

In all three cases, the SoC is a percentage (%), and the battery nominal energy $E^{\rm sm}_{{\rm bat},n}$ is expressed in (W · s).

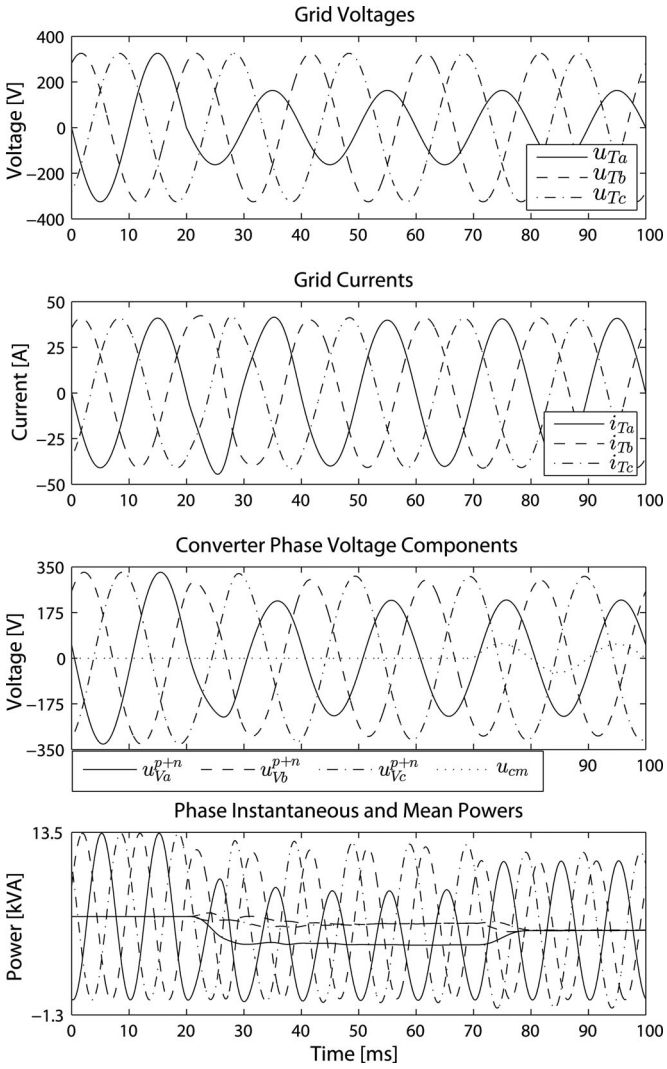


Fig. 8. Simulation results from a battery charging mode under unbalanced grid conditions for the MMC-BESS case: Three-phase grid voltages and respective currents, converter phase components, as well as instantaneous absorbed powers with their respective mean values.

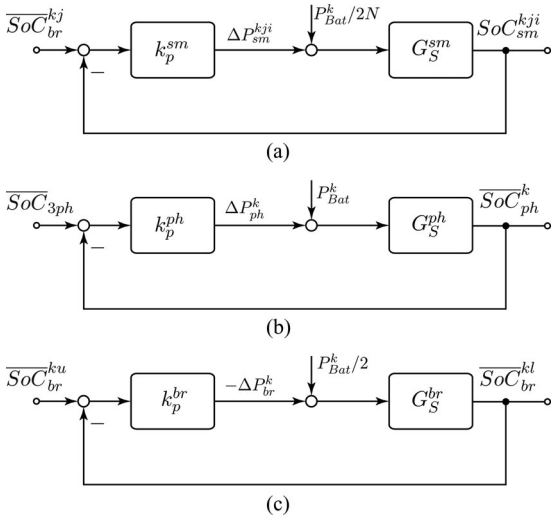


Fig. 9. Block diagrams for (a) submodule, (b) phase, and (c) branch balancing of battery SoCs.

The required active powers of the SoC balancing can be calculated utilizing a proportional controller, such as in the active symmetrization concept presented in [45]. Fig. 9 presents the block diagrams used for the control system design. By setting a desired rise time $t_r$ for the closed-loop control system, the gains are calculated as a function of the nominal submodule battery energy storage $E_{\mathrm{bat},n}^{\mathrm{sm}}$, which represents the plant time constant

$$k_p^{\mathrm{sm}} = \frac{E_{\mathrm{bat},n}^{\mathrm{sm}}}{100 \cdot t_r^{\mathrm{sm}}} \ln 9, \quad k_p^{\mathrm{ph}} = \frac{2NE_{\mathrm{bat},n}^{\mathrm{sm}}}{100 \cdot t_r^{\mathrm{ph}}} \ln 9 \quad \text{and}$$
$$k_p^{\mathrm{br}} = \frac{NE_{\mathrm{bat},n}^{\mathrm{sm}}}{100 \cdot t_r^{\mathrm{br}}} \ln 9. \tag{27}$$

Fig. 9 reveals that the submodule, phase and branch powers will consist of two terms: the main power contribution, which is common for all submodules/phases/branches and does not contribute to the unbalance, as well as the balancing power term, which is the result of the closed-loop control. The total SoC will be a result of both terms. It is noted that the sum of all balancing terms in all three directions will have to be zero, in order not to affect the global power transfer. Finally, the rise times are set higher than a respective capacitor voltage balancing loop, as dictated by the significant difference in the system time constants.

### A. Limitations on Gain Selection

The SoC-balancing controller gains have to follow certain constraints, which are linked to the operation and ratings of the converter. These limitations are established in this section. For sake of simplicity, only balanced grid conditions are assumed.

Initially, the phase balancing loop is examined. The maximum achievable common-mode voltage defines the amount of balancing power $\Delta P_{\mathrm{ph}}^{\max}$ that can be utilized for the balancing. This limitation is directly related to the dimensioned branch blocking voltage $u_{\mathrm{br}}^{\mathrm{dim}}$, where the tolerated submodule capacitor voltage variation $k_{\Delta v}$ has to be taken into account [31]. This can be expressed as

$$u_{\mathrm{br}}^{\mathrm{dim}} \geq k_{\Delta v}\left(U_S/2 + u_T^{\max} + u_{\mathrm{cm}}^{\max}\right) \overset{(20)}{\Leftrightarrow} \frac{2\Delta P_{\mathrm{ph}}^{\max}}{\hat{i}_T^p \cos x}$$
$$\leq \frac{Nu_{\mathrm{sm}}^{\mathrm{dim}}}{k_{\Delta v}} - U_S/2 - u_T^{\max} \overset{(27)}{\Leftrightarrow}$$
$$\Leftrightarrow \frac{4NE_{\mathrm{bat},n}^{\mathrm{sm}} \Delta \mathrm{SoC}_{\mathrm{ph}}^{\max} \ln 9}{100 \cdot t_r^{\mathrm{ph}}}$$
$$\leq \left(\frac{Nu_{\mathrm{sm}}^{\mathrm{dim}}}{k_{\Delta v}} - U_S/2 - u_T^{\max}\right) \hat{i}_T^p \cos x,$$
$$x = \arctan\left[\frac{2\left(\frac{\Delta \mathrm{SoC}_{\mathrm{ph}}^{\mathrm{k}+1}}{\Delta \mathrm{SoC}_{\mathrm{ph}}^{\mathrm{k,max}}}\right)+1}{\sqrt{3}}\right]. \tag{28}$$

Taking phase $a$ as a reference and assuming that the maximum SoC variations are shared between phases $a$ and $c$ with the same value and opposite signs, $\Delta \mathrm{SoC}_{\mathrm{ph}}^{\mathrm{k}+1}$ of phase $b$ will be zero (since $\sum \Delta \mathrm{SoC}_{\mathrm{ph}}^{\mathrm{k}} = 0$). Therefore, $x$ can be approximated as having the worst case value of $\arctan\left(1/\sqrt{3}\right) = \pi/6$. The latter leads to the definition of a minimum rise time $t_r^{\mathrm{ph}}$ of

$$t_r^{\mathrm{ph}} \geq \frac{8NE_{\mathrm{bat},n}^{\mathrm{sm}} \Delta \mathrm{SoC}_{\mathrm{ph}}^{\max} k_{\Delta v} \ln 9}{100\sqrt{3}\hat{i}_T^p \left[Nu_{\mathrm{sm}}^{\mathrm{dim}} - k_{\Delta v}\left(U_S/2 + u_T^{\max}\right)\right]}. \tag{29}$$

In addition, each branch cannot provide negative voltages. That means that a second constraint should be posed regarding the minimum branch voltage value, which should not fall below zero. This is formulated as follows:

$$\frac{U_S}{2} - u_T^{\max} - u_{\mathrm{cm}}^{\max} \geq 0 \Leftrightarrow u_{\mathrm{cm}}^{\max} \leq \frac{U_S}{2} - u_T^{\max}$$
$$\Leftrightarrow \frac{8NE_{\mathrm{bat},n}^{\mathrm{sm}} \Delta \mathrm{SoC}_{\mathrm{ph}}^{\max} \ln 9}{100\sqrt{3}\hat{i}_T^p t_r^{\mathrm{ph}}} \leq U_S/2 - u_T^{\max} \tag{30}$$

giving therefore the second limitation as

$$t_r^{\mathrm{ph}} \geq \frac{8NE_{\mathrm{bat},n}^{\mathrm{sm}} \Delta \mathrm{SoC}_{\mathrm{ph}}^{\max} \ln 9}{100\sqrt{3}\hat{i}_T^p \left(U_S/2 - u_T^{\max}\right)}. \tag{31}$$

Therefore, the rise time is proportional to the battery nominal energy as well as the tolerated maximum SoC error. However, it is inversely proportional to the maximum current, which means that the maximum achievable balancing power is limited in lower currents.

The constraint for the submodule SoC-balancing control is related to overmodulation. The branch voltage is weighted with the ratio factor $\beta_{kji}$, which is related to the sum of the submodule mean power $P_{\mathrm{Bat}}^k/2N$ with the respective balancing action $\Delta P_{\mathrm{sm}}^{kji}$, as shown in Fig. 9(a). This can be finally expressed as

$$\beta_{kji} u_{\mathrm{br}}^{\max} \leq U_{\mathrm{sm}}^{\min} \Leftrightarrow \frac{\frac{P_{Bat}^k}{2N} + \Delta P_{\mathrm{sm}}^{\max}}{\frac{P_{\mathrm{Bat}}^k}{2}} u_{\mathrm{br}}^{\max} \leq U_{\mathrm{sm}}^{\min}$$
$$\Leftrightarrow \left(\frac{1}{N} + \frac{2\Delta P_{\mathrm{sm}}^{\max}}{P_{\mathrm{Bat}}^k}\right) \leq \frac{U_{\mathrm{sm}}^{\min}}{u_{\mathrm{br}}^{\max}}$$

$$\Leftrightarrow \Delta P_{\rm sm}^{\max} \le \frac{P_{\rm Bat}^k}{2}\left(\frac{U_{\rm sm}^{\min}}{u_{\rm br}^{\max}} - \frac{1}{N}\right)$$
$$\overset{(27)}{\Leftrightarrow} \frac{E_{{\rm bat},n}^{\rm sm}\Delta {\rm SoC}_{\rm sm}^{\max}\ln 9}{100\cdot t_r^{\rm sm}} \le \frac{P_{\rm Bat}^k\left(NU_{\rm sm}^{\min} - u_{\rm br}^{\max}\right)}{2Nu_{\rm br}^{\max}} \tag{32}$$

leading to a minimum rise time of

$$t_r^{\rm sm} \ge \frac{2Nu_{\rm br}^{\max}E_{{\rm bat},n}^{\rm sm}\Delta {\rm SoC}_{\rm sm}^{\max}\ln 9}{P_{\rm Bat}^k\left(NU_{\rm sm}^{\min} - u_{\rm br}^{\max}\right)100} = \frac{2Nu_{\rm br}^{\max}E_{{\rm bat},n}^{\rm sm}\Delta {\rm SoC}_{\rm sm}^{\max}\ln 9}{P_{\rm Bat}^k\left[N\left(1-k_u\right)\overline{U}_{\rm sm} - u_{\rm br}^{\max}\right]100} \tag{33}$$

where $k_u$ is the allowed voltage ripple on the submodule capacitor voltage and $u_{\rm br}^{\max} = U_S/2 + u_T^{\max} + u_{\rm cm}^{\max}$.

In this case, a faster balancing can be achieved with a higher amount of absorbed submodule power $P_{\rm Bat}^k/2N$. Another way to avoid overmodulation is to control the mean value of the submodule capacitor voltages $\overline{U}_{\rm sm}$ at a higher value, which means however an increase in the required installed capacitive energy.

Finally, the limitation of the branch SoC-balancing loop should be established. Since it regards a circulating current injection, it is limited by the respective rating of the semiconductors in the converter branches. Considering all different components, the branch current can be expressed as

$$i_{\rm br} = \frac{\hat{i}_T^p}{2}\cos(\omega t + \phi_i^p) + \frac{I_S}{3} + \hat{i}_{{\rm circ},2}\cos(2\omega t + \phi_i^p) + \hat{i}_{\rm bal}^k\cos\omega t + \frac{1}{\sqrt{3}}\left(\hat{i}_{\rm bal}^{k+2} - \hat{i}_{\rm bal}^{k+1}\right)\sin\omega t. \tag{34}$$

Considering the worst case, i.e., that all three phases are experiencing the maximum SoC error between their upper and lower branches, the following inequality should hold for the dimensioned branch current:

$$i_{\rm br}^{\rm dim} \ge \hat{i}_T^p\left(\frac{1}{2}\cos(\omega t + \phi_i^p) + \frac{\varepsilon}{4}\cos\phi_i^p + \frac{1}{4}\cos(2\omega t + \phi_i^p)\right) + \frac{NE_{{\rm bat},n}^{\rm sm}\ln 9}{100\cdot t_r^{br}}\left[\frac{\Delta {\rm SoC}_{\rm br}^{\rm k,max}}{\left(\hat{u}_V + \hat{u}_{cm}\cos\phi_{cm}\right)}\cos\omega t + \frac{1}{\sqrt{3}}\left(\frac{\Delta {\rm SoC}_{\rm br}^{\rm k+2,max}}{\left(\hat{u}_V + \hat{u}_{\rm cm}\cos\left(\phi_{\rm cm} - \frac{2\pi}{3}\right)\right)} - \frac{\Delta {\rm SoC}_{\rm br}^{\rm k+1,max}}{\left(\hat{u}_V + \hat{u}_{\rm cm}\cos\left(\phi_{\rm cm} + \frac{2\pi}{3}\right)\right)}\right)\sin\omega t\right]. \tag{35}$$

It is clear that the phase balancing SoC loop is interacting with the branch balancing one through the appeared injection of the common-mode voltage component $u_{\rm cm}$. In addition the ratio $\varepsilon$, which defines the value of $I_{\rm circ0}$, has an impact on the branch current peak value. A generalized analytical solution is therefore not straightforward. Instead, a numerical evaluation can be performed in order to specify the minimum rise time of the loop. The respective equation is obtained as (36), at the bottom of the page.

Some remarks can be therefore made. Relation (33) reveals that a common-mode voltage increase limits the amount of active power that can be absorbed or injected from each submodule for balancing purposes. Moreover, the branch average power $P_{\rm Bat}^k/2$ is a function of the current angle $\phi_i^p$ as well as the power $\Delta P_{\rm ph}^k$ needed for the phase SoC balancing. This is a constraint, which should be also taken into account during the design process. In general, the phase balancing control loop has an effect on the submodule balancing one, implying that the latter should be chosen with a lower bandwidth, leading therefore to $t_r^{\rm ph} < t_r^{\rm sm}$. Moreover and in order to achieve independence from the global current control as well as power transfer, the relations $\sum \Delta P_{\rm ph}^k = \sum \Delta P_{\rm sm}^{kji} = 0$ should hold. This can be also guaranteed through the use of $(N-1)$ controllers/branch for the submodule as well as two controllers for the phase SoC-balancing loops.

Finally, it is noted that the established limitations in (31) and (33) can be utilized for adaptive gain calculation in cases of operating point changes, as already mentioned for (36).

### *B. Simulation Results*

The final overall system control block diagram of the MMC-BESS system is illustrated in Fig. 10. All different utilized control systems and variables are depicted according to the considerations made throughout the previous sections. It is noted that the SoC-balancing controllers will not have any contribution to the system once the batteries are perfectly balanced, as already assumed for the results of Fig. 6.

The proposed SoC-balancing control strategy has been tested in simulations and the results are shown in Fig. 11. All battery packs have been initialized with an arbitrary SoC and the maximum difference reaches up to 22.5%. A battery charging procedure until $t = 250$ s is followed by a respective discharging. The convergence of the submodule, phase, and branch SoCs is evident. The common-mode voltage as well as the balancing circulating currents are also fading out as the respective phase and branch SoC deviations tend asymptotically to zero. The unequal power distribution to the batteries for balancing purposes is depicted on the battery currents of Fig 11(a). In Fig. 11(d), it is shown that the dc-link current will not be affected by the branch balancing circulating currents, due to the respective reactive injection in the other two phases. Therefore, it will bear only a dc component.

$$t_{\rm br} \ge \max\left\{\frac{\frac{NE_{{\rm bat},n}^{\rm sm}\ln 9}{100}\left[\frac{\Delta {\rm SoC}_{\rm br}^{\rm k,max}}{\left(\hat{u}_V + \hat{u}_{\rm cm}\cos\phi_{\rm cm}\right)}\cos\omega t + \frac{1}{\sqrt{3}}\left(\frac{\Delta {\rm SoC}_{\rm br}^{\rm k+2,max}}{\left(\hat{u}_V + \hat{u}_{\rm cm}\cos\left(\phi_{\rm cm} - \frac{2\pi}{3}\right)\right)} - \frac{\Delta {\rm SoC}_{\rm br}^{\rm k+1,max}}{\left(\hat{u}_V + \hat{u}_{\rm cm}\cos\left(\phi_{\rm cm} + \frac{2\pi}{3}\right)\right)}\right)\sin\omega t\right]}{i_{\rm br}^{\rm dim} - \hat{i}_T^p\left(\frac{1}{2}\cos(\omega t + \phi_i^p) + \frac{\varepsilon}{4}\cos\phi_i^p + \frac{1}{4}\cos(2\omega t + \phi_i^p)\right)}\right\} \tag{36}$$

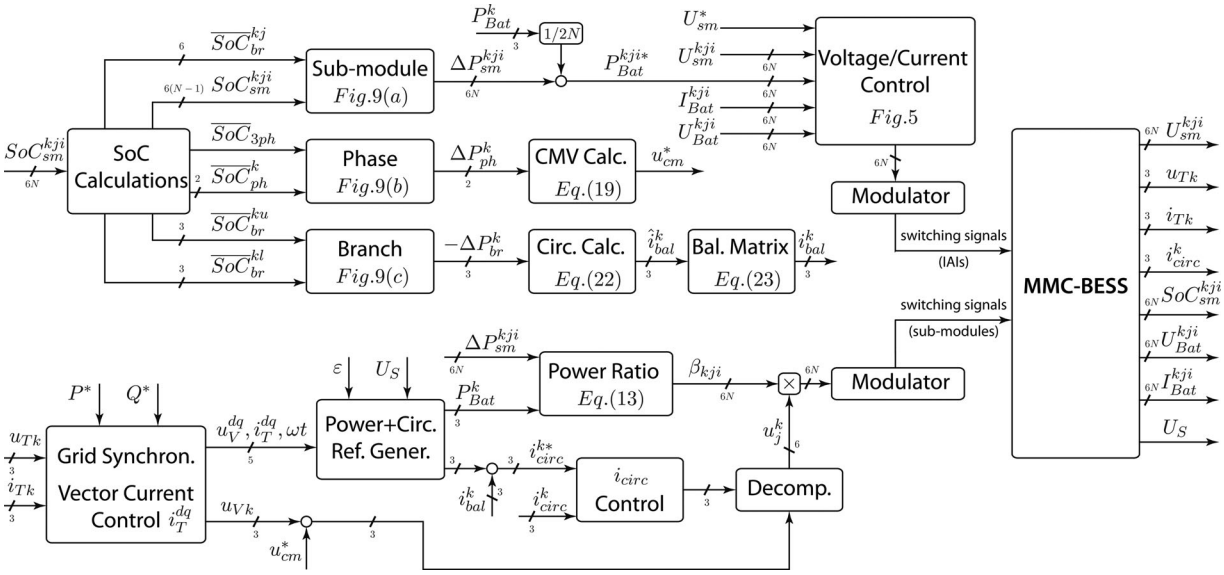


Fig. 10. Overall system control block diagram.

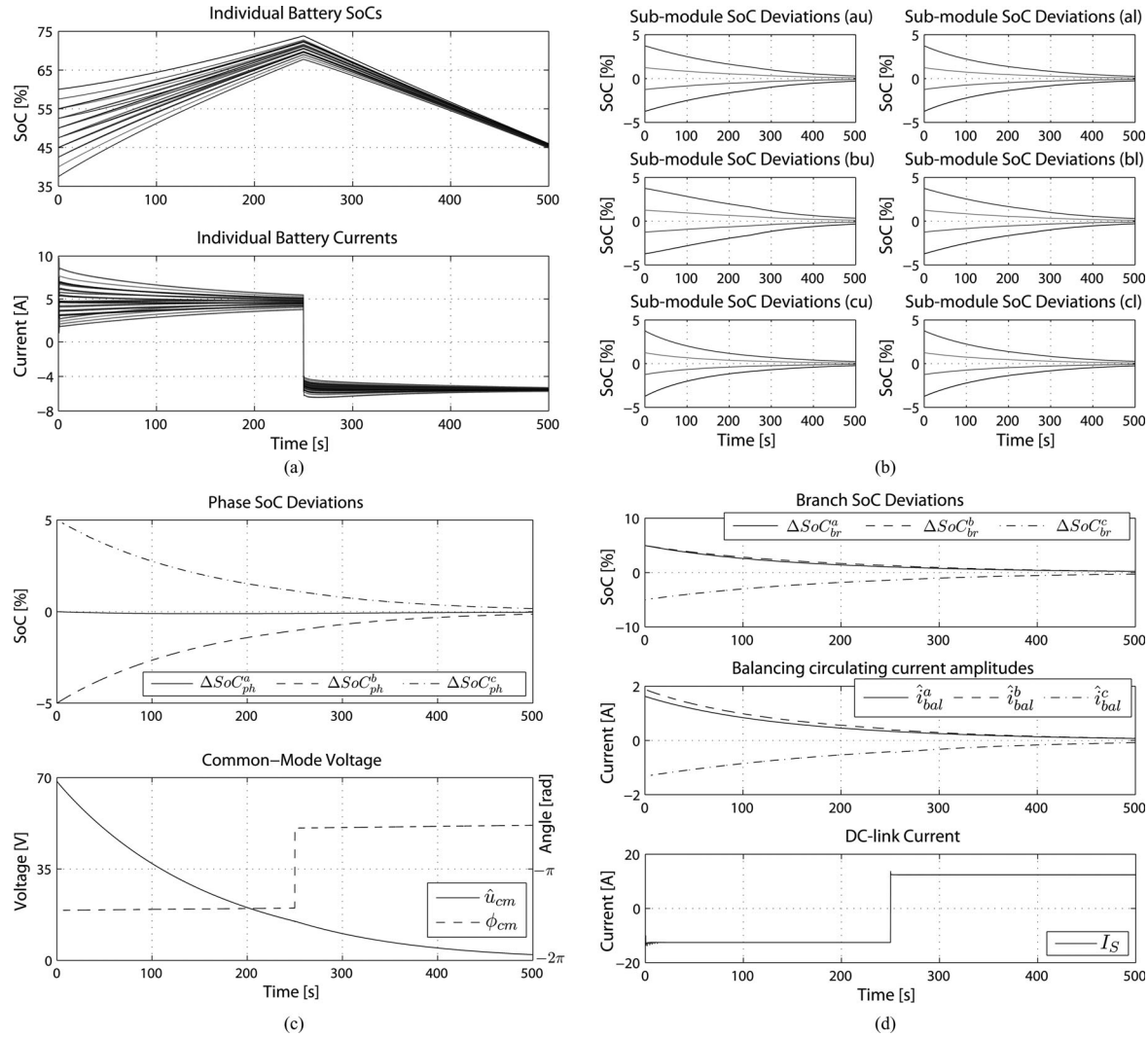


Fig. 11. Simulation results for the MMC-based storage unit: (a) Individual battery SoCs and respective currents during converter-balancing action. (b), (c), (d) Time-domain convergence of the submodule, phase, and branch SoC-balancing regulators. Closed-loop rise times have been set to $t_r^{\mathrm{sm}} = 400$ s, $t_r^{\mathrm{ph}} = 300$ s, and $t_r^{\mathrm{br}} = 350$ s.

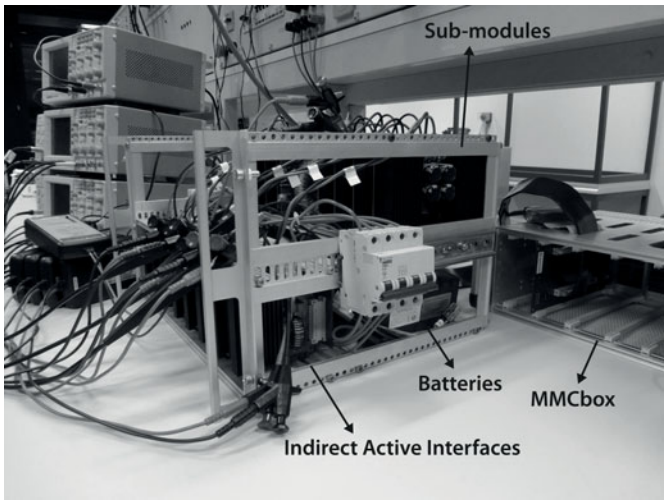


Fig. 12. MMC phase leg with the integrated BESS.

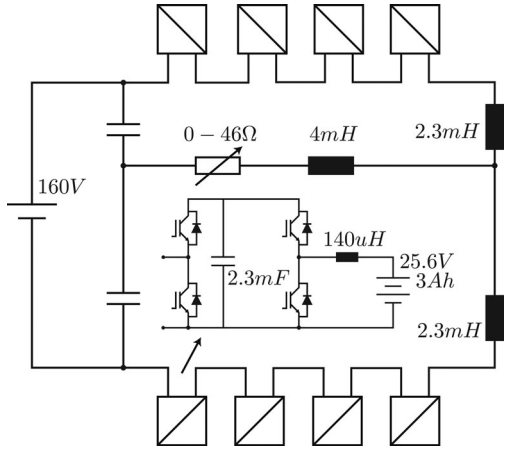


Fig. 13. Schematic of the experimental setup circuit configuration.

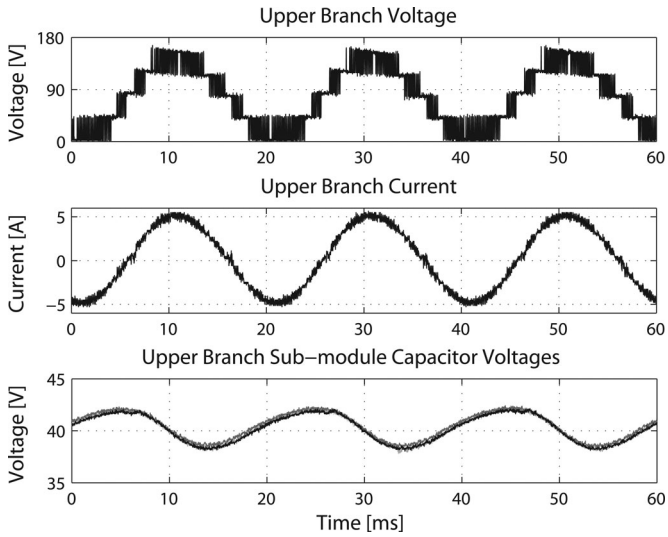


Fig. 14. Experimental results for a discharging procedure of the batteries in the inverting operation, corresponding to Mode V: Upper branch quantities.

In the presented concept of voltage control through the dc/dc conversion stage, the average submodule voltages can be kept constant throughout the whole balancing operation. This is an advantage over proposed concepts of direct submodule/battery interface [25], [26]. The latter implies an inevitable submodule voltage dependence on the battery SoC, which can lead to significant variations according to the utilized electrochemical technology.

## V. Experimental Results

A reduced-scale prototype has been implemented, in order to test experimentally the basic functionalities of the studied system. A single phase leg of 4-kVA nominal power has been designed and constructed so far, which consists of eight submodules with split BESSs. This is illustrated in Fig. 12. Each submodule consists of four switches, giving the user the option between a half-bridge or full-bridge configuration, as well as a capacitor with a respective voltage measurement. The buck converters (IAIs) comprise a half-bridge with a filter inductor, and provide the measurements of the battery current and voltage. Both the submodules and the IAIs are mounted in a rack, whose backplanes carry all gate signals, measurements, and power supplies. The batteries are also placed in the same rack. The utilized packs are of $LiFePO_4$ 25.6 V/3 Ah technology [46]. The embedded BMS of each pack protects the battery from short circuits, under- and over-voltages. However, it does not provide cell-balancing functions or estimation for the SoC of the pack. Therefore, the purpose of the prototype is to test the basic control/modulation functions and operating modes rather than implementing the SoC-balancing algorithms developed in the previous section.

The converter control is carried out in a custom hardware platform, namely the MMCbox, whose design and features resemble the one of [47]. All hardware components are connected to a backplane and communicate via a common parallel bus. The communication is supervised by a central microcontroller-based unit programmed in C. The latter executes all the high-level control tasks and sends the calculated duty cycles to the slave VHDL-programmed FPGA-based boards. A modularized concept is followed with one FPGA card/phase leg, therefore in this case only one is used. This is responsible for producing the firing signals and retrieving the necessary measurements from the converter, i.e., the submodule voltages as well as the battery currents/voltages. In addition, it is in charge of ensuring the converter protection, in cases where overvalues are detected. An additional FPGA-based board has been designed for the retrieval of external converter measurements, such as dc link and grid voltages as well as to control the relays used for converter precharging and discharging operations.

For the performed test, the phase leg is connected to a fixed voltage source on the dc-link side and to an inductive/resistive passive load on the ac side. The circuit configuration is shown in Fig. 13 along with the main system parameters. Fig. 14 illustrates the resulted magnitudes of the upper branch. The circulating current is controlled to comprise an almost zero dc component, therefore most of the power will be delivered to the load by the batteries. This corresponds to operating Mode V, as explained in

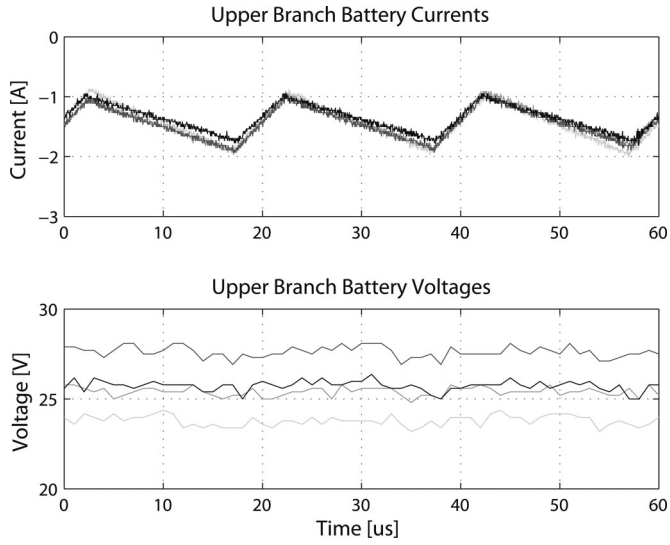


Fig. 15. Experimental results for a discharging procedure of the batteries in the inverting operation, corresponding to Mode V: Battery magnitudes.

Section II. The carriers of the submodule modulators are phase-shifted in order to obtain the five-level voltage waveform $u_u$. Finally, the submodule capacitor voltages are perfectly balanced due to their active control from the battery side through the IAIs.

A detail of the battery currents and voltages is depicted in Fig. 15. The currents contain only the switching-related ripple but no low-frequency components. The difference of the battery voltages according to their SoC has no effect on the upper branch voltage waveform, which is an advantage of their decoupling from the submodules. In this test, the same battery current reference is set for all IAIs. This implies a different amount of injected power due to the respective difference of the battery voltages. The latter is handled effectively by the individual submodule power control. It is noted that larger active power differences between the submodules would lead to more visible differences on their capacitor voltage ripples, due to the different respective current variations.

## VI. Conclusion

This paper has investigated the operation and control of a MMC-based storage unit with split accumulation. The batteries have been interfaced to the converter submodules by means of nonisolated dc/dc converters. The latter offer an additional DOF for the capacitor voltage control from the battery side. The ways to control the active power flows in all directions within the converter have been studied. The submodule, phase, and branch battery SoCs have been modeled in a straightforward manner and three types of loops have been designed in order to achieve their balancing. The gain limitations have been established and all analytical developments have been verified by simulations for several expected modes of operation, including grid unbalances. The development of a low-scale prototype has been described and experimental results have been presented validating the basic control functions of such a converter structure.

## Acknowledgment

The authors would like to thank EOS Holding, Switzerland, for the financial support of this research project.

## References

[1] A. Lesnicar and R. Marquardt, "A new modular voltage source inverter topology," in *Proc. 10th Eur. Conf. Power Electron. Appl.*, Toulouse, France, Sep. 2–4, 2003.

[2] R. Marquardt, "Modular multilevel converter: An universal concept for HVDC-Networks and extended DC-Bus-applications," in *Proc. Int. Power Electron. Conf.*, Jun. 21–24, 2010, pp. 502–507.

[3] M. Glinka and R. Marquardt, "A new AC/AC multilevel converter family," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 662–669, Jun. 2005.

[4] L. Baruschka and A. Mertens, "A new three-phase AC/AC modular multilevel converter with six branches in hexagonal configuration," *IEEE Trans. Ind. Appl.*, vol. 49, no. 3, pp. 1400–1410, May/Jun. 2013.

[5] A. J. Korn, M. Winkelnkemper, P. Steimer, and J. W. Kolar, "Direct modular multi-level converter for gearless low-speed drives," in *Proc. 14th Eur. Conf. Power Electron. Appl.*, Aug. 30–Sep. 1, 2011, pp. 1–7.

[6] S. Kenzelmann, A. Rufer, M. Vasiladiotis, D. Dujic, F. Canales, and Y. R. de Novaes, "A versatile DC–DC converter for energy collection and distribution using the modular multilevel converter," in *Proc. 14th Eur. Conf. Power Electron. Appl.*, Aug. 30/Sep. 1, 2011, pp. 1–10.

[7] S. Allebrod, R. Hamerski, and R. Marquardt, "New transformerless, scalable modular multilevel converters for HVDC-transmission," *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 15–19, 2008, pp. 174–179.

[8] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2903–2912, Oct. 2010.

[9] X. Li, Q. Song, W. Liu, H. Rao, S. Xu, and L. Li, "Protection of nonpermanent faults on DC overhead lines in MMC-Based HVDC systems," *IEEE Trans. Power Del.*, vol. 28, no. 1, pp. 483–490, Jan. 2013.

[10] Q. Song, W. Liu, X. Li, H. Rao, S. Yu, and L. Li, "A steady-state analysis method for a modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 3702–3713, Aug. 2013.

[11] M. Hiller, D. Krug, R. Sommer, and S. Rohner, "A new highly modular medium voltage converter topology for industrial drive applications," in *Proc. 13th Eur. Conf. Power Electron. Appl.*, Sep. 8–10, 2009, pp. 1–10.

[12] M. Hagiwara, K. Nishimura, and H. Akagi, "A medium-voltage motor drive with a modular multilevel PWM inverter," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1786–1799, Jul. 2010.

[13] M. Winkelnkemper, A. Korn, and P. Steimer, "A modular direct converter for transformerless rail interties," in *Proc. IEEE Int. Symp. Ind. Electron.*, Jul. 4–7, 2010, pp. 562–567.

[14] M. Vasiladiotis, S. Kenzelmann, N. Cherix, and A. Rufer, "Power and DC link voltage control considerations for indirect AC/AC modular multilevel converters," in *Proc. 14th Eur. Conf. Power Electron. Appl.*, Aug. 30–Sep. 1, 2011, pp. 1–10.

[15] M. Hagiwara, R. Maeda, and H. Akagi, "Control and analysis of the modular multilevel cascade converter based on double-star chopper-cells (MMCC-DSCC)," *IEEE Trans. Power Electron.*, vol. 26, no. 6, pp. 1649–1658, Jun. 2011.

[16] A. Korn, M. Winkelnkemper, and P. Steimer, "Low output frequency operation of the modular multi-level converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 12–16, 2010, pp. 3993–3997.

[17] M. A. Pérez and J. Rodríguez, "Generalized modeling and simulation of a modular multilevel converter," in *Proc. IEEE Int. Symp. Ind. Electron.*, Jun. 27–30, 2011, pp. 1863–1868.

[18] P. Munch, D. Gorges, M. Izak, and S. Liu, "Integrated current control, energy control and energy balancing of modular multilevel converters," in *Proc. 36th Annu. Conf. IEEE Ind. Electron. Soc.*, Nov. 7–10, 2010, pp. 150–155.

[19] J. Kolb, F. Kammerer, and M. Braun, "Straight forward vector control of the modular multilevel converter for feeding three-phase machines over their complete frequency range," in *Proc. 37th Ann. Conf. IEEE Ind Electron. Soc.*, Nov. 7–10, 2011, pp. 1596–1601.

[20] N. Cherix, M. Vasiladiotis, and A. Rufer, "Functional modeling and energetic macroscopic representation of modular multilevel converters," in *Proc. 15th Int. Power Electron. Motion Control Conf.*, Sep. 4–6, 2012, pp. 1–8.

[21] Q. Tu, Z. Xu, Y. Chang, and L. Guan, "Suppressing DC voltage ripples of MMC-HVDC under unbalanced grid conditions," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1332–1338, Jul. 2012.

[22] M. Guan and Z. Xu, "Modeling and control of a modular multilevel converter-based HVDC system under unbalanced grid conditions," *IEEE Trans. Power Electron.*, vol. 27, no. 12, pp. 4858–4867, Dec. 2012.
[23] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modulation, losses, and semiconductor requirements of modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2633–2642, Aug. 2010.
[24] K. Ilves, A. Antonopoulos, S. Norrga, and H.-P. Nee, "A new modulation method for the modular multilevel converter allowing fundamental switching frequency," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3482–3494, Aug. 2012.
[25] L. Maharjan, T. Yamagishi, and H. Akagi, "Active-Power control of individual converter cells for a battery energy storage system based on a multilevel cascaded PWM converter," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1099–1107, Mar. 2012.
[26] L. Maharjan, S. Inoue, H. Akagi, and J. Asakura, "State-of-charge (SOC)-balancing control of a battery energy storage system based on a cascade PWM converter," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1628–1636, Jun. 2009.
[27] M. Vasiladiotis and A. Rufer, "Balancing control actions for cascaded H-bridge converters with integrated battery energy storage," in *Proc. 15th Eur. Conf. Power Electron. Appl.*, Sep. 2–6, 2013, pp. 1–10.
[28] M. Vasiladiotis, A. Rufer, and A. Béguin, "Modular converter architecture for medium voltage ultra fast EV charging stations: Global system considerations," in *Proc. IEEE Int. Electric Vehicle Conf.*, Mar. 4–8, 2012, pp. 1–7.
[29] I. Trintis, S. Munk-Nielsen, and R. Teodorescu, "Cascaded H-bridge with bidirectional boost converters for energy storage," in *Proc. 14th Eur. Conf. Power Electron. Appl.*, Aug. 30–Sep. 1, 2011, pp. 1–9.
[30] I. Trintis, S. Munk-Nielsen, and R. Teodorescu, "A new modular multilevel converter with integrated energy storage," in *Proc. 37th Ann. Conf. IEEE Ind. Electron. Soc.*, Nov. 7–10, 2011, pp. 1075–1080.
[31] L. Baruschka and A. Mertens, "Comparison of cascaded H-Bridge and modular multilevel converters for BESS application," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 17–22, 2011, pp. 909–916.
[32] M. Schroeder, S. Henninger, J. Jaeger, A. Rasic, H. Rubenbauer, and H. Leu, "Integration of batteries into a modular multilevel converter," in *Proc. 15th Eur. Conf. Power Electron. Appl.*, Sep. 2–6, 2013, pp. 1–12.
[33] A. Hillers and J. Biela, "Optimal design of the modular multilevel converter for an energy storage system based on split batteries," in *Proc. 15th Eur. Conf. Power Electron. Appl.*, Sep. 2–6, 2013, pp. 1–11.
[34] M. Vasiladiotis, N. Cherix, and A. Rufer, "Accurate capacitor voltage ripple estimation and current control considerations for grid-connected modular multilevel converters," *IEEE Trans. Power Electron.*, 2014, to be published.
[35] S. P. Engel and R. W. De Doncker, "Control of the modular multi-level converter for minimized cell capacitance," in *Proc. 14th Eur. Conf. Power Electron. Appl.*, Aug. 30–Sep. 1, 2011, pp. 1–10.
[36] S. Rivera, S. Kouro, B. Wu, J. I. Leon, J. Rodríguez, and L. G. Franquelo, "Cascaded H-bridge multilevel converter multistring topology for large scale photovoltaic systems," in *Proc. IEEE Int. Symp. Ind. Electron.*, Jun. 27–30, 2011, pp. 1837–1844.
[37] M. Coppola, A. Del Pizzo, and D. Iannuzzi, "A power traction converter based on modular multilevel architecture integrated with energy storage devices," in *Proc. Int. Conf. Electr. Syst. Aircraft, Railway Ship Propulsion*, Oct. 16–18, 2012, pp. 1–7.
[38] H. Bühler, *Réglage de systèmes d'électronique de puissance—Volume 1: Théorie*. Lausanne, Switzerland: Presses Polytechniques et Universitaires Romandes, 1997.
[39] A. D. Aquila, M. Liserre, V. G. Monopoli, and P. Rotondo, "An energy-based control for an $n$-H-bridges multilevel active rectifier," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 670–678, Jun. 2005.
[40] R. E. Betz and T. J. Summers, "Using a cascaded H-bridge STATCOM for rebalancing unbalanced voltages," in *Proc. 7th Int. Conf. Power Electron.*, Oct. 22–26, 2007, pp. 1219–1224.
[41] T. J. Summers, R. E. Betz, and G. Mirzaeva, "Phase leg voltage balancing of a cascaded H-bridge converter based STATCOM using zero sequence injection," in *Proc. 13th Eur. Conf. Power Electron. Appl.*, Sep. 8–10, 2009, pp. 1–10.
[42] A. Antonopoulos, L. Ängquist, and H.-P. Nee, "On dynamics and voltage control of the modular multilevel converter," in *Proc. 13th Eur. Conf. Power Electron. Appl.*, Sep. 8–10, 2009, pp. 1–10.
[43] P. Rodriguez, J. Pou, J. Bergas, J. I. Candela, R. P. Burgos, and D. Boroyevich, "Decoupled double synchronous reference frame PLL for power converters control," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 584–592, Mar. 2007.
[44] M. Vasiladiotis, N. Cherix, D. Siemaszko, and A. Rufer, "Operation of modular multilevel converters under grid asymmetries," in *Proc. 39th Annu. Conf. IEEE Ind. Electron. Soc.*, Nov. 10–13, 2013, pp. 6281–6286.
[45] C. Fahrni, A. Rufer, F. Bordry, and J. P. Burnet, "A novel 60 MW pulsed power system based on capacitive energy storage for particle accelerators," *Eur. Power Electron. Drives Assoc. J.*, vol. 18, no. 4, pp. 5–13, Dec. 2008.
[46] *Powerizer product catalog*. (2013). [Online]. Available: www.batteryspace.com
[47] N. Cherix, S. Delalay, P. Barrade, and A. Rufer, "Fail-safe modular control platform for power electronic applications in R&D environments," in *Proc. 15th Eur. Conf. Power Electron. Appl.*, Sep. 2–6, 2013, pp. 1–10.

**Michail Vasiladiotis** (S'09) was born in Athens, Greece, in 1986. He received the Diploma degree in electrical and computer engineering from the National Technical University of Athens, Athens, Greece, in 2009. Since 2010, he has been working toward the Ph.D. degree at the Laboratory of Industrial Electronics, École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland.

His research interests include multilevel conversion systems for high power applications, modern control methods for power converters, as well as power electronic interfaces for ultrafast EV charging.

**Alfred Rufer** (M'95–SM'01–F'06) received the M.S. degree from the Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland, in 1976.

In 1978, he joined ABB, Turgi, Switzerland, where he was involved in the fields of power electronics and control, such as high-power variable frequency converters for drives, and where he was a Group Leader involved with power electronic development beginning in 1985. In 1993, he became an Assistant Professor at EPFL, where, since 1996, he has been a Full Professor and the Head of the Industrial Electronics Laboratory (LEI). LEI is active in power electronics used in energy conversion and energy storage and in the modeling and simulation of systems, including control strategies and control circuits. He has authored or co-authored many publications on power electronics and its applications, such as multilevel converters and various energy-storage systems. He is the holder of several patents.