A Simplified Nearest Level Control (NLC) Voltage Balancing Method for Modular Multilevel Converter (MMC)

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***Abstract*—In this paper, a simplified nearest level control balancing method for modular multilevel converter is presented. The proposed method neither requires individual sorting of the submodule voltages nor the redundancy of the switching states. Once the sorting of the submodules is done on the basis of the number of the submodules to be switched on, the identifications of the submodules can be carried out throughout the stages of the implementation of the this method. The proposed method also does not require the individual submodule status in the gate pulse generation stage. The gate logic in the presented method can be implemented with the help of the switching states of the voltage levels. Those simplifications and removing of the some of the stages by the proposed balancing method may ease and lead to the less processor time at the implementation level. The pictorial presentation further helps in consolidating the understanding of the different stages of the method. Rigorous simulations are carried out for open and one of the prominent closed-loop applications, i.e., modular multilevel converter-based high-voltage direct current to demonstrate the validity and effectiveness of the proposed simplified balancing method under normal and emergency conditions.**

***Index Terms*—Modular multilevel converter (MMC), nearest level control (NLC) method, submodule (SM), voltage-source converter high-voltage direct current (VSC-HVDC) transmission.**

NOMENCLATURE

A. Abbreviations

CHB	Cascaded H-bridge.
IGBT	Insulated-gate bipolar transistor.
MMC	Modular multilevel converter.
NLC	Nearest level control.
PWM	Pulse width modulation.
PSPWM	Phase-shifted PWM.
SM	Submodule.
SHE	Selective harmonic elimination.

B. Symbols

n	Number of SM per arm.
C	SM capacitance.
L_S	Arm inductance.
V_C	SM capacitor voltage.
$V_{\rm dc}$	Pole-to-pole dc-bus voltage.
$I_{\rm dc}$	DC current.
v_j	Voltage with respect to fictitious point "o" of phase-j $(j = a, b, c)$.
i_j	Output current of phase-j ($j = a, b, c$).
$v_{{\rm up}j}$, $v_{{\rm lo}j}$	Total voltage of upper and lower arms of phase-j $(j = a, b, c)$.
$v_{{\rm up}_j}^{\rm SM}$, $v_{{\rm lo}_j}^{\rm SM}$	Total voltage of upper and lower SMs of phase-j $(j = a, b, c)$.
$i_{{\rm up}_j}$, $i_{{\rm lo}_j}$	Upper and lower arms current of phase-j $(j = a, b, c)$.
i_{zj}	Circulating current of phase-j $(j = a, b, c)$.
$v_{c1{\rm up}_j} \cdots v_{cn{\rm up}_j}$	Instantaneous voltage of SM-1, SM-2… SM-n of the upper arms of phase-j $(j = a, b, c)$.
$v_{c1{\rm lo}_j} \cdots v_{cn{\rm lo}_j}$	Instantaneous voltage of SM-1, SM-2… SM-n of the lower arm of phase-j $(j = a, b, c)$.
$S_{{\rm up}_{j_k}}$, $S_{{\rm lo}_{j_k}}$	Switching functions of upper and lower arms of phase-j $(j = a, b, c)$ for $k =$ SM-1, SM-2…SM-n.

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I. INTRODUCTION

MULTILEVEL inverters have presented an important development in recent years to reach higher power with increasing voltage levels [1]–[5]. Large numbers of multilevel inverters topology have been investigated but few of them are practical for industrial applications [6]–[12]. Diode clamped and CHB are the most preferred choices [13]–[20]. For medium-voltage (2.3, 3.3 and 4.16 kV) applications, three-level neutral-point clamped is the suitable topology, but having the constrained of mass clamping and the voltage imbalance of dc-link capacitors in extending its use to higher voltage levels [6]–[19]. For applications with voltage higher than 6 kV, CHB multilevel inverters are commonly used [15], [17], [20]. Isolated sources are required in this topology. To generate individual voltage sources, a conventional method is to employ a multiwinding transformer with the same number of isolated secondary windings, which is huge and expensive.

The MMC topology has recently drawn huge interest in high-voltage applications [21]–[25], [29]–[44]. It is first

proposed by Marquardt and Lesnicar [22] and is regarded as one of the next-generation high-voltage multilevel converters without line-frequency transformers [29]. The modularity, voltage scalability, and common dc bus make MMC topology favorite for high-voltage applications [31]–[40]. The first commercialized MMC-voltage-source converter high-voltage direct current (VSC-HVDC) project is the Trans Bay Cable Project in the U.S.A., with 216 SMs for each arm. In addition, another MMC–VSC-HVDC project INELFE from France to Spain built by Siemens completed in 2013. It can transmit rated power 2 $\times$ 1000 MW and has 401 voltage levels [30], [37]. Most of the advantages come from its scaled structure. Therefore, the voltage balancing of multiple floating dc capacitors of the SMs becomes a vital factor for the safe operation of MMC [24], [31]. There have been many research efforts made to explore the voltage balancing strategies based on level-shifted PWM [31]–[35], PSPWM [36]–[38], SHE [39], and NLC [40]–[44]. The high switching frequency of PWM is unsuitable for large numbers of SMs MMC. The switching losses are predominant in high switching frequency modulation. The voltage balancing algorithm based on PSPWM requires individual SM balancing controller which is inappropriate for large numbers SMs MMC [36]–[38]. However, a large amount of switching angles in the SHE modulation is computed offline and stored in tables, so with large number of SMs MMC-based HVDC, the SHE method is complicated [40]–[44].

Due to the conceptual and implementation simplicity of the NLC method, the aim is to use it in converters with a high number of levels [43]. Few research papers are published on the NLC-based voltage balancing algorithm of SMs capacitor voltages of MMC with the application to HVDC. One commonly used balancing approach is based on sorting of the voltages of the capacitors. Then, the capacitors with the highest or lowest voltages are selected to be discharged or charged determined by the current direction [31]–[35], [40]. The predefined voltage deviation of the SM voltages can be set in [41]. The SM voltages fluctuations are limited by controlling the triggering frequency [42]. There are number of stages of implementation of the balancing algorithm based on sorting. However, every stage of the balancing algorithm has not been clearly demonstrated in [40]–[44].

This paper presents simplified NLC method of voltage balancing based on sorting of the voltages of the SM capacitors, which can simplify and eliminate some of the stages of the balancing algorithm. Elimination of some of the stages can reduce the processor time in the hardware implementation. The proposed method is pictorially presented to consolidate the understanding of the balancing algorithm. The feasibility and robustness of the proposed method have been verified by applying to one of the prominent applications MMC–VSC-HVDC. The comprehensive simulations have been carried out in MATLAB/SIMULINK.

This paper starts in Section II with a description of the MMC structure and its operation. Section III explains the NLC method. The various stages of the proposed balancing simplified NLC method are introduced in Section IV. The MMC–VSC-HVDC transmission system and its control strategies are presented in Section V. The simulation results and how the proposed algorithm can be implemented are described in Sections VI and VII, followed by the concluding remarks in Section VIII.

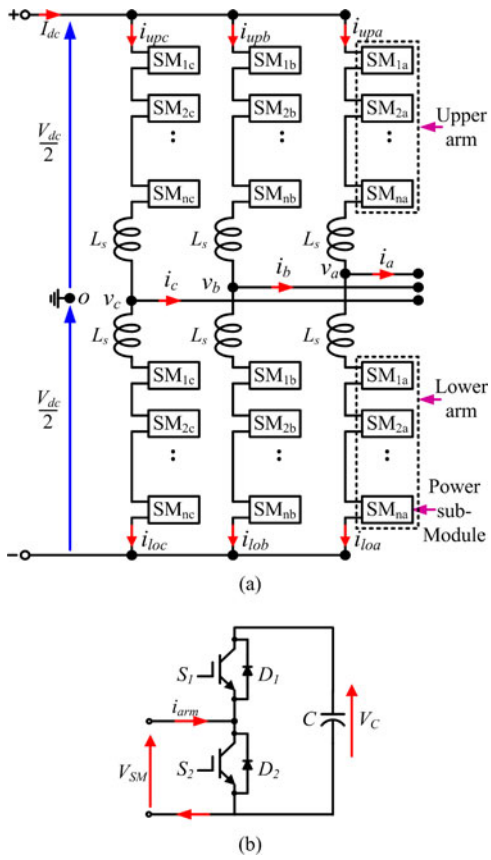

Fig. 1. (a) Three phase n-level MMC topology and (b) MMC SM.

II. Modular Multilevel Converter

A. Basic Structure

The typical structure of a MMC is shown in Fig. 1(a) and the configuration of an SM is given in Fig. 1(b). Each SM is a simple chopper cell composed of two IGBT switches S_1 and S_2, two antiparallel diodes D_1 and D_2, and a capacitor C. Each phase leg of the converter has two arms, upper and lower. Each one is constituted by n number of SMs. In each arm, there is also a small inductor L_s to compensate for the voltage difference between upper and lower arms produced when a SM is switched in or out. With reference to the SM shown in Fig. 1(b), the output voltage $V_{\rm SM}$ has two values; $V_{\rm SM} = V_C$ when S_1 is ON and S_2 is OFF or $V_{\rm SM} = 0$ when S_1 is OFF and S_2 is ON. Table I summarizes the switch states of a SM and their resultant influence on associated capacitor voltages.

B. Operation Principle

The number of levels in the phase leg depends not only on the way number of SMs connected in the arm but also on the way converter leg is modulated. Output line-to-neutral (phase) voltage has $(n+1)$ levels in LSPWM, if topology consisting "n"

TABLE I
SWITCHING STATES OF A CELL

S_1	S_2	D_1	D_2	Current direction	Capacitor states	Output voltage
OFF	ON	OFF	OFF	$i_{arm} > 0$	Unchanged	0
OFF	OFF	OFF	ON	$i_{arm} < 0$	Unchanged	0
OFF	OFF	ON	OFF	$i_{arm} > 0$	Charging	V_C
ON	OFF	OFF	OFF	$i_{arm} < 0$	Discharging	V_C

numbers of SMs per arm. When PSPWM is adopted, $2n$ SMs in each phase leg have $2n$ triangular waveforms with the same frequency but a phase difference of $360/2n$, and then output line-to-neutral voltage has $2n + 1$ levels. Based on Fig. 1(a), the mathematical equations which govern dynamic behavior can be expressed for each phase as [40]

$$v_{\mathrm{up}j} = v_{\mathrm{up}_j}^{\mathrm{SM}} + L_s \frac{di_{\mathrm{up}_j}}{dt} \tag{1}$$

$$v_{\mathrm{lo}j} = v_{\mathrm{lo}_j}^{\mathrm{SM}} + L_s \frac{di_{\mathrm{lo}_j}}{dt} \tag{2}$$

$$v_{\mathrm{up}_j}^{\mathrm{SM}} = \sum_{k=1}^{n} \left(S_{\mathrm{up}_{j_k}} v_{C\,\mathrm{up}_{j_k}} \right) \tag{3}$$

$$v_{\mathrm{lo}_j}^{\mathrm{SM}} = \sum_{k=1}^{n} \left(S_{\mathrm{lo}_{j_k}} v_{C\,\mathrm{lo}_{j_k}} \right) \tag{4}$$

$$v_j = \frac{V_{\mathrm{dc}}}{2} - v_{\mathrm{up}_j} = -\frac{V_{\mathrm{dc}}}{2} + v_{\mathrm{lo}_j} \tag{5}$$

$$v_{\mathrm{up}_j}^{\mathrm{SM}} = -v_j - L_s \frac{di_{\mathrm{up}_j}}{dt} + \frac{V_{\mathrm{dc}}}{2} \tag{6}$$

$$v_{\mathrm{lo}_j}^{\mathrm{SM}} = v_j - L_s \frac{di_{\mathrm{lo}_j}}{dt} + \frac{V_{\mathrm{dc}}}{2} \tag{7}$$

$$i_{\mathrm{up}_j} = \frac{i_j}{2} + \frac{I_{\mathrm{dc}}}{3} + i_{zj} \tag{8}$$

$$i_{\mathrm{lo}_j} = -\frac{i_j}{2} + \frac{I_{\mathrm{dc}}}{3} + i_{zj} \tag{9}$$

where $v_{\mathrm{up}j}$ is the total arm voltage on each phase j including the total voltage of all upper $\mathrm{SM_S}$ ($v_{\mathrm{up}_j}^{\mathrm{SM}}$) and the voltage of the inductor L_S. $V_{\mathrm{dc}}, I_{\mathrm{dc}}, i_{\mathrm{up}_j}, i_{\mathrm{lo}_j}$ and i_{zj} are the total dc bus voltage, dc current, upper arm current, lower arm current, and the circulating current, respectively. The value of the circulating current of all the phases is zero ($i_{za} + i_{zb} + i_{zc} = 0$). The discrete steps in the output voltage is obtained by controlling switching functions of the SMs in the upper and lower arms of each phase according to (1)–(5). Similar definitions are applicable for the lower arm identified with the subscript "l_o."

III. NLC METHOD

The NLC, also known as the round method, uses the nearest voltage level that can be generated by converting to the desired output voltage reference [44]. The three phases are controlled separately based on the process of independent comparisons. As illustrated in Fig. 2(a), sampled waveform can be formed by comparing the reference waveform with the existing output

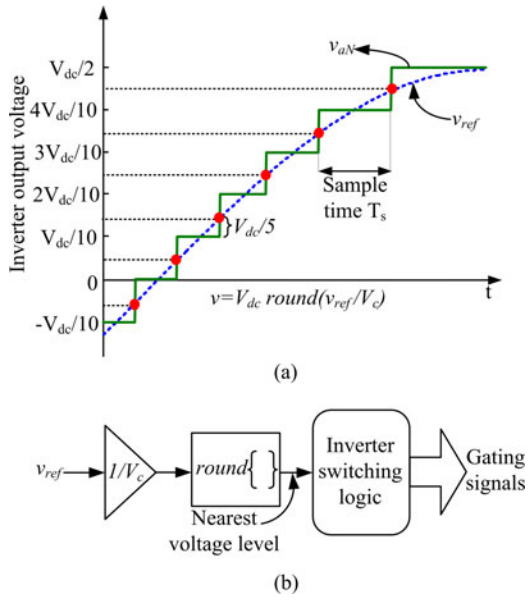

Fig. 2. Nearest level selection (a) waveform synthesis and (b) control diagram.

voltage level. Given a voltage reference v_{ref}, the nearest output voltage level n_{nl} can be determined with

$$n_{nl} = \frac{1}{V_c} \mathrm{round}(v_{\mathrm{ref}}) \tag{10}$$

where V_c is the SM capacitor voltage. The next step is to determine how many numbers of SMs shall be switched ON and is performed by round function. The function returns the nearest integer of the input number (e.g., round $(3.4) = 3$, round $(3.6) = 4$) [42]. This nearest integer multiplied by V_c corresponds to the closed level to the reference that is generated by the inverter [10]. The operating principle for the 11-level output voltage is demonstrated in Fig. 2(a) for the first quarter cycle of a sinusoidal reference [31]. The numbers of SMs required are $n = 10$ per arm. The capacitor voltage of each SM is $V_c = \frac{V_{\mathrm{dc}}}{n} = \frac{V_{\mathrm{dc}}}{10}$. The approximation error is $V_{dc}/5$. The implementation of the nearest voltage level generation is illustrated in Fig. 2(b)

IV. SIMPLIFIED NLC METHOD

In the simplified NLC method, the same concept of balancing i.e., on the basis of sorting the voltages of the capacitors is used [21]–[23], [31], [33], [40]–[44]. Then, the capacitors with highest voltages or the capacitors with lowest voltages are selected to be discharged or charged determined by the current direction. Simplification at the each stage is done to reduce the processor time for the hardware implementation in the proposed method. The simplified NLC method in this paper has been described for the seven levels of voltages of the MMC. The pictorial presentation of the simplified LSPWM balancing algorithm is presented here for the consolidation of the understanding of the method at the different levels of the implementation. The similar following subprocesses are applied for the lower arm.

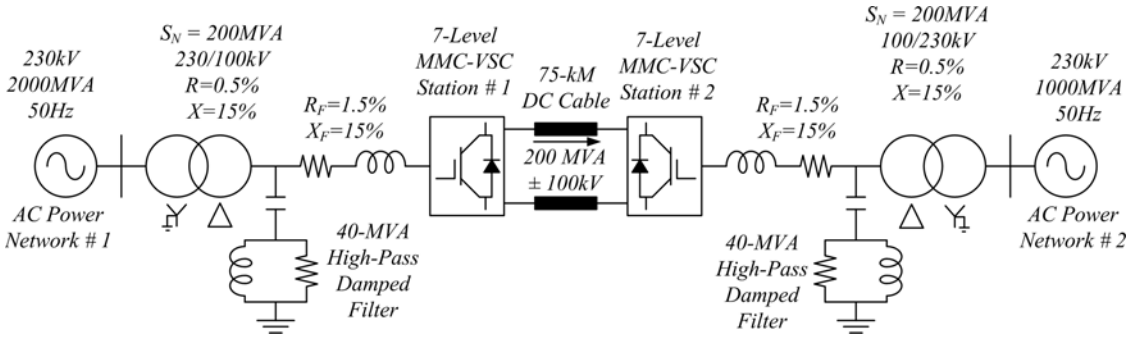

Fig. 3. Data and parameters of the MMC-VSC-HVDC transmission system.

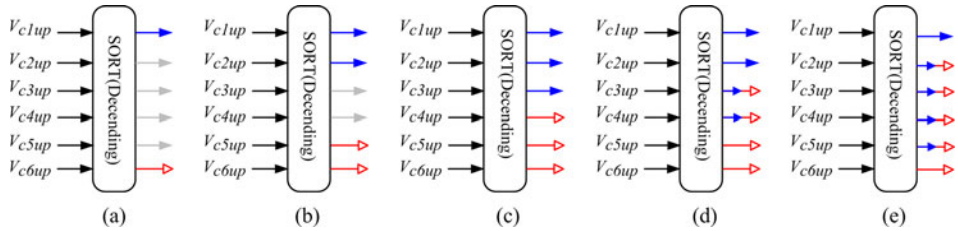

Fig. 4. Sorting of SMs capacitor voltages in the descending order. (a) Single SM voltage. (b) Two SMs voltages. (c) Three SMs voltages. (d) Four SMs voltages. (e) Five SMs voltages (blue solid arrow indicates maximum and red hollow arrow indicates minimum capacitor SM voltages).

A. *Sorting of SMs Voltages*

The voltages of the capacitors of the arm SMs are sorted in the descending order. The total number of the SMs is switched ON at any time are 6 for realizing the seven level of phase to neutral voltage of the MMC. Therefore, sorted capacitor voltages are chosen according to the requirement of the switching sequence of the SMs, i.e., when one SM from the upper arm is chosen, five SMs from the lower arm are chosen, next two SMs from upper arm and four from lower arm, then three from upper and three from lower arm, and this continues till the six from upper arm and none from the lower arm selection comes. The last capacitor voltage in the descending order sorting is the minimum and the first sorted capacitor voltage is the maximum. The minimum and maximum values of the single capacitor voltage are chosen from the last and the first signal from Fig. 4(a). Similarly, two capacitor voltages are chosen from the last and from the first. The procedure for choosing the three, four, and the five SMs capacitor voltages are the same and illustrated in Fig. 4(b)–(e). There is no rigmarole method in choosing minimum and maximum number of the capacitor voltages in the simplified NLC method. In the conventional balancing method, which is based on sorting of the capacitor voltages [21]–[23], [31], [33], [40]–[44], the individual sorting of the capacitor voltages is required. Individual sorting is required comparatively complex logic and more processor space.

B. *Passing SM Voltages by Detection of the Arm Current*

After the detection of the arm current, selected number of SMs can be forwarded according to the direction of the current. If the arm current is greater than zero, the SMs with lowest voltages are selected otherwise highest SMs. The process of forwarding the one, two, three, four, and five numbers of the SM capacitors voltages according to the direction of the arm current is illustrated in Fig. 5(a)–(e).

C. *Status Identification of the Capacitor Voltages*

The SMs capacitor voltages are available according to the direction of arm current. Available capacitor voltages of the SMs can have the lowest or highest values. Those available outputs of Fig. 5(a)–(e) are only the numbers of the SM capacitor voltages. Each of that outputs can have the value of first, second, third, fourth, fifth, and sixth SM capacitor voltage. The task of this controller is to pass that status of the input signal of the multiport switch. For an example, when input to the multiport switch has first SM capacitor value, it should be passed. Similarly, second, third, fourth, fifth, and sixth SM capacitor voltage value for that input to be forwarded. The procedure for passing the status to each of the inputs to the multiport port switch is pictorially demonstrated in Fig. 6(a)–(d).

D. *Serial Passing of SMs Capacitor Voltages*

When only one number of SM capacitor voltage (*O/P1_1*) is selected, the probability of appearing of the first SM capacitor voltage (V_{c1up}) is only once and hence, it is straightforward be made available for the gate pulse logic. It is not the case with the two, three, four, five and six numbers of SM capacitor voltages are selected. When two numbers of SMs with their lowest or highest SM voltages (*O/P2_1* and *O/P2_2*) are selected, the

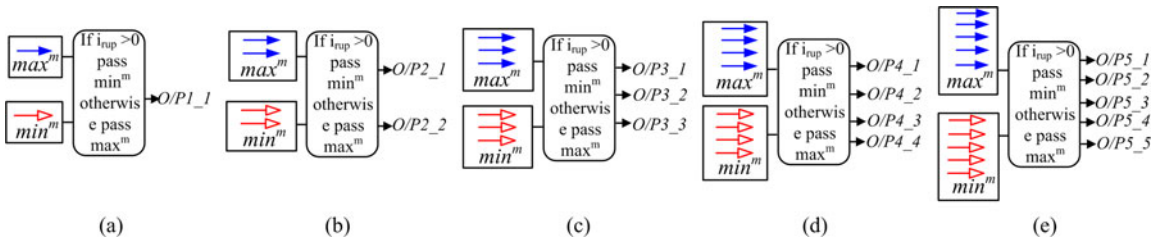

Fig. 5. Minimum or maximum capacitor voltages forwarded according to the direction of arm current. (a) One SM voltage. (b) Two SMs voltages. (c) Three SMs voltages. (d) Four SMs voltages. (e) Five SMs voltages.

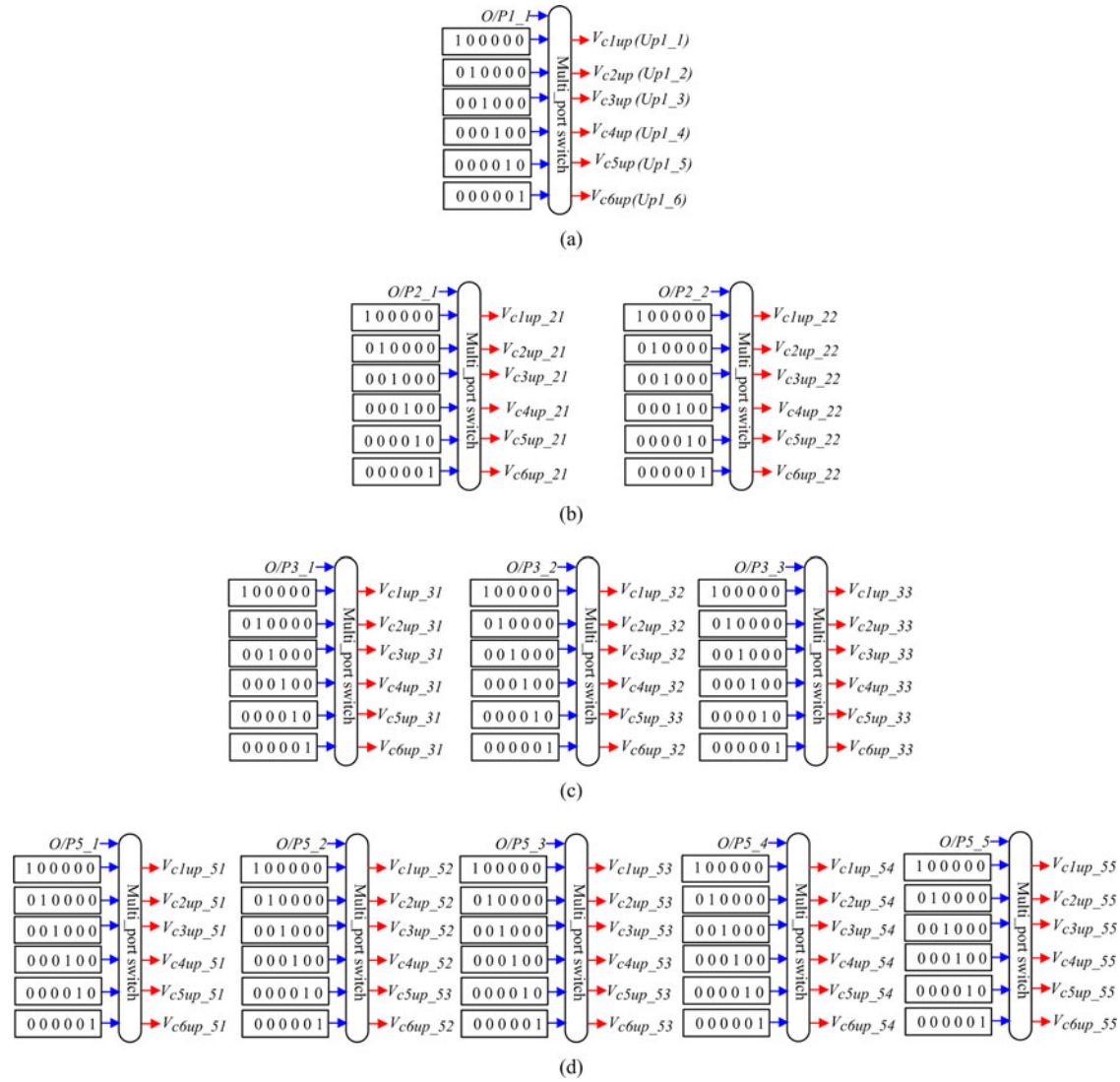

Fig. 6. Realization of module capacitor voltages serially. (a) For one SM voltage. (b) For two SMs voltages. (c) For three SMs voltages. (d) For five SMs voltages.

O/P2_1 and *O/P2_2* can have the first SM voltage (V_{c1up_21} and V_{c1up_22}) at different instants of the time. Both the outputs (V_{c1up_21} and V_{c1up_22}) are provided to the OR gate so that whenever the first SM capacitor voltage is present at any of the two inputs that shall be made available to the gate pulse logic. The same process is applied to get the first, second, third, fourth, fifth, and sixth SM capacitor voltages by giving them to the OR gates. The pictorial presentation is presented in Fig. 7(a) and (b).

E. Generation of Gate Pulses

When all SMs from the upper (i.e. none from the lower) or lower (i.e. none from the upper) arm are ON, it will not affect

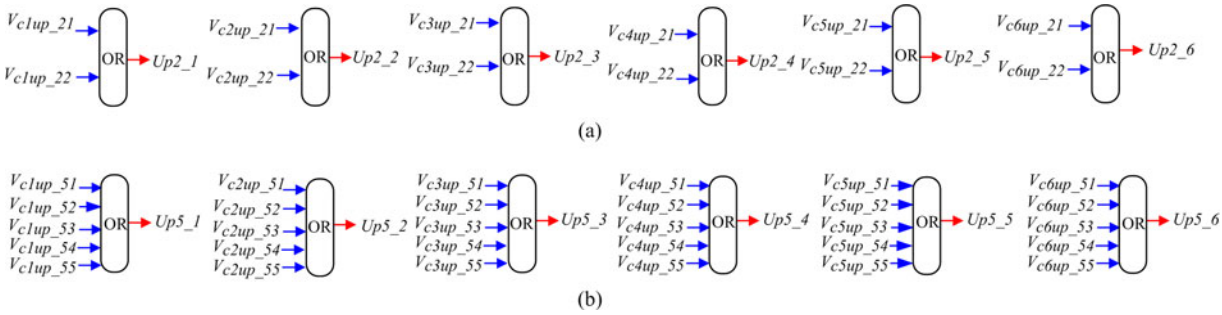

Fig. 7. Collection of one, two, three, four, five, and six SMs capacitor voltages: (a) for two SMs and (b) for five SMs.

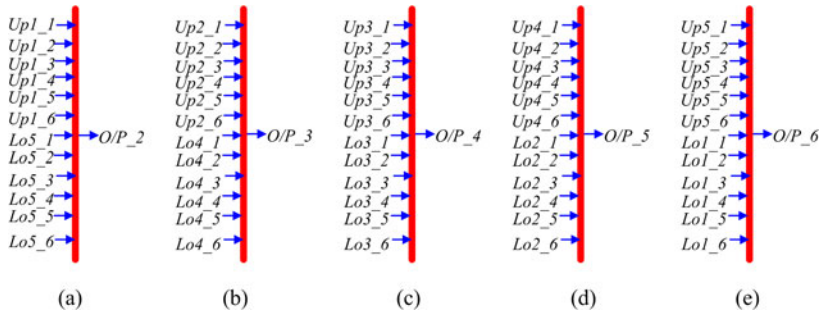

Fig. 8. Generation of gate pulses. (a) Upper one and five lower SMS. (b) Upper two and lower four SMs. (c) Upper three and the lower three SMS. (d) Upper four and the lower two SMs and (e) upper five and lower one SMs.

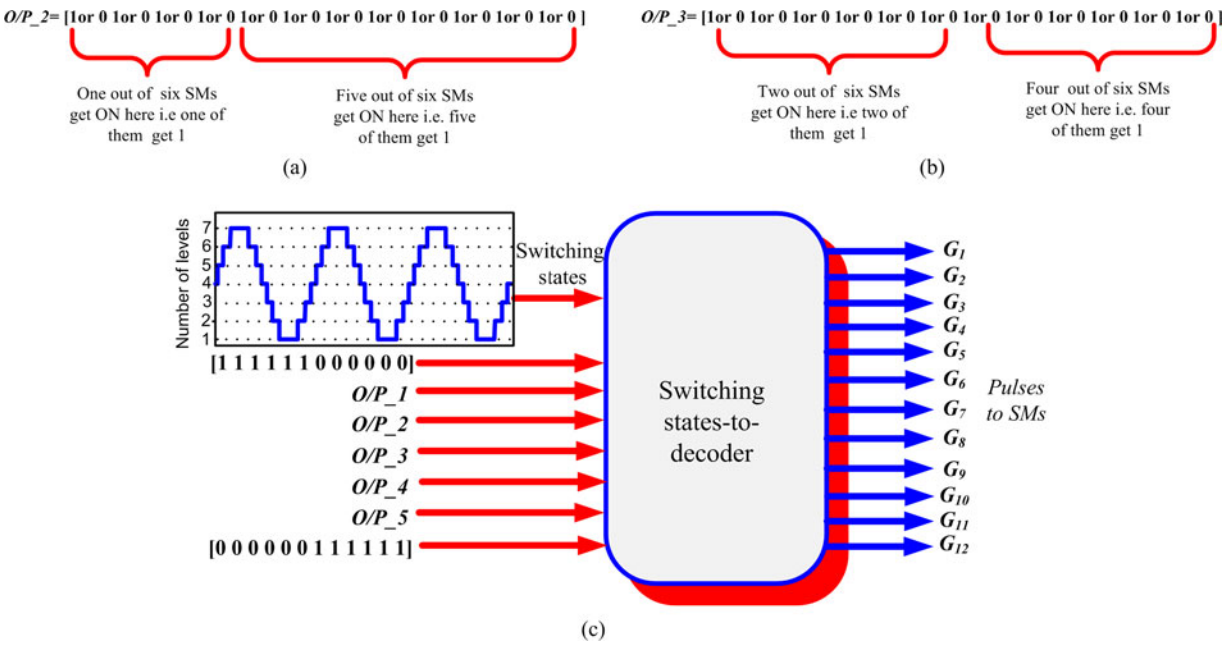

Fig. 9. Gate generation process for the IGBTs of the SMs. (a) and (b) Status of the IGBT on (which one is ON) and (c) switching states to decoder.

the capacitor voltage of the SM. The task of the state-to-decoder is when first level of the output voltage is available, first input should pass. When second output level, the second input shall pass. State condition "1" means that the switch is ON, and "0" means the switch is OFF and illustrated in Fig. 9(a) and (b).

V. MMC–VSC-HVDC System

MMC-based VSC-HVDC is a new electrical transmission based on IGBT and VSC technology. It primarily consists of three parts: a rectifier station, an inverter station, and high-voltage dc transmission cable or lines. The power system

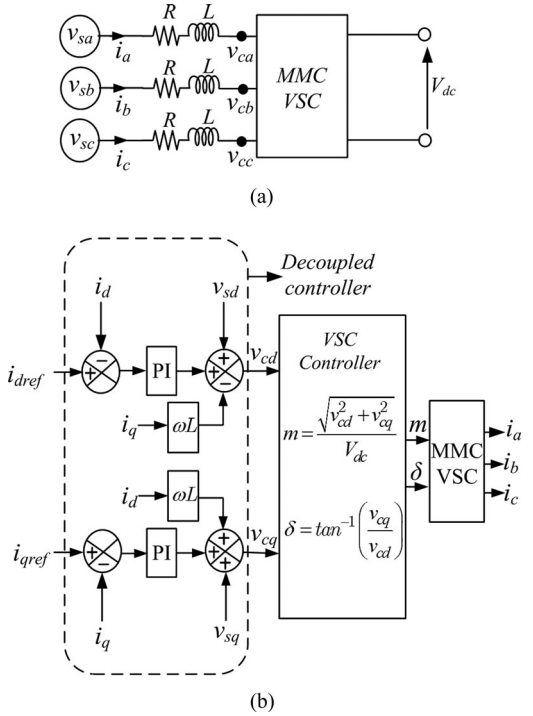

Fig. 10. (a) Three-phase network connected to the VSC and (b) vector control of MMC-HVDC.

considered is a MMC-HVDC system in which two VSCs are linked by 75 km dc cable. System data and parameters are shown in Fig. 3. Both converter stations are composed of seven-level phase voltage MMC connected through the step-up transformers. The shunt-connected low-pass and high-pass-damped *RLC* filters are provided on the ac system to mitigate characteristics harmonics generated by switching actions of the converter.

A. Controls of the MMC-HVDC System

The control strategy of MMC–VSC-HVDC can adopt both direct current control strategy [27] and vector current control strategy [28]. Because of its excellent dynamic performance due to the decoupling of the *d*- and *q*-axes parameters, this paper implemented the vector control strategy. The converter can implement four different control modes: active power control, dc voltage control, dc current control, and ac voltage or reactive power control.

A three-phase view of the ac side of the VSC is shown in Fig. 10(a). The ac-side dynamics can be described as follows:

$$L\frac{di_a}{dt} + i_a R = v_{ca} - v_{sa} \tag{11}$$

$$L\frac{di_b}{dt} + i_b R = v_{cb} - v_{sb} \tag{12}$$

$$L\frac{di_c}{dt} + i_c R = v_{cc} - v_{sc}. \tag{13}$$

The vector representation of above equation can be written as

$$\frac{di_{abc}}{dt} = \frac{1}{L}v_{cabc} - \frac{R}{L}i_{abc} - \frac{1}{L}v_{sabc} \tag{14}$$

where i_a, i_b, and i_c are the currents of the system; v_{ca}, v_{cb}, and v_{cc} are the converter generated voltages; v_{sa}, v_{sb}, and v_{sc} are the system voltages of phases a, b, and c, respectively. Through Park transfer, (14) can be expressed as

$$\frac{Ldi_d}{dt} = v_{cd} - v_{sd} - i_d R + \omega L i_q \tag{15}$$

$$\frac{Ldi_q}{dt} = v_{cq} - v_{sq} - i_q R - \omega L i_d. \tag{16}$$

Equations (15) and (16) are non linear because of the existence of multiplication terms between v_{cd}, v_{cq} and i_d, i_q, so that decoupled controller is defined by

$$v_{cd} = v_{sd}\left(k_p + \frac{k_i}{s}\right)(i_{\mathrm{dref}} - i_d) - \omega L i_q \tag{17}$$

$$v_{cq} = v_{sq}\left(k_p + \frac{k_i}{s}\right)(i_{\mathrm{qref}} - i_q) + \omega L i_d\,. \tag{18}$$

The decoupled controller is shown in Fig. 10(b). If the system operates in three phase balance steady state, "a" phase voltage phase degree is zero. Then, $v_{sd} = |v_{sa}|$, and $v_{sq} = 0$. The active and reactive power flowing into the VSC can be shown as follows:

$$P = \frac{3}{2}(v_{sd}i_d + v_{sq}i_q) = \frac{3}{2}v_{sd}i_d \tag{19}$$

$$Q = \frac{3}{2}(v_{sq}i_d - v_{sd}i_q) = -\frac{3}{2}v_{sd}i_q. \tag{20}$$

VI. Simulation Results

The proposed simplified NLC method has been simulated in MATLAB/SIMULINK. The performance of the simplified NLC method is tested to open-loop *R–L* load, as well as the closed-loop MMC–VSC-HVDC system. The comprehensive results to check the robustness of the method are discussed in following sections. Steps on the regulators, minor, and severe perturbations on the ac sides are carried out.

A. Open-Loop Response of MMC

The converter rating for the open-loop simulation is considered as 1540 MVA with the total dc voltage $V_{\mathrm{DC}} = 200$ kV. Load resistance is 19.44 Ω, load inductance 0.02944 H, and the load capacitor is 0.344 mF. The load power factors 0.5, 0.8, and 0.9 lagging are considered. The buffer inductor is 0.15 p.u. (7.734 mH). Seven-level MMC is considered for the simulation. The effect of modulation index on SM capacitor voltage balance is investigated by considering a load power factor 0.8 lagging at modulation indices. Fig. 11(a) and (b) shows the upper and lower arms SM capacitor voltages at different modulation indices $m = 1$ and $m = 0.5$. For modulation index 1, peak ac voltage output is 100 kV ($m * V_{\mathrm{DC}}/2 = 1 * 100$ kV), and the SM capacitor voltage is 33.33 kV, i.e., $m * V_{\mathrm{DC}}/6$. Similarly,

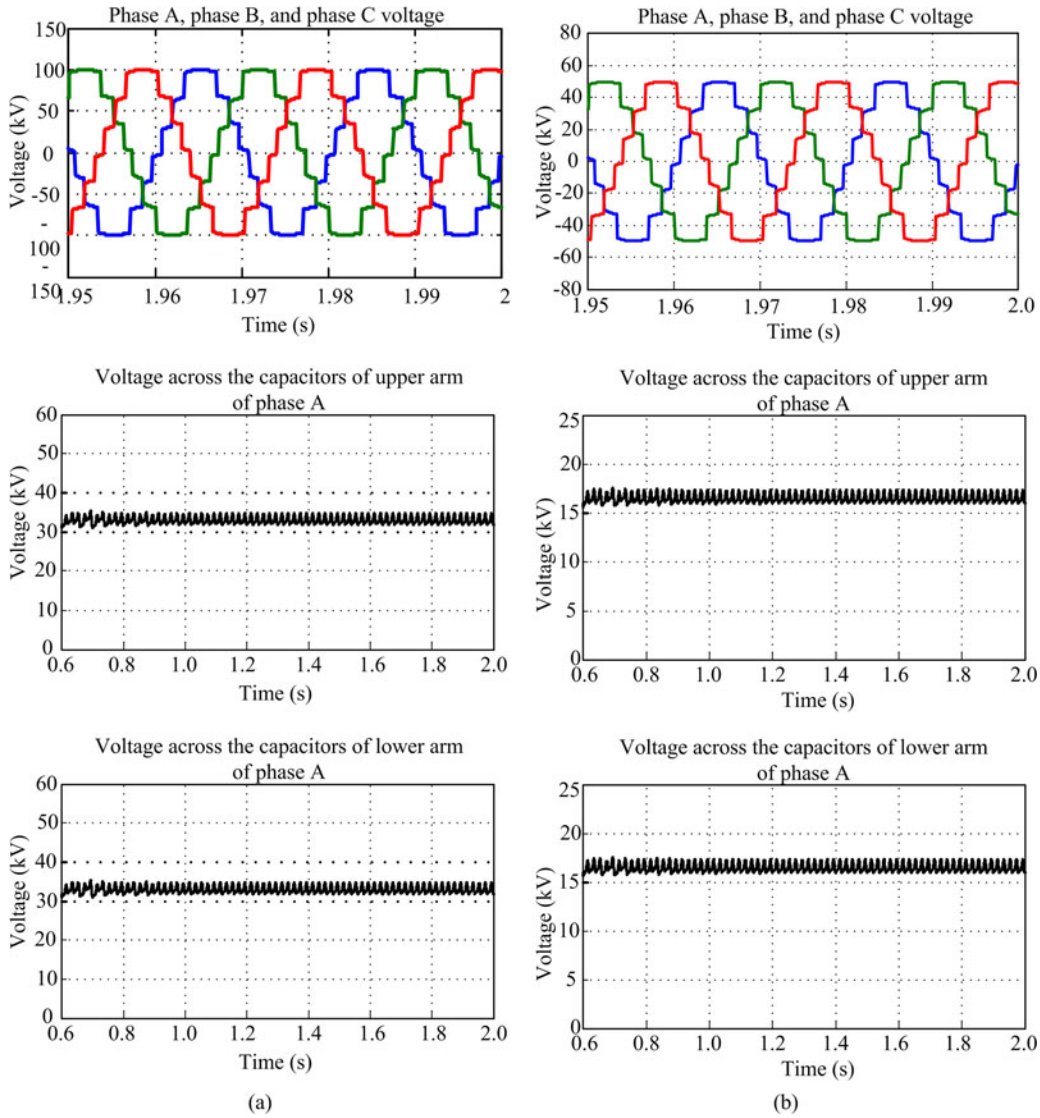

Fig. 11. Effect of modulation index on voltage balance of SM capacitors voltages at power factor 0.8 lagging (voltage across the SMs capacitors voltages of the phases b and c are identical to phase a at (a) modulation index $m = 1$ and (b) modulation index $m = 0.5$.

the peak ac output voltage and the SM capacitor voltage for modulation index 0.5 are 50 and 16.66 kV, respectively. The effect of load power factor on SM capacitor voltage balance is examined for 0.5 and 0.9 lagging and is shown in Fig. 12(a) and (b). The modulation index is considered 0.9. It is observed that even at the low power factor 0.5 lagging, the SM capacitor voltage is well stabilized around the 1.0 s to the expected value 30 kV. The voltages of the SMs capacitors are well maintained at wide range of modulation indices and power factors.

B. Step Response of Power (P&Q) and DC Voltage

The system is programmed to start and reach a steady state. Steps are then sequentially applied on the reference active and reactive power of the station 1 and the reference dc voltage of the inverter. The steady-state values of active, reactive power, and dc voltage are 1 p.u. (200 MW), 1 p.u. (200 MVAR), and 1 p.u. (200 kV), respectively. To examine the robustness of the proposed method, the different regulators are deliberately subjected to the very large values of steps (positive and negative) which is not the practical case. Fig. 13(b) and (c) shows the dynamic response to the changes in real and reactive power commands. At $t = 1.3$ s, large step is first applied to the reference active power from 1 to –0.5 p.u. It is because of the very large steps active power requires more cycles to get stabled to its steady value and the dc voltage at the station 1 is also recovered around the same time that of active power to its steady value of 1 p.u. The second step on the reference active power is applied at the 2.5 s of $+1.5$ p.u., i.e., from -0.5 to 1 p.u. The recovery of the active power in this case is fast as compared to the first step. The dc voltage is stabilized around the same time to its steady state value of 1 p.u.

The step of -0.3 p.u. to the reference of the reactive power is applied at the $t = 2$ s; the reactive power is reached to its

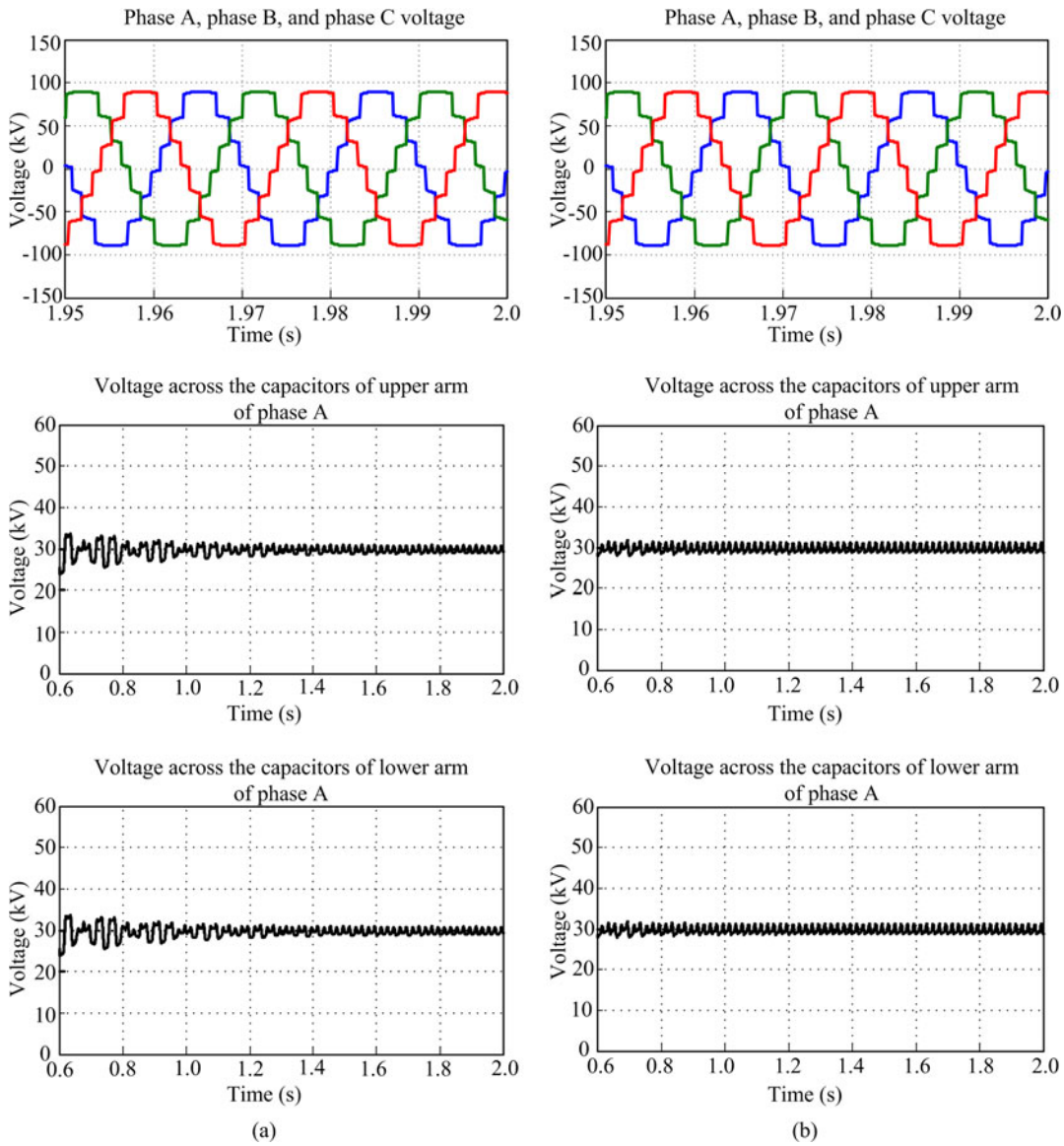

Fig. 12. Effect of power factor on voltage balance of SM capacitors voltages at modulation index $m = 0.9$ (voltage across the SMs capacitors voltages of the phases b and c are identical to phase a (a) power factor 0.5 lagging and (b) power factor 0.9 lagging.

steady-state value within three cycles and the dc voltage is least disturbed. The second step is of 0.5 p.u. applied at the reference reactive power at the 2.7 s. The actual reactive power follows its command and reached to steady state within few cycles. The capacitor voltages are well maintained at their nominal voltage, i.e., under transient and steady-state conditions. This confirms the capability of the simplified NLC method maintaining the SM capacitor voltages to the specified values. Fig. 13(e) shows that the net dc-link voltage, subsequent to the disturbances, is well regulated. The ac system voltage in the per unit at the station 1 is shown in Fig. 13(a). The step of 0.05 p.u. is also applied on the reference dc voltage of the station 2. The various dynamic responses of the different parameters at station 2 are shown in Fig. 14(a)–(e). Though the applied steps are huge at the reactive, active power references and the dc voltage, the effect on the SM capacitor voltages are minimal. This confirms the robustness of the proposed method.

C. Dynamic Response of the MMC–VSC-HVDC Transmission System

For a duration of 7 cycles, the first step of disturbance of value -0.1 p.u. at $t = 1.5$ s on voltage magnitude at the station 1 is applied as shown in Fig. 15(a). The second disturbance of three-phase fault is applied at $t = 2.1$ s for the duration of 6 cycles at the station 2 PCC as shown in Fig. 16(a). The recovery time for active, reactive powers, and dc voltage is less than 0.3 s to reach the steady state. Because of its overcharging, the dc voltage is increased to 1.2 p.u. following the second disturbance. Fig. 15(b) shows the overshoot of 1.33 p.u. in the active power at

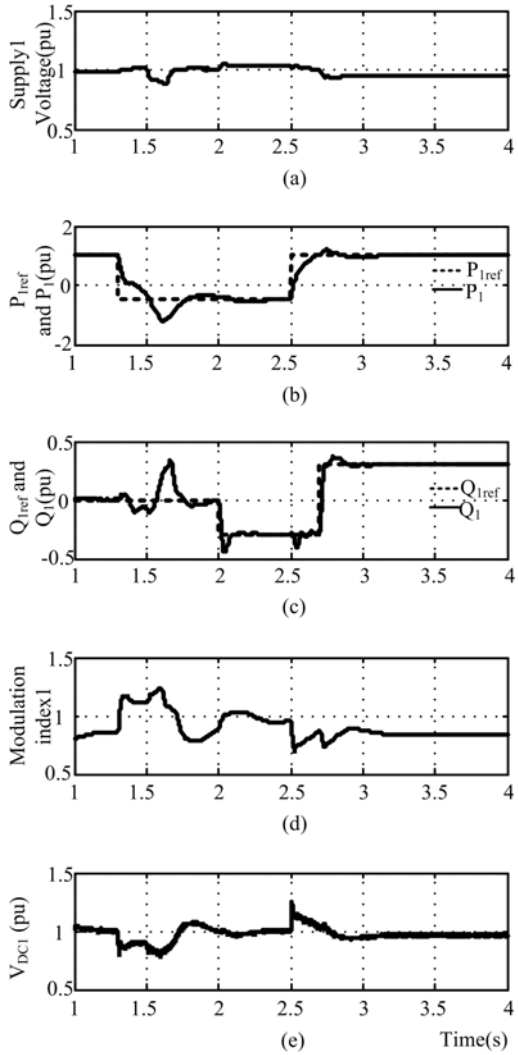

Fig. 13. Station 1 parameters in p.u. (a) Supply voltage. (b) Supplied active power and the reference power. (c) Reactive power and the reference reactive power. (d) Modulation index. (e) DC-link voltage.

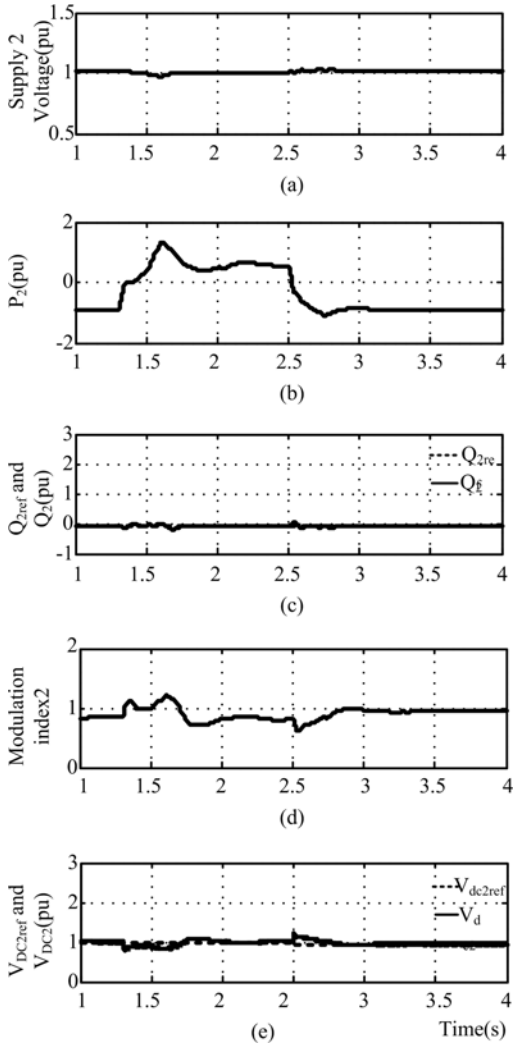

Fig. 14. Station 2 parameters in p.u. (a) Supply voltage. (b) Active power. (c) Reactive power and the reference reactive power. (d) DC voltage and the reference dc voltage. (e) Modulation index.

station 1. The damped oscillations in the reactive power in station 1 are observed and are shown in Fig. 15(c). The dc voltage response at the sending end is shown in Fig. 15(d). Similarly, the responses of the various parameters in station 2 are shown in Fig. 16(a)–(d). Figs. 15(d) and 16(d) show that the dc voltage is quite well regulated even at the huge disturbances, and it recovers within 0.3 s.

VII. Example for the Proposed Algorithm Implementation

The proposed algorithm can be implemented as illustrated in Fig. 17. An example of open-loop MMC is considered for seven-level output voltage. The proposed algorithm for single phase, i.e., per leg is possible to implement using Texas DSP TMS320F2812 with 150 MHz operating frequency. This DSP has 12-bit ADC module with 16-channels. Out of 16 channels, 12 channels can be used to sense the SM capacitor voltages and two channels for upper and lower arm currents through the sensors. It has five input–output ports (GPIO) with 56 pins, out of which 24 pins can be used to trigger the IGBT switches. It has 128 K $\times$ 16 memory with interfacing external memory of 1 MB. This is sufficient to write the proposed algorithm. The conversion time of ADC in TMS320F2812 is 80 ns or 12.5 MSPS (M samples per sec.). It can convert 14 signals within 1120 ns. The sampling frequency can be increased more than 800 KSPS, whereas required sampling frequency is 700 SPS (14 $\times$ 50). The switching frequency is considered 50 Hz. The memory required will be around 65 KB. The number of SMs and the IGBT switches required for three phases are 36 (12 SM per phase, i.e., per leg $\times$ 3) and 72(36 $\times$ 2), respectively. The experimental realization of this method for the three phases is possible using one master and two slave DSPs.

The proposed algorithm eliminates the selection stage of redundancies of voltage levels. It does not require the individual sorting of the SM, and the identification of the SM can be carried out throughout the stages of the implementation of this method. This simplification and elimination of some of the stages may reduce the memory required and computational time to 60%

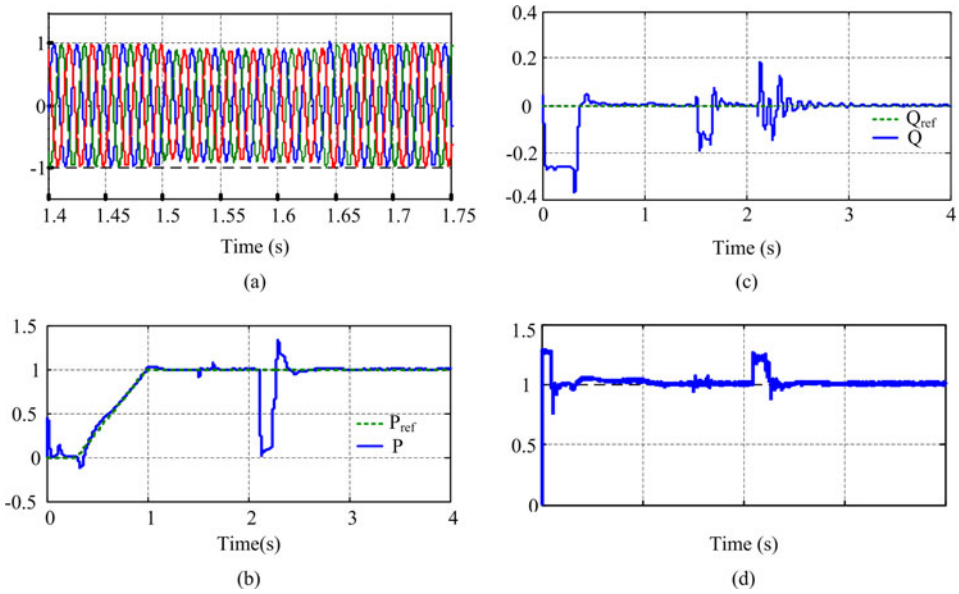

Fig. 15. Dynamic responses at the station 1: (a) supply voltages (in p.u.), (b) active power and the reference active power (in p.u.), (c) reactive power and the reference reactive power (in p.u.), and (d) DC voltage (in p.u.).

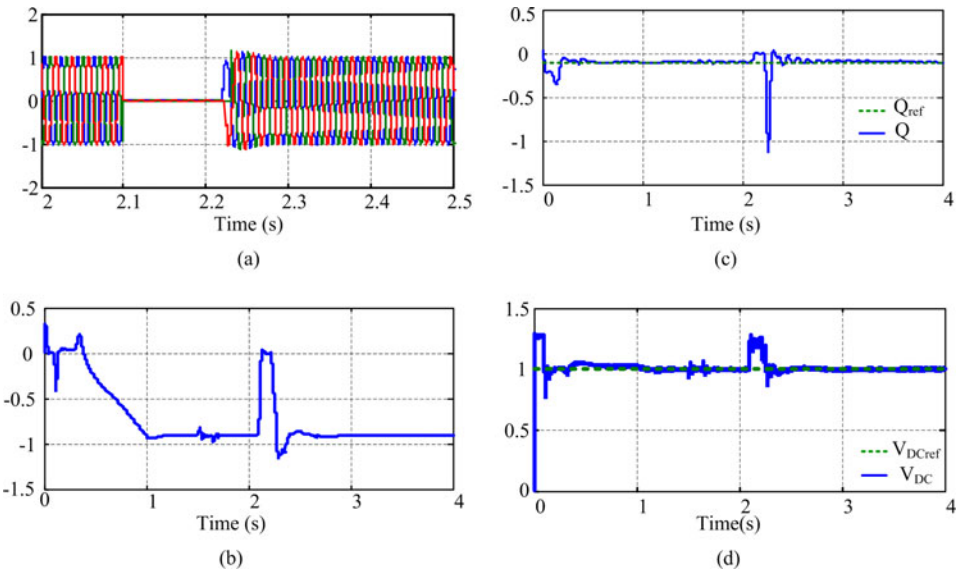

Fig. 16. Dynamic responses at the station 2: (a) supply voltages (in p.u.), (b) active power (in p.u.), (c) reactive power and the reference reactive power (in p.u.), and (d) DC voltage and the reference dc voltage (in p.u.).

as compared to the existing balancing algorithm methods. The NLC method is basically suited for high number of SMs of the output voltage. This is not convenient for the low number of levels and a low modulation index, since the total harmonic distortion of the output is very high [10]. Therefore, the simplification, saving in memory and the computational time is more prominent to the high scale of the system.

VIII. Conclusion

This paper proposed the simplified NLC voltage balancing method for MMCs. This algorithm reduces processes of the different stages from sorting of the SMs to the selection of the number of SMs for the triggering. The proposed method neither requires redundancy and the individual sorting of the SMs nor the identification of individual SM at the time of the triggering. The pictorial presentation of the simplified balancing algorithm also helps in enhancing the understanding of different stages of the algorithm. The comprehensive investigation of this method to one of the applications MMC–VSC-HVDC confirms the robustness under steady state as well as transient conditions. The SM capacitor voltages can be well balanced for open as well as closed-loop applications. The results show that the proposed method is significantly more accurate to the huge disturbances made at the various stages of the controllers. The combined simplification and reduction of processes at various

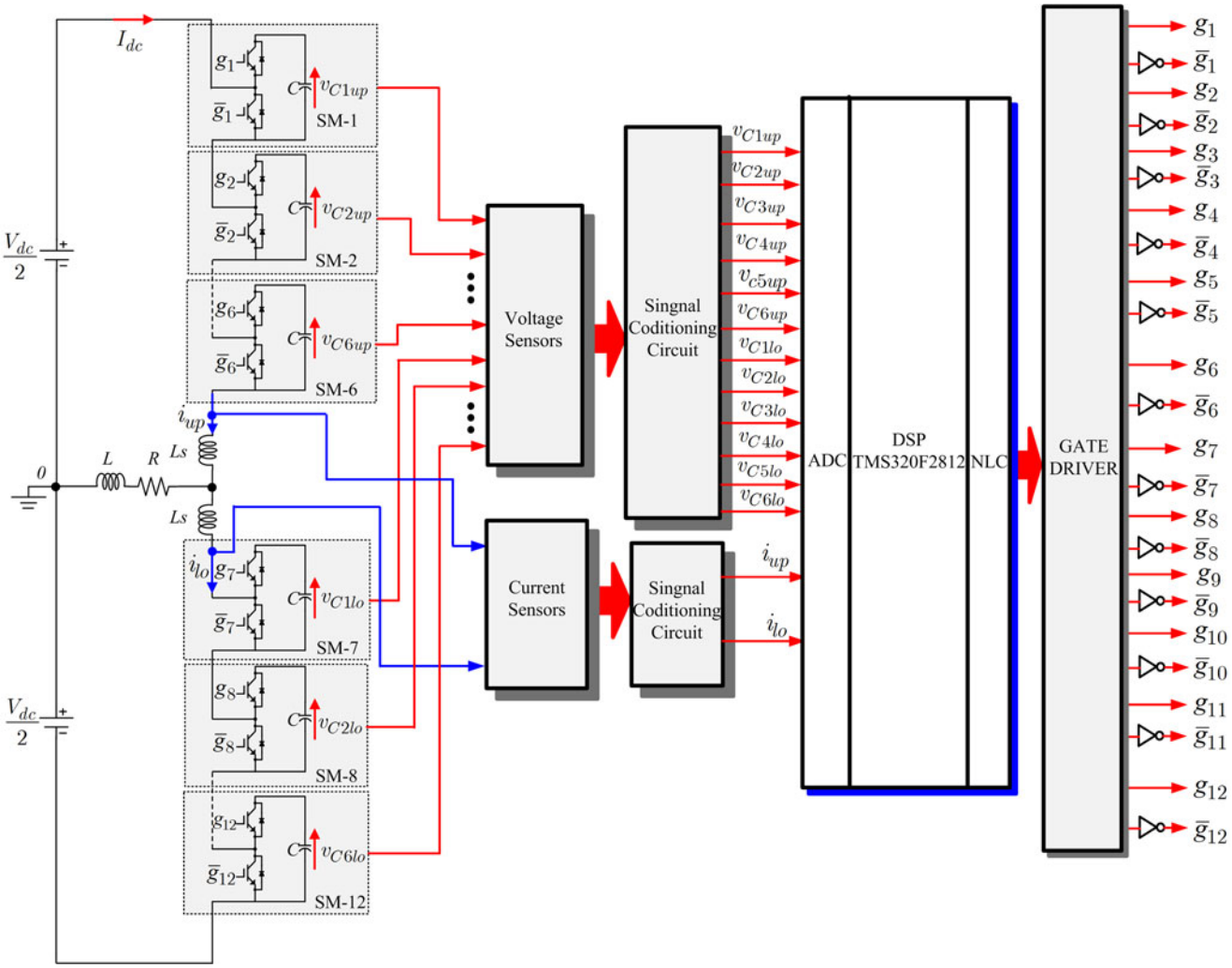

Fig. 17. Schematic of the proposed algorithm implementation for seven-level open-loop MMC.

stages of this method can lead to 60% saving in memory and the computational time of the processor at the implementation level compared to the existing balancing algorithms.

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